DESIGN AND IMPLEMENTATION OF MULTIPLE FAULT DIAGNOSIS ON VLSI CIRCUITS USING ARTIFICIAL NEURAL NETWORKS

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ABSTRACT

Artificial Neural Network (ANN) plays a vital role in VLSI circuits for diagnosing the faults in digital circuits. In this paper, a method for diagnosing the multiple faults in VLSI circuits using ANN is proposed [2]. First, the test pattern generation method injects the faults into the logic element of IEEE benchmark circuits. Second, injected faults are diagnosed using the ANN namely MLP, BPN and ART. And it's implemented on FPGA. The simulation result is obtained with modelsim ISE SC 6.2C software.

KEYWORDS: *ANN, BPN, MLP, ART, FPGA and VLSI circuits.*

I. INTRODUCTION

Testing of digital very large scale integration (VLSI) circuits has become a challenge and has gained more interest in recent years for several reasons, such as increase in the applications of digital circuits [1], integration of whole systems on single chips, and high cost of digital circuit testing. The high digital test cost results from many factors, such as expensive test equipment, long test development time, and long test production time.

The development and production test time cost constitutes a part of the development and production costs of the integrated circuits, respectively. The challenge faced by test engineers is to develop a test methodology to reduce the test cost and to accelerate the time-to-market without sacrificing integrated circuits (IC) quality. Consequently, the generation and evaluation of an effective test methodology is a very important issue in the production of an IC and has direct consequence on the price and the quality of the final product.

Normally digital signal processor (DSP) is used for the control strategy. However, neural network based intelligent control provides advantage of fast parallel processing, economical ASIC chip implementation, adaptability, and fault Tolerance capability. Traditionally, ANN has been implemented by a single or multiple DSPs [2]. The DSP technology has advanced tremendously in the recent years. However, the main disadvantage with DSP implementation is sluggishness due to sequential computation.

Artificial Neural Networks have been widely used in many fields. A great variety of problems can be solved with ANNs in the areas of pattern recognition, signal processing, control systems etc [3], Most of the work done in this field until now consists of software simulations, investigating capabilities of ANN model or new algorithms [2] [5]. But hardware implementations are also essential for applicability and for taking the advantage of neural network's inherent parallelism. In order to have an integrated understanding on neural networks, we adopt the next perspective, called top-down, from application, algorithm to architecture. The approach is application-motivated, theoretically based, and implementation oriented. The main applications are for signal processing and pattern recognition. The

algorithmic treatment represents a combination of mathematical theory and heuristic justification for neural models.

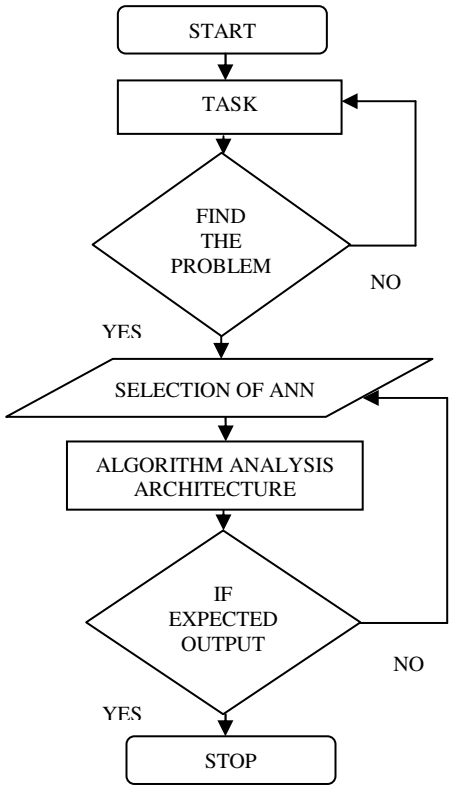

Figure 1.Neural Network Implementation Flowchart

The ultimate objective is the implementation of digital neuro computers, embracing technologies of VLSI, adaptive, digital and parallel processing. ANNs are biologically inspired and require parallel computations in their nature. Microprocessor and DSPs are not suitable for parallel designs. Designing fully parallel modules can be available by ASICs and VLSIs but it is expensive and time consuming to develop such chips. In addition the design results in an ANN suited only for one target application. FPGAs not only offer parallelism but also flexible designs, savings in cost and design cycle.

II. DESIGN OF ARTIFICIAL NEURAL NETWORKS

The development of ANN started 50 years ago. ANN is gross simplification of real network neurons. Due to complexity and incomplete understanding of biological neurons, various architectures of artificial neural networks have been reported in the literature [9].

ANN consist of many nodes, i.e. processing units analogous to neurons in the brain. Each node has a node function, associated with it which along with a set of local Back-propagation algorithm is a powerful algorithm for training MLPs. This learning consists of two passes through the different layers of network 1.forward pass and 2.reverse pass. In forward pass, weights are all fixed. In reverse pass, weights an adjustment is based on error produced between desired and actual output.

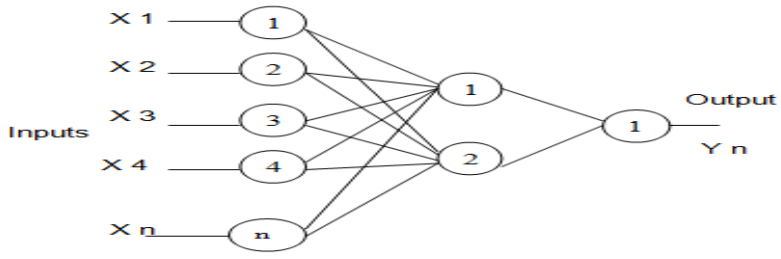

Figure 2. Neural network architecture

The BP learning process works in small iterative steps: one of the example cases is applied to the network, and the network produces some output based on the current state of its synaptic weights. A multilayered feed-forward artificial neural network (ANN) was used for evaluation. The processing elements of the models, called neurons, are arranged in a three-layer network. The first layer, called the input layer, connects with the input variables. There is one neuron for each of the input variables. As a result, the first layer consisted of maximally 17 neurons.
The last layer, called the output layer, connects with the output variables. There are two neurons in the output layer, which account for the two categories into which individuals have to be classified, namely present and absent. The layers between the input layer and the output layer are the hidden layers. In our case, an ANN with one hidden layer of 10 neurons was used. Neurons are connected with the neurons in the adjacent layers.

A. Back Propagation Networks (BPN)

BPN is systematic method for training multilayer artificial neural networks [5]. It has mathematical foundation that is strong if not highly practical. It is a multilayer forward network using extend gradient does not based delta learning rule, commonly known as a back propagation [4].BPN provides computationally efficient method for changing the weights in a feed forward networks,with differentiable activation function unit, to learn a training set of input-output examples. The aim of this network to train the net to achieve a balance between ability to respond correctly to the input patterns that are used for training and ability to provided a good response to the input that are similar.
A unit in the output layer determines its activity by following as two steps procedure

$$x_j = \sum_i yiwij \tag{1}$$

Where yi is the activity level of the jth unit is the previous layer and Wij the weights of the connetion between the ith and jth unit. Next ,the unit calculates the activity yj using some function of the total weighted input. Typically we use the sigmoid function.

$$Yi = \left[1 + e^{-xj}\right]^{-1} \tag{2}$$

Once the activities of all output units have been determined, the network computes the error E, which is defined by the expression

$$y_j = \frac{1}{1 + e^{-xj}} \tag{3}$$

Now my intention is for you to understand the structure of fully-interconnected neural network and how learning is achieved through the back propagation algorithm.

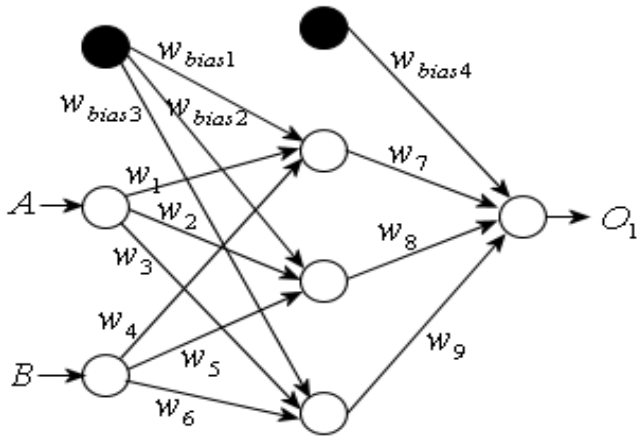

Figure 3. Fully-interconnected neural network

Process flow is the most important aspect of programming, which is always lacking in mathematical articles. Let's create a neural network version of the popular logic gate XOR.

Suppose a XOR function is to be estimated using a network such as below. Two truth tables are presented in the diagram, a XOR truth table, and a NOT-XOR truth table. The XOR logic gate has always been the choice when experimenting with neural network [3], so this time I decided on using its inverse, the NOT-XOR logic gate, So if you feel the need to estimate a XOR function.

B. Multilayer Perceptron Network (MLP*)*

MLP is an important class of neural networks. The networks consist of a set of sensory units that constitute the input layer and one or more hidden layer of computation modes. The input signal passes through the network in the forward direction. The network of this type is called MLP [5]. It's used with supervised learning and has led to the successful back propagation algorithm. The disadvantage of the single layer perceptron is that it cannot be extended to multilayered version. In MLP networks there exists a non-linear activation function. The MLP network also has various layers of hidden neurons. The hidden neurons make the MLP network active for highly complex tasks. The layers of the network are connected by synaptic weights. The output of the standard MLP network with m outputs can be expressed as:

$$\hat{Y}k(t) = \sum_{i=1}^{ni} w^{2}_{jk} F\left[\sum_{j=1}^{ni} w^{1}_{ij} v^{0}_{j}(t) + b^{1}_{j}\right]; 1 \le k \le m \quad (4)$$

Where w_{ij}^{1} And w_{ij}^{2} denote the weight of the connection between input and hidden layer, weights of connection between hidden and output layer, respectively b1j and v0i denote the thresholds in hidden nodes and inputs that are supplied in the input layer [8], respectively. F(•) is an activation function that is normally selected as a sigmoidal function. In the advent of VLSI circuits has resulted in increasing the number of components in a single chip. By this, probability of fault occurring in the circuits also increases. Due to this kind of problem, we should involve the process of fault diagnosis in the circuits. The task of problem, we should involve the process of fault diagnosis in the circuits [8]. The task of determining whether a fault is present or not is fault detection. And, the corresponding task of isolation the fault is fault location.

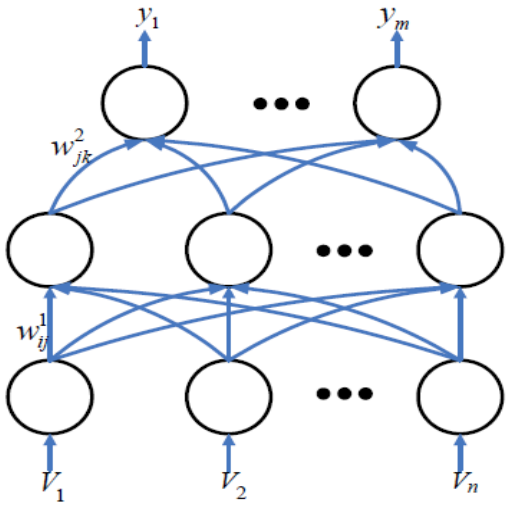

Figure 4. The MLP Network

The combined task of fault detection and location is referred as fault diagnosis. The problem with expert systems is that the labor required to acquire the knowledge needed to diagnose a given circuit board is very large. Artificial neural systems can perform the same tasks as expert systems. However, expert systems cannot do everything that artificial neural systems do because the structures of a neural network and an expert system are different. This structural difference and the mechanisms put in place to take advantage of this difference allow the neural network to learn, i.e. autonomously acquire knowledge.

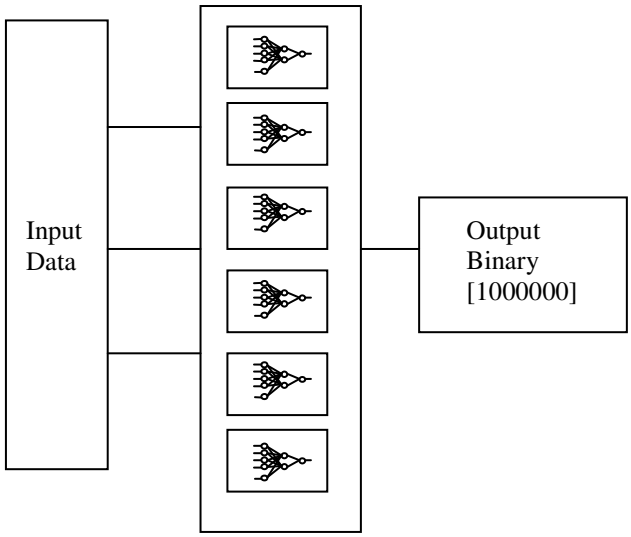

Figure 5.Implementation of neural network classification system

Artificial Neural Networks have been widely used in many fields. A great variety of problems can be solved with ANNs in the areas of pattern recognition, signal processing, control systems etc. Most of the work done in this field until now consists of software simulations, investigating capabilities of ANN models or new algorithms. But hardware implementations are also essential for applicability and for taking the advantage of neural network s inherent parallelism. There are analog, digital and also mixed system architectures proposed for the implementation of ANNs. The analog ones are more precise but difficult to implement and have problems with weight storage. Digital designs have the advantage of low noise sensitivity, and weight storage is not a problem. With the advance in programmable logic device technologies, FPGAs has gained much interest in digital system design.
A neural network (NN) is an interconnected group of natural or artificial neurons that uses a mathematical or computational model for information processing based on a connectionist approach to computation. In most cases an ANN is an adaptive system that changes its structure based on external or internal information that flows through the network [9]. The objective of fault diagnosis at the early production phase of ultra V LSI circuits is to guide the test engineers to search for the physical location of defects on a chip.

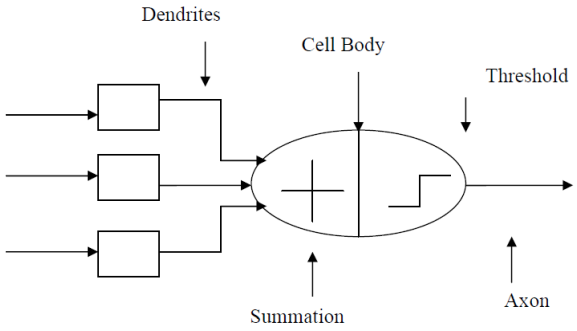

Figure 6.Neuron Model

The BIST,LFSR and CA based scheme has been reported to achieve better solutions in circuit diagnosis. In the above scenario, we report the design of an innovative diagnosis scheme for VLSI circuits. A particular class of CA referred to as Multiple Attractor Cellular Automata (MACA) is employed to realize the objective [13].

C. Adaptive Resonance Theory (ART)

ART requires a number of neurons in addition to the input units, cluster units and units for the comparison of the input signal with the cluster unit's weights.

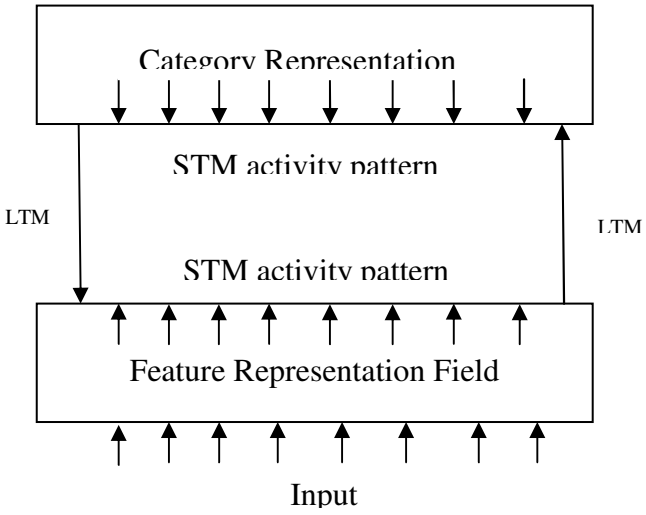

Figure 7.ART Architecture

ART nets are also called clustering nets with unsupervised learning. The fundamental of ART is studied by knowing its basic architecture, operation, its way of learning and the basic steps involved in training. During the training, information is encoded in the system by the adjustment of weight values. Once the training is deemed to be adequate, the system is ready to be put into production, and no additional weight modification is permitted.. Under such conditions, it is usually possible to define an adequate set of training inputs for whatever problem is being solved. Unfortunately, in many realistic situations, the environment is neither bounded nor stable. Consider a simple example. Suppose you intend to train a back propagation to recognize the silhouettes of a certain class of aircraft.

After the network has learned successfully to recognize all of the aircraft, the training period is ended and no further modification of the weights is allowed. If, at some future time, another aircraft in the same class becomes operational, you may wish to add its silhouette to the store of knowledge in your neural network. To do this, you would have to retrain the network with the new pattern plus all of the previous patterns. Training on only the new silhouette could result in the network learning that pattern quite well, but forgetting previously learned patterns. Although retraining may not take as long as the initial training, it still could require a significant investment.

III. TEST PATTERN GENERATOR

Since the cost of testing in VLSI chip is a significant fraction of the manufacturing cost, the time required to test a chip should be minimized, and there should be significant faults coverage. The objective of the automatic test pattern generator is to find an optimal set of test stimuli which detects all modeled faults, that is a set of test stimuli which when applied to the circuits can distinguish between the correct circuit and any circuit with a modeled fault.

The goal of the proposed approached is to compute a set of test stimuli that maximizes the fault coverage while minimizing test access.Therefore,the problem of test signal generation is optimization problem in principel.Test vector generation using deterministic techniques is highly complex and time consuming because of the extremely large search spaces involve. Therefore, artificial intelligence methods have gain much attention.

Neural algorithms are search optimization algorithms based on the mechanics of natural neural network that attempt to use similar methods for selection and reproduction to solve various optimization problems. Neural networks have proven to be effective in VLSI applications, including circuit layout and partitioning, cell placement, routing, and automatic test generation. The proposed method uses a neural network algorithm for the generation of the test stimulis which detects both catastrophic and parametric faults present in the circuit under test (CUT).

Here these papers implement both MLP and BPN. This algorithms are teaches the neural networks application to the test vector generator. The test vector generator produces the test pattern, that is all given to the CUT. In the CUT fixed as the digital circuits and we check the fault.

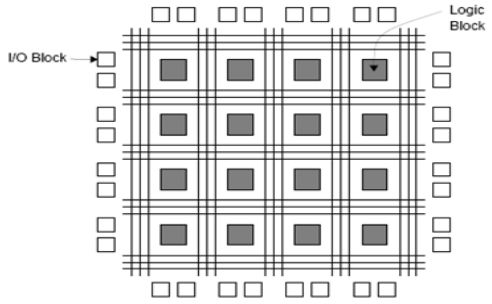

Figure 8. Simplified version of FPGA internal architecture

All fault features, can be classified based upon their effects upon the output voltages. The transformation of output voltage signals is achieved by using FFT. The systematic mathematical technique may be complicated to implement in practical real time control system.

The FPGA chip can be programmed using a language called hardware description language (HDL) [1], and this contains two types of the language.

BENCH MARK CIRCUITS

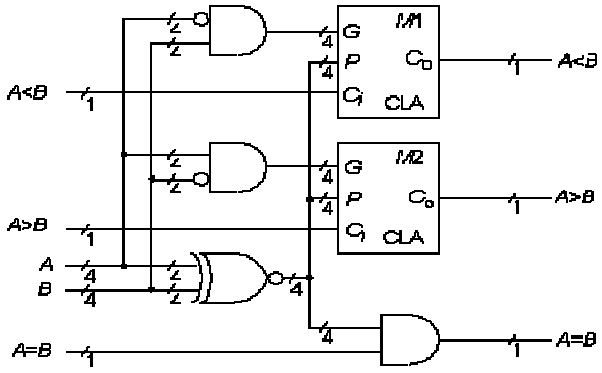

Figure9.74L85 Magnitude Comparator

A digital comparator or magnitude comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number. Comparators are used in a central processing units (CPU) and microcontrollers [12].

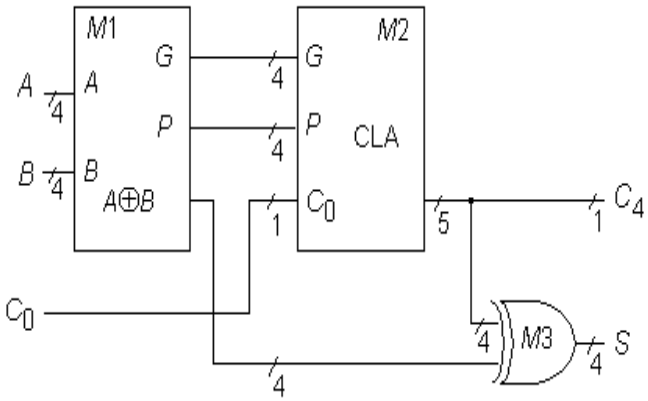

Figure 10.74283 4-Bit Adder

Addition is a fundamental operation for any digital system, digital signal processing or control system. A fast and accurate operation of a digital system is greatly influenced by the performance of the resident adders. Adders are also very important component in digital systems because of their extensive use in other basic digital operations such as subtraction, multiplication and division. Hence, improving performance of the digital adder would greatly advance the execution of binary operations inside a circuit compromised of such blocks. The performance of a digital circuit layout area and its operating speed.

The c6288 benchmark, whose multiplication function was previously known, represents a much larger gate-level circuit that also has a concise functional description. The figure above shows how the 2406 gates form 240 full and half adder cells arranged in a 15x16 matrix. 32 inputs; 32 outputs; 2406 gates an alternate representation is shown here, and the adder cells are detailed here.

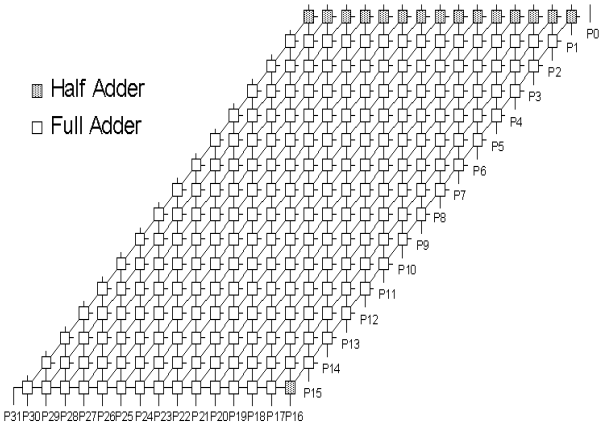

Figure 11.C6288 16x16 Multiplier

IV. FPGA-BASED NEURAL NETWORK DIGITAL MODEL IMPLEMENTATION

Once ANN is designed and trained, there are two main challenges in implementing it by FPGA [3]. First is the basic neuron implementation, and the second is to assure that the neurons in the same layer of ANN operate in parallel In order to achieve fast processing [18]. In a neuron, the input signals are multiplied by weight and then transfer function (TF) is applied to the result of the sum. The first step can be easily, but the TF implementation may be generally complex. If the TF is linear, for example it can be easily implemented by multiplication and sum operations. If the TF is nonlinear sigmoidal type, the implementations quite involved.

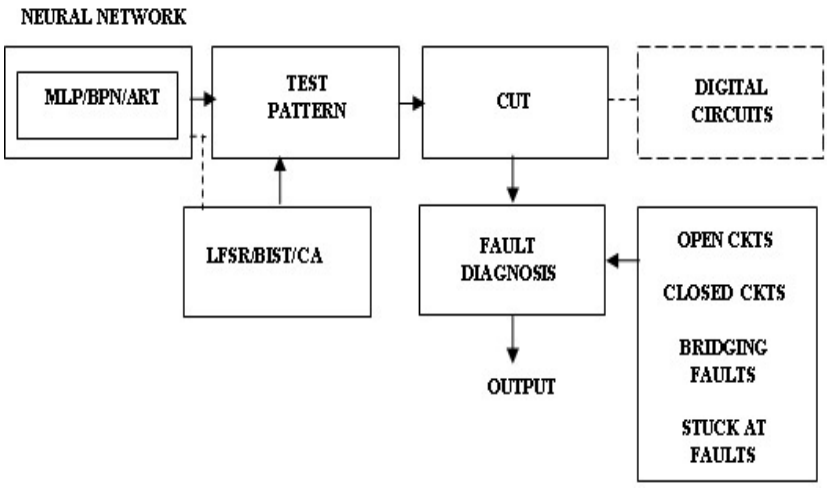

Figure 12. Block diagram Representation of Fault Diagnosis

The domain of the sigmoid in to seven intervals. The first and seventh intervals are interpolated by a constant, zero and one, respectively where as the remaining intervals used fifth order polynomials. The FPGA implementation of linear and log-sigmoid neurons, respectively [15]. The linear neuron is basically composed by the adder and multiplier, as Shown. At each transition (low to high), the adder and multiplier inputs (E0 and E1) are modified to perform new calculation.

V. RESULTS

The simulated outputs are as follows which shows output of sinusoidal wave based on the fault and fault free cycles of the sinusoidal output the comparator and four bit adder pulses are generated. The design of multiple fault diagnosis of VLSI circuits using ANN was implemented in a Xilinx 3E FPGA. The design was described using VHDL [3] [16]. The synthesis, placement and route are implemented in an ISE modelsim SC 6.2C environment and 54% slices of the FPGA were used.

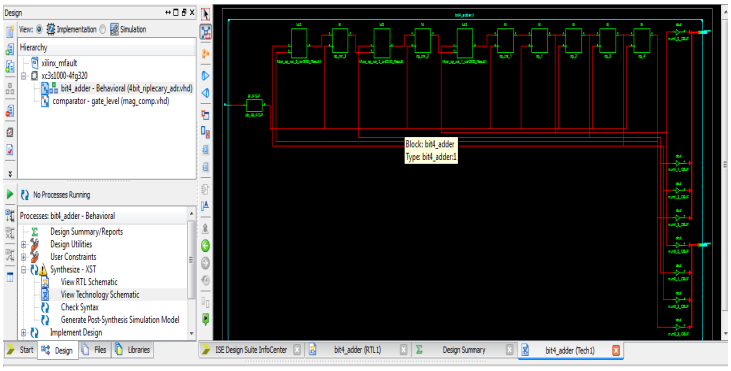

Figure 13. Four bit Adder Technology Schematic

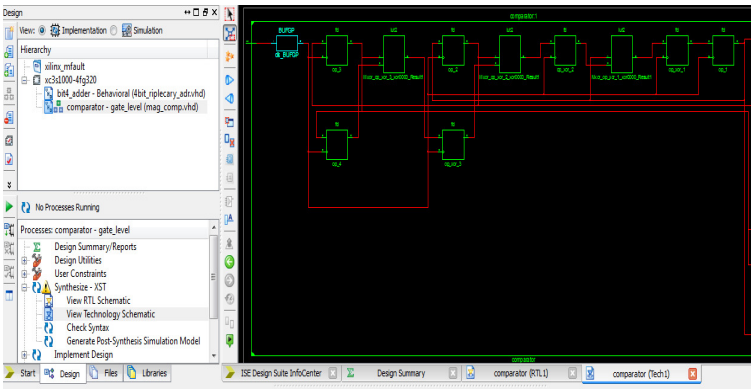

Figure 14.comparator schematic

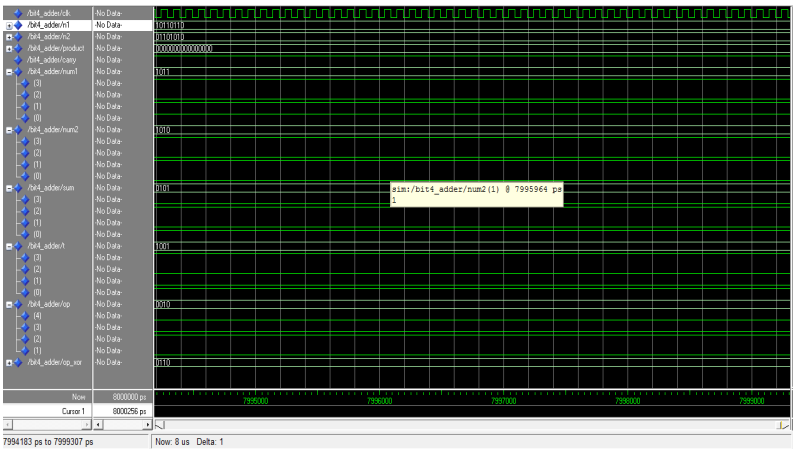

Figure 15. Four bit adder simulation

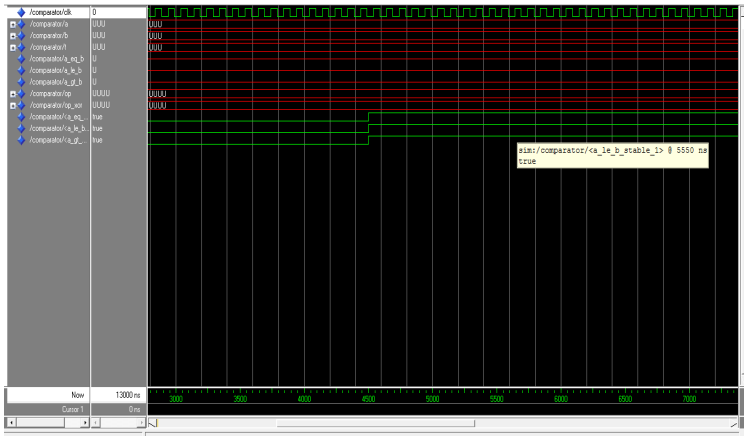

Figure 16.comparator simulation

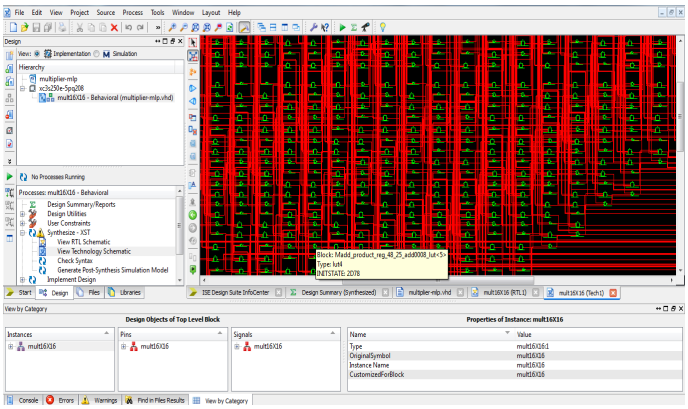

Figure 17.16x16 Multiplier Technology Schematic

Table 1. Comparison

	BPN			MLP			ART		
UNITS	4-BIT ADDER	MAGNITUDE COMPARATOR	16 X16 MULTIPLIER	4-BIT ADDER	MAGNITUDE COMPARATOR	16 X16 MULTIPLIER	4-BIT ADDER	MAGNITUDE COMPARATOR	16 X16 MULTIPLIER
Registers	7	7	7	7	7	7	6	6	6
1-Bit register	7	7	7	7	7	7	6	6	6
Xors	3	3	3	3	3	3	3	3	3
1-Bit Xors	3	3	3	3	3	3	3	3	3
IO Buffers	8	8	1	1	1	80	15	15	72
No of Slices	0 out of 2448 of 0%	0 out of 2448 of 0%	0 out of 2448 of 0%	0 out of 2448 of 0%	0 out of 2448 of 0%	260 out of 2448 of 10%	0 out of 2448 of 0%	0 out of 2448 of 0%	238 out of 2448 of 972%
NO of IO'S	9	1	1	33	33	97	30	30	72
No of Bounded IOB's	9 out of 158 of 5%	0 out of 158 of 0%	0 out of 158 of 0%	16 out of 158 of 10%	16 out of 158 of 10%	81out of 158 of 51%	15out of 158 of 95%	15 out of 158 of 95%	72 out of 158 of 45%
Total Real Time	7.00 Sec	5.00 Sec	7.00 Sec	8.00 Sec	4.00 Sec	7.00 Sec	7.45 Sec	3.76 Sec	6.78 Sec

VI. CONCLUSION

The research work is focused on diagnosing the faults in VLSI circuits using ANN. MLP network which is feed forward analyzing and it is used to identify the type and location of faults. BPN is a backtracking algorithm and it is found that the recognition accuracy of 100% is obtained with least computational complexity. MLP and BPN are the same area of ANN their approach for diagnosing

faults is completely different. ART recognizes the multiple faults in VLSI. Comparing to MLP and BPN, ART is best algorithm for diagnosis the faults [6]. Because execution time less. Number of slices usage also high.

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