LOAD COMPENSATION OF A DIESEL GENERATOR SET FOR AN OBSCURE SYSTEM USING DSTATCOM

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ABSTRACT
This paper deals harmonics, reactive power and unbalanced load current compensation of a Diesel Generator set for an isolated system using the control of Distribution Static Synchronous Compensator (DSTATCOM). Least Mean Square Based Adaptive Linear Element (ADALINE) method is used for the control of DSTATCOM. In order to extract balanced positive sequence real fundamental frequency component of the load current an ADALINE is used and in order to maintain a constant voltage at the dc-bus of a voltage-source converter (VSC) and to obtain a fast dynamic response a proportional-integral (PI) controller is used and are working as a DSTATCOM. Switching of Voltage Source Converter is achieved by using hysteresis-based Pulse Width Modulation (PWM) control. This scheme is simulated using MATLAB/SIMULINK for linear, nonlinear and Brushless DC (BLDC) motor loads. Results are given to verify the effectiveness of the control of DSTATCOM for the load compensation of the DG-SET.

KEYWORDS: *ADALINE, Brushless DC Motor, Diesel Generator Set, Distribution Static Synchronous Compensator (DSTATCOM).*

I. INTRODUCTION

The electricity generation by diesel engine-based unit (DG set and PMSG set) is a widely used in practice to feed the power to some crucial equipment in remote areas [1]-[3]. Distributed Generation sets used are loaded with un balanced, reactive, nonlinear loads and BLDC motors such as power supplies in telecommunication and medical equipments. The DG set is having high source impedance, and the unbalanced and distorted currents lead to the unbalanced and distorted three-phase voltages at point of common coupling (PCC). Nowadays, small generator units are available with full conversion (inverter-converter) units to meet stringent power quality norms [4]. Instead of using these, a DSTATCOM [3] can be used with a three-phase DG set to feed unbalanced loads without de rating the DG set and to have the same cost involved. For example, a 24-kW lagging power factor load of0.8 p f will consume 18 kVAR which is 60% of total kVA rating of a 32 kVA generator. The market price of an inverter is $50–70 per kVA which can be easily be configured to work as a DSTATCOM. Moreover, the DSATCOM can provide compensation for harmonics which facilitates to load the DG set up to its full kVA rating.

The DSTATCOM performance is very much dependent on the method of deriving reference compensating signals. Synchronous reference frame theory, method for estimation of reference currents by maintaining the voltage of dc link, instantaneous reactive power theory, modified p-q theory and instantaneous $id-iq$ theory for estimation of reference currents by maintaining the voltage of dc link are generally reported in the literature for an estimation of reference currents for the DSTATCOM through the extraction of positive-sequence real fundamental current component from the load current [5]–[8]. These techniques generally incorporate a set of low-pass filter which results in a delay in the computation of reference currents and therefore leads to slow dynamic response of the DSTATCOM.

The control of DSTATCOM with capabilities of reactive power, harmonics and unbalanced load compensation is achieved by Least Mean Square (LMS) algorithm [9], [10] based adaptive linear

element (Adaline). The Adaline is generally used to extract positive-sequence fundamental frequency real component of the load current. The dc-bus voltage of voltage source converter(VSC) is supported by a proportional–integral (PI) controller which computes current component to compensate losses in DSTATCOM. The modeling of the DG set is performed using a synchronous generator, a speed governor, and the excitation control system.

In this paper, a fast and simple neural network-based control scheme is used to estimate reference source currents for the control of the DSTATCOM. This paper presents a DSTATCOM for the load compensation of a diesel generator set to increase its performance.

This proposed system is simulated by MATLAB/Simulink *[11]*. The results for a 32-kVA DG set with the linear load at 0.8 lagging pf and a nonlinear load with different load dynamics and unbalance load conditions are presented to demonstrate the effectiveness of DSTATCOM-DGset system.

II. CONFIGURATION OF THE SYSTEM

Fig.1 shows the configuration of the system for a three phase three-wire DG set feeding to variety of loads such as linear, nonlinear and Brushless DC (BLDC) motor loads. A 32 kVA system is chosen to demonstrate the work of the system with the DSTATCOM. The DSTATCOM comprising of an insulated gate bipolar transistors-based three-phase three-leg Voltage Source Converter system. The load current is tracked using Adaline-based reference current generator, which in conjunction with the hysteresis-based PWM current controller that provides switching signals for VSC-based DSTATCOM. It controls source currents to follow a set of three-phase reference currents. The parameters of a salient pole synchronous generator are 415 V, 32 kVA, 4 pole, 1500 rpm,50 Hz, X_d = 1.57 pu, X^1_d= 0.155 pu X^{11}_d = 0.115 pu, X_q =0.79, X^1_q = 0.17, X^{11}_q = 0.5, H_s = 0.08. The other critical parameters are given in Table I.

TABLE 1: SYSTEM SPECIFICATIONS

Load-1	Linear Load	Delta connection R-L load of 39 kvA at 0.8 pf
Load-2	Non Linear Load	29 kW diode bridge converter with LC filter at output with L=2Mh, and c=500 uF
Load-3	BLDC motor	Snubber resistance = 500 ohm, snubber capacitance = 1uF capacitance = 1000uF
Voltage Source Converter		DC link capacitor C=10000 uF L = 3.6mH, ripple filter c= 13uF R = 9 ohm, f = 20kHz

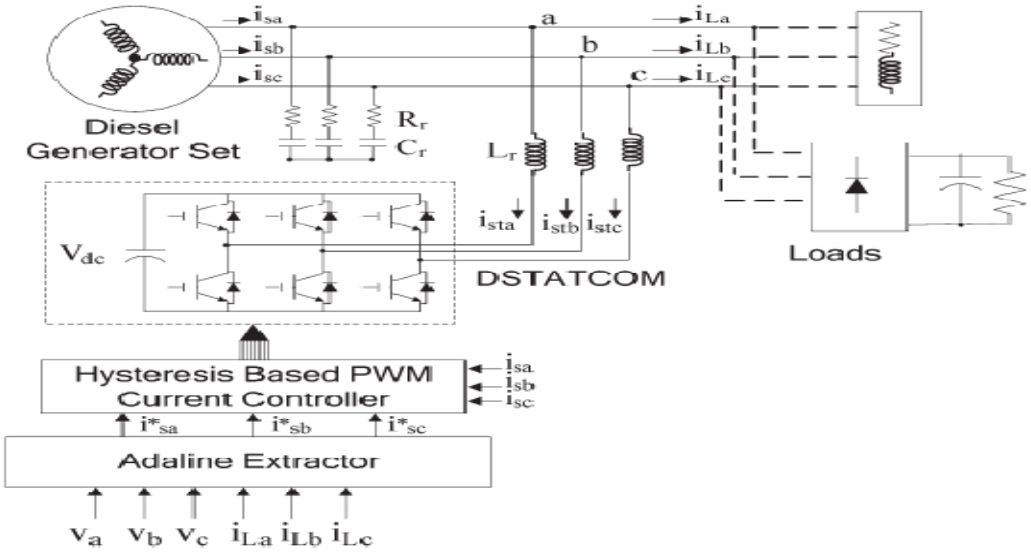

Fig.1. Basic configuration of the diesel generator set with DSTATCOM

III. PROPOSED CONTROL METHODOLOGY

DG set is required to this system to supply real power required to the load and some losses (switching losses of devices used in VSC, losses in the reactor, and dielectric losses). The DSTATCOM consisting of two parts, one is real fundamental frequency component of the load current, which is being extracted using Adaline and another component, which corresponds to the losses in the DSTATCOM, are estimated using a PI controller over dc voltage of DSTATCOM. Fig. 2(a) shows the control scheme for the implementation of reactive, unbalanced and harmonic currents compensation. The output of the PI controller is added to the weight calculated by the Adaline to maintain the dc-bus voltage of the DSTATCOM.

3.1 Real Positive-Sequence Fundamental Frequency Current Extraction from Load Current

The proposed decomposer's basic theory is based on LMS algorithm [10] and its training through Adaline, which tracks unit voltage vector templates to maintain minimum error which is given. For an ac system, the supply voltage may be expressed as

$$v_s = V \sin \omega t \tag{1}$$

where *vs* is the instantaneous ac terminal voltage, *V* is an amplitude and ω is the angular frequency of the voltage. The load current (i_L) consists of active current (i_p^+), reactive current (i_q^+) for the positive sequence, negative-sequence current (i^-), and harmonic frequency current (i_h) can be written as summation of different parts as

$$i_L = i_p^+ + i_q^+ + i^- + i_h \tag{2}$$

The control algorithm is based on the extraction of the current component in phase with unit voltage template. To estimate the fundamental frequency positive-sequence real component of load current, the unit voltage template should be in phase with the system voltage and should have unit amplitude. The unit voltage template (*up*) derived from the system phase voltage can be represented as:

$$u_p = v_s / V \tag{3}$$

For proper estimation of the current components of the load current, the unit voltage templates must be undistorted. In case of the voltage being distorted, the zero crossing of phase voltage is detected to generate sinusoid (sin ωt) vector template, synchronized with system terminal voltage. This signal is generated from the look-up table by adjustment of the delay to track the change in the frequency of the system.

An initial estimate of the active part of load current for single-phase can be chosen as

$$i_p^+ = W_p u_p \tag{4}$$

where weight (W*p*) is estimated using an Adaline. This weight is variable and changes as per the load current. The scheme for estimating weights corresponding to fundamental frequency real component of load current (for three-phase system), based on LMS algorithm-tuned Adaline tracks the unit vector templates to maintain minimum error. The estimation of the weight is given as per the following iterations:

$$W_{p(k+1)} = W_{p(k)} + \eta\{i_{L(k)} - W_{p(k)} u_{p(k)}\} u_{p(k)} \tag{5}$$

where subscript k and k + 1 represent sample instant and η is the convergence coefficient. The value of convergence coefficient decides the rate of convergence and the accuracy of the estimation. The practical range of convergence coefficient lies in between 0.1 to 1.0. Three-phase reference currents corresponding to positive-sequence real component of the load current may be computed as

$$i_{pa}^+ = W_p^+ u_{pa}; i_{pb}^+ = W_p^+ u_{pb}; i_{pc}^+ = W_p^+ u_{pc} \tag{6}$$

$$W_p^+ = (W_{pa}^+ + W_{pb}^+ + W_{pc}^+)/3 \tag{7}$$

w is averaged weight. Weights of phase a, b and c are averaged to compute the equivalent weight for positive sequence current component in the decomposed form. The averaging of weights helps in removing the unbalance in load current components.

3.2 PI Controller for Maintaining Constant DC-Bus Voltage of DSTATCOM

In order to compute the second component of reference active power current, a reference dc-bus voltage is compared with sensed dc bus voltage of DSTATCOM. This comparison of sensed dc-bus voltage (*v*dc) to the reference dc-bus voltage (v^*_{dc}) of VSC, results in a voltage error (*vdc*), which in the nth sampling instant is expressed as

$$v_{dcl(n)} = v^*_{dc(n)} - v_{dc(n)} \tag{8}$$

This error signal is processed in a PI controller and output at the nth sampling instant is expressed as:

$$I_{p(n)} = I_{p(n-1)} + K_{pdc}\{v_{dcl(n)} - v_{dcl(n-1)}\} + K_{idc}v_{dcl(n)} \tag{9}$$

The output of the PI controller accounts for the losses in DSTATCOM and it is considered as the loss component of the current, which is added with the weight estimated by the Adaline corresponding to fundamental frequency positive sequence reference active current component. Therefore, the total real reference current has component corresponding to the load and component corresponding to feed the losses of DSTATCOM, is expressed as

$$\begin{aligned} &i^*_{sa} = (W^+_p + I_p)u_{pa}; i^*_{sb} = (W^+_p + I_p)u_{pb}; \\ &i^*_{sc} = (W^+_p + I_p)u_{pc} \end{aligned} \tag{10}$$

These three-phase currents are considered reference source currents *iref* ($i^*_{sa}, i^*_{sb}, i^*_{sc}$) and along with sensed source currents *iact* (*isa*, *isb* and *isc*), these are fed to the hysteresis based PWM current controller to control the source currents to follow these reference currents. The switching signals generated by the PWM current controller force actual source currents to acquire shape close to the reference source currents. This indirect current control results in the control of the slow varying source current (as compared to DSTATCOM currents) and therefore requires less computational efforts. Switching signals are generated on the following logic:

if $(i_{act}) > (i_{ref} + hb/2)$ upper switch of the leg is ON and lower switch is OFF

if $(i_{act}) > (i_{ref} + hb/2)$ upper switch of the leg is OFF and lower switch is ON

where *hb* is hysteresis band around the reference current *i*ref . The weights are computed online by LMS algorithm. The update equation of weights based on LMS algorithm is described in (5) for each phase. The structure of such Adaline is depicted in Fig. 2(b). Weights are averaged not only for averaging at fundamental frequency but to cancel out sinusoidal oscillating components in weights present due to harmonics in the source current. The averaging of weights in different phases is shown in Fig. 2(a). Thus Adaline is trained at fundamental frequency of a particular sequence in-phase with voltage. Fig. 2(a) and(b) show the detailed scheme implemented for control of DSTATCOM.

Because of the unbalance in the load currents, a second harmonic ripple is produced in the dc-bus voltage. Similarly, harmonics in the load currents also produce ripple at dc-bus voltage. However, this ripple is at higher frequency as compared to the second harmonic ripple. These ripples have to be filtered out before feeding the signal of the PI controller; otherwise this may introduce the harmonics component in source currents (predominantly because of harmonic ripple at dc bus). For this purpose the dc-bus voltage is filtered using a low-pass filter (LPF). Since major amount of reference current (load real current component) is computed using Adaline-based extractor, effect of the delay caused by the LPF is negligible in practical cases.

IV. MATLAB BASED SIMULATION MODEL

Fig.3(a) shows the MATLAB based simulation model with linear and nonlinear loads with DG set isolated systems and Fig.3(b) shows the MATLAB based simulation model with BLDC motor load. The modeling of the DG set is carried out using a star connected synchronous generator of 32 kVA, controlled by a speed governor and an excitation system. The linear load applied to the generator is at 0.8 lagging pf which is modeled as a delta connection of the series combination of resistance and inductance (R-L) models. The nonlinear load is modeled using discrete diodes connected in a bridge with a capacitor filter and a resistive load on the dc bus. The unbalanced was realized by disconnecting phase-a from the diode bridge.

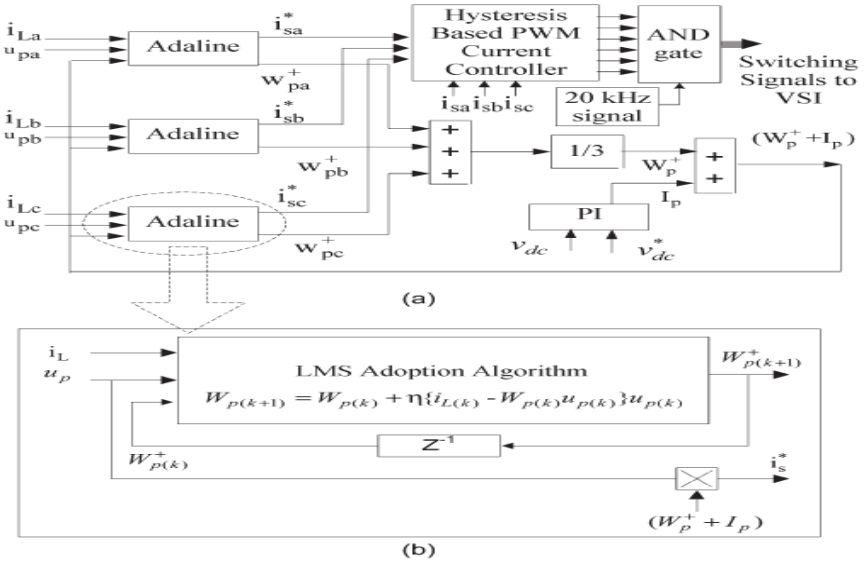

Fig. 2(a),(b). Control block diagram of the reference current extraction scheme.

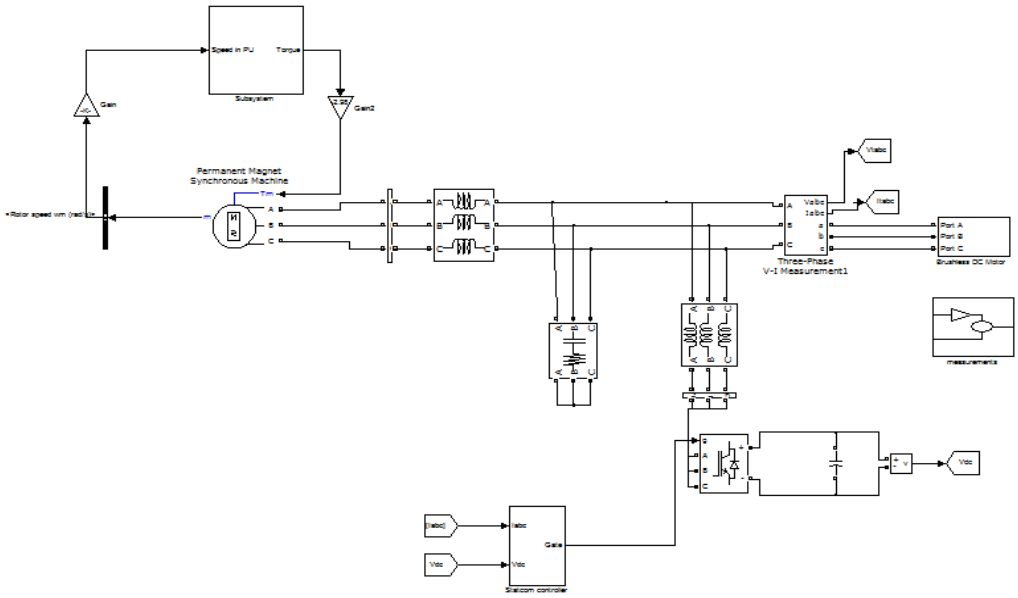

Fig.3(a).MATLAB based simulation model (with linear, nonlinear and BLDC motor loads)

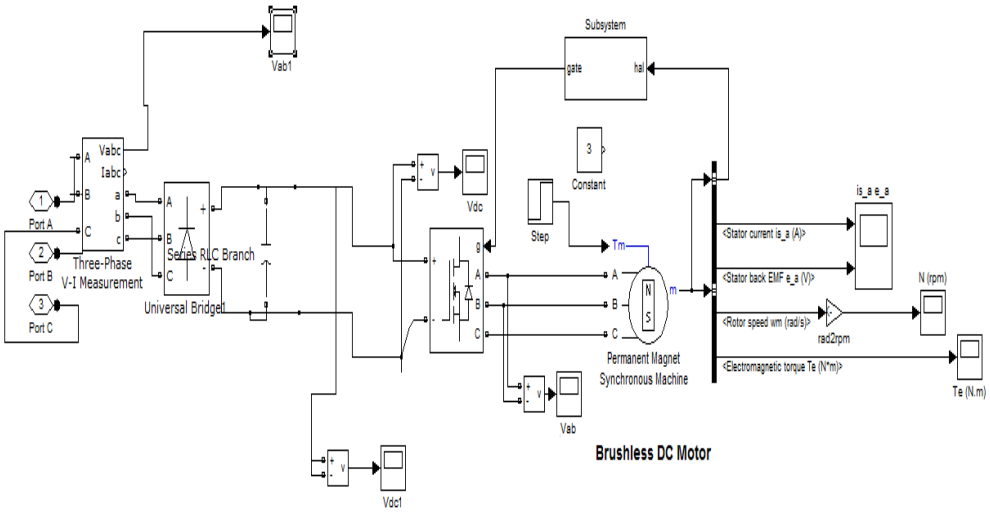

Fig. 3(b).MATLAB based simulation model with BLDC motor load

V. RESULTS AND DISCUSSION

The simulation of the DSTATCOM-DG isolated system is carried out with different types of loads i.e., a linear R-L load, a nonlinear load i.e., a diode bridge converter load and BLDC motor load. The following observations are made on the basis of obtained simulation results under different system conditions.

5.1 DG Set System Operation under Linear Load

Fig. 4 shows the dynamic performance of the DSTATCOM-DG isolated system with linear load. From t =0.01 s to 0.05 s, a three-phase 18.75-kVA load at 0.8 pf is being connected. At t = 0.05 s, the load is increased up to 39 kVA at 0.8 pf. The real power supplied by the DG set is 30 kW and reactive power is supplied by the DSTATCOM. At t = 0.20 s, an unbalanced is introduced in the load by taking off load from phase a. It can be easily observed that even if load currents (i_L) are unbalanced, the source currents (*is*) are still balanced. At t = 0.25 s, the load is taken out from phase b also, even in this condition the DSTATCOM system is able to balance DG set currents. For time t = 0.32 s to t = 0.35 s these dynamics are shown in the reverse sequence of events. The dc-bus voltage of VSC is well maintained at 800 V during the complete range of operation and the small sag and swell in the voltage at the load change are compensated by the PI controller action.

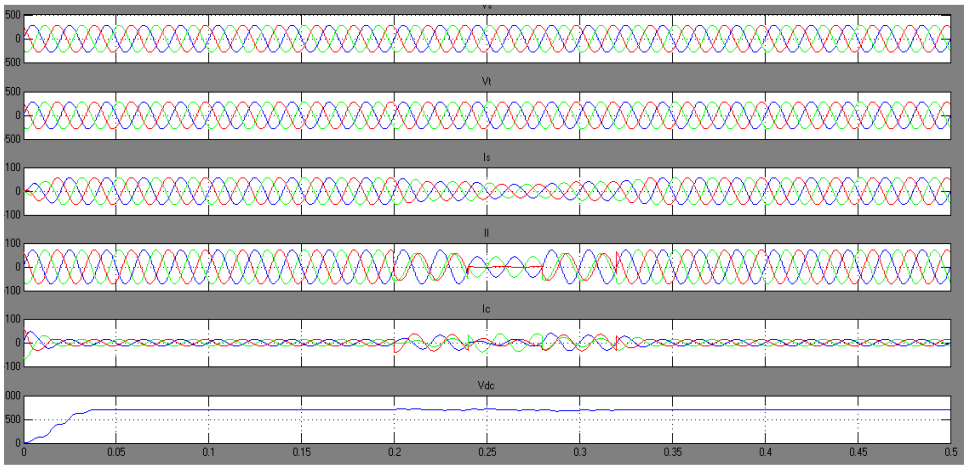

Fig. 4. Dynamic performance of the DSTATCOM-DG isolated system with linear load.

5.2 DG Set System Operation under Non-Linear Load

Fig. 5 shows the dynamic performance of the DSTATCOM- DG set with isolated system under nonlinear loading conditions. The load on the system is kept 15.0 kW initially for time t = 0.01 s to 0.10 s. The load compensation in terms of harmonic mitigation is also being provided by the DSTATCOM during this condition. The load is increased to 29 kW at t = 0.10 s. At t = 0.20 s, an unbalanced is introduced in load and therefore the load is reduced to 16.4 kW. At t = 0.70 s, phase-a load is reconnected again to the diode bridge and the load is reduced to its initial value.

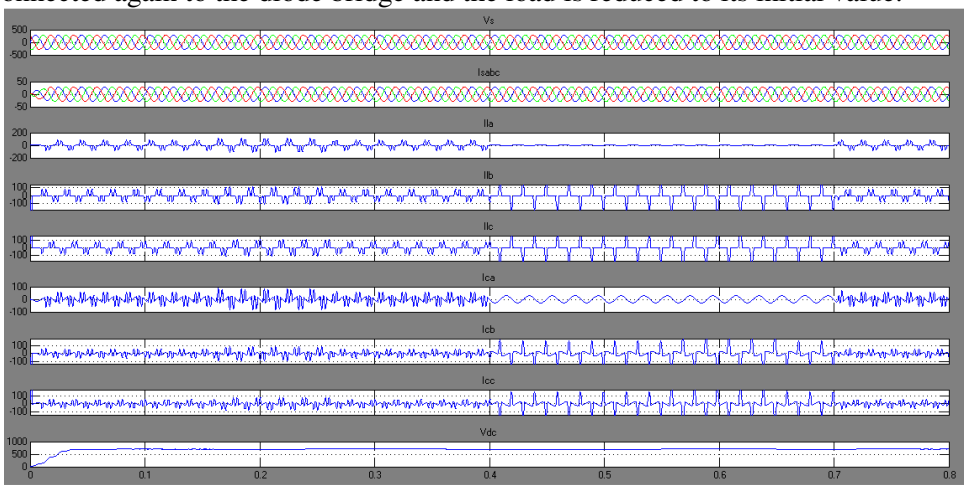

Fig. 5. Dynamic performance of the DSTATCOM-DG isolated system with nonlinear load.

5.3 PMSG Set System Operation under BLDC motor Load

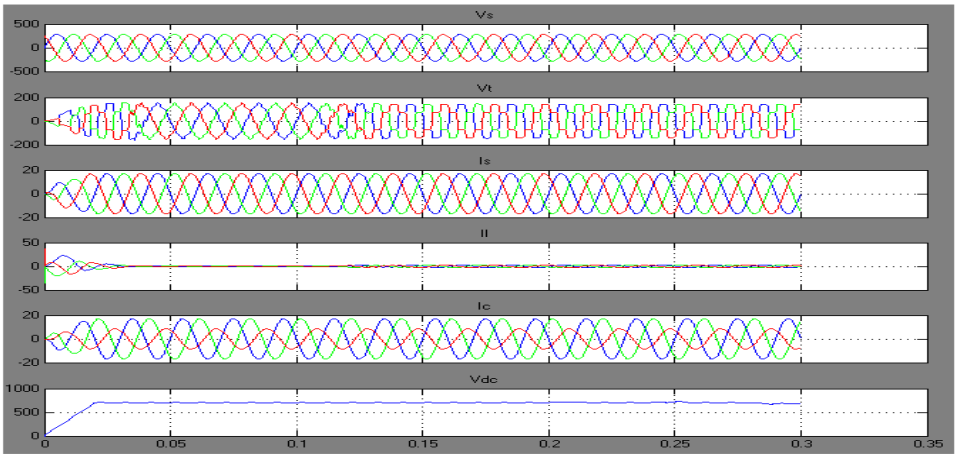

Fig. 6. Dynamic performance of the DSTATCOM-PMSG isolated system with BLDC motor load.

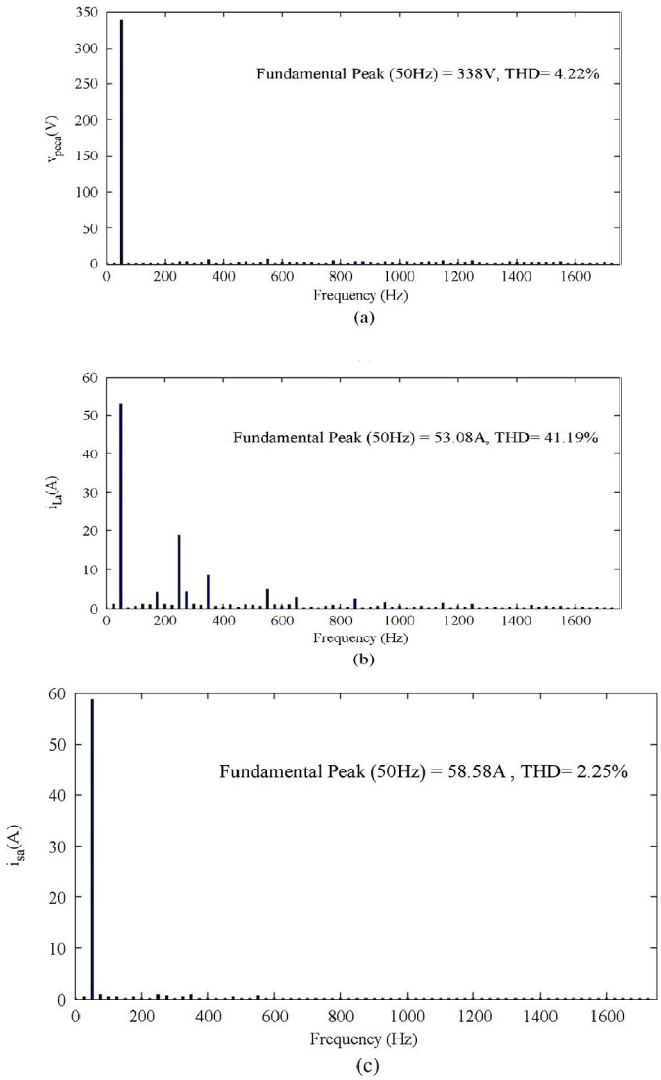

Fig.7. Harmonic spectrum of phase-a (a) Voltage at PCC, (b) Load current and, (c) Source current at peak nonlinear load condition.

Fig. 6 shows the dynamic performance of the DSTATCOM-PMSG set with isolated system with BLDC motor load. The load on the system is kept 15.0 kW initially for time t = 0.01 s to 0.10 s. The load is increased to 29 kW at t = 0.10 s. From the Fig.6, it is observed that the source current becomes pure sinusoidal. Fig.7 shows the Harmonic spectrum of phase-a, (a) Voltage at PCC (b) Load current and (c) Source current at

peak nonlinear load condition. It is observed that the % THD is reduced to 2.25% for source current at peak non linear load condition.

VI. CONCLUSION

The proposed control algorithm of the DSTATCOM has been found to improve the performance of the isolated DG system. The DSTATOM has compensated the variety of loads on the DG set and it has sinusoidal voltages at PCC and currents with compensated and equivalent linear balanced unity power factor loads. The cost of the installation of DSTATCOM system with the DG set can be compensated as it leads to less initial and running cost of DG set as its ideal operation while feeding variety of loads (linear, nonlinear and BLDC loads). It is observed that the % THD is reduced 41.19 % to 2.25% for source current at peak non linear load condition.

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