IMPACT OF BUFFER DRIVER STRENGTH ON CROSSTALK NOISE PROPAGATION IN GLOBAL INTERCONNECTS

Swatilekha Majumdar[1] and Jatinder Pal Singh Sahota[2]
[1]Department of VLSI and Embedded System, IIIT Delhi, Delhi-110020
[2]ST Microelectronics, Greater Noida, UP-201308

ABSTRACT

Shrinking technology has allowed the design engineers to come up with chips with large number of blocks compacted in smaller area, to have whole system-on-chip. This has led to close proximity of wires on chip giving rise to one of the crucial phenomenon affecting the circuit timing delay and functionality: the crosstalk. Crosstalk occurs due to the presence of coupling capacitance between the wires. Drive strengths of the cells put on wires is one of the prime factors determining the life of crosstalk bump. This paper gives an insight to the drive strength impact of aggressor, victim and victim's receiver on crosstalk bump in lower technology nodes. Our analysis show that the buffers added to the on-chip routing during the static timing analysis can be exploited to reduce the on-chip interconnect noise. We also analyse the effect of driver strength on the crosstalk noise. It can be seen that optimum buffer sizing is required to properly handle the issue of on-chip interconnect. Re-sizing the buffers by increasing the driver strength to 8X reduce the crosstalk noise by almost 80%, which significantly increases the system performance.

KEYWORDS: *System-on-chip, crosstalk, coupling capacitance, wireload model, interconnect.*

I. INTRODUCTION

With the advent of technology, the interconnect size is shrinking. Thickness of wire is being increased to decrease the resistance offered by the wire contributing to the wire delay. Simultaneously the wire width is being decreased to pack more wires on the chip. Thus the ratio of coupling capacitance to the ground capacitance has increased. For digital circuits, when a signal flows through a wire from a logic block, it contains information in form of logic low or logic high. The wire gets charged or discharged according to the logic it transmits at a time. In older technologies the wire used to get charged in a short span of time but now it takes substantial amount of time to charge which is comparable or even more than the cell delay.

It can be inferred from the above statements that the increasing frequency of operation and decrease in feature size have become dominant factors in determining the performance of a circuit. With each successive technology generation, wires are spaced closer to each other and also have more skewed aspect ratios, resulting in increased levels of coupling capacitance in each generation, which can cause a switching net to induce large noise spikes on its neighbouring nets [1]. This effect is amplified if the neighbouring wires have transitions in opposite directions. The crosstalk between wires, called as the "victim" wire (the wire being affected) and the "aggressor" wire (wire affecting the victim wire), affect not only the timing delays of the wire but also the circuit functionality. The crosstalk noise spike might lead the receiver of the wire to believe that the input obtained by it is logic high, but in actual the signal transmitted was logic low.

Various works proposed in literature have worked on solving this burning issue which pertains to the deep-submicron era. In work by Lee et al. [2], a 95 fJ/b current mode transceiver is designed for on-chip interconnects. The transceiver has a BER< 10^{-12} and a data rate of upto 4 Gb/s. In [3], Mensink et al. proposed a voltage mode signalling capacitive boasting for low power on-chip interconnects. The scheme uses aggressive equalization schemes at the receivers and transmitters to increase data rate over RC interconnect and reduce the crosstalk. In [4] and [5], the authors exploited the RC time

constant of the wire (metal routing) to handle the issue of interconnects for fast sensing memory designs.

To reduce the timing delay from one logic block to another, buffers of different drive strengths are inserted across the wire length. These buffers or buffers have the capability to drive the wire and propagate the signal across it reducing the delay of the wire [2]. These buffers/buffers also provide path for the wire capacitor and coupling capacitor to discharge or charge according to the logic on the wire.

This paper gives an insight to the effect of driver strength of the buffers used across the wire sections to reduce delay on the crosstalk bump as generated by the coupling capacitance between the wires. The simulations have been performed for 40nm technology using spice (ELDO). The paper is organised as follows: Section II talks about the basic wireload model. The impact of buffers added to the on-chip routing (wires) on the crosstalk noise generated is discussed in section III. Section IV talks about the experimental simulation and setup used for this work. Section V concludes the paper and section IV talks about the future prospects of the understanding of such phenomena in deep-submicron technology.

II. WIRELOAD MODEL

In the case of long, global buses, crosstalk can become a serious limiting factor in the timing verification of the design [6]. To handle this problem, wires are divided in sections and these sections contain buffers which act as crosstalk suppressor. But the selection of buffer size here becomes an important factor, since larger buffers will lead to high power consumption.

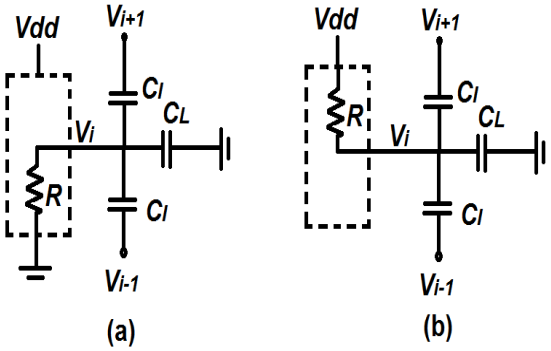

Fig. 1. Equivalent circuit for buffer drivers used in global interconnects (a) when the pull-down transistors of the driver are on (b) when the pull-up transistors of the driver are on

Whenever the delay of wire is to be calculated, the wire is represented in form of wire load model which is a combination of RC circuit. This representation of the wire is due to the body capacitance effect of the wire. The wires in new technology charge one section at a time and as a whole as was in older technology. While calculating the wire delay, the transmitter and the receiver for each wire sections are generally not considered. But if we consider the transmitter and the receiver driver, we will see that the driver also contributes to the total RC for the wire delay.

According to [6], to calculate the energy consumed by the circuit, we need to represent the driver transmitter and the receiver as a combination of resistances and capacitances. Thus, line drivers also contribute to the total resistance and capacitance of the wireload model. Figure 1(a) signifies the equivalent circuit of driver when NMOS is on and 1(b) signifies the equivalent circuit of driver when the PMOS is on. The NMOS and PMOS are represented by resistances. C_I is the coupling capacitance between victim and aggressor wires and C_L is the capacitance of the wire with respect to the substrate.

III. IMPACT OF BUFFER DRIVER STRENGTH ON CROSSTALK NOISE

As the drive strength of buffer increases, the input capacitance or the load capacitance offered by the buffer to previous stage increases. This is because, to increase the drive strength of the buffer, the width of the transistor is increased. So the bump generated at previous stage is suppressed to some extent. In actuality, the width of the buffer not physically increased but is done by connecting transistors in parallel. This will facilitate an equivalent transistor of greater width and also the resistance of the transistor will be reduced as compare to transistor, if created by increasing the width

by fabrication. Suppression of bump occurs because higher drive strengths are slowing down response of previous stage driver, by increasing its load. It needs more time to respond to bump at its input. From this we can say that, the trend for the increase in drive strength to the crosstalk bump is a linearly increasing plot.

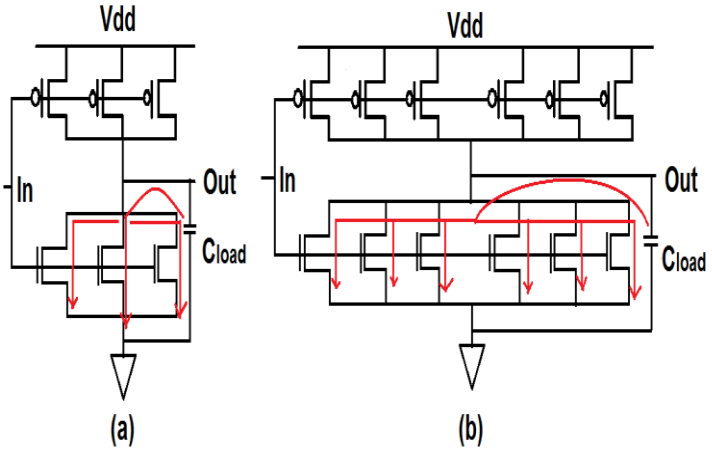

Fig. 2. Load capacitance of buffer with different driver strengths- (a) Buffer size x3 (b) buffer size x6

Figure 2 shows the discharge path of output load capacitance for different buffer driver strengths (x3 and x6). In the first case, the output load capacitance is being discharged by 3 pull-down transistors, whereas in the second case it is being discharged by six pull-down transistors. Since the number of pull-down transistors is more in the second case, the discharge will be faster for larger buffer strengths.

IV. EXPERIMENTAL SIMULATION AND ANALYSIS

For experimental simulation, two cases are considered- how will a single standalone buffer behave to a crosstalk noise of Vdd/2 of significant time duration and; how will the buffered global wire behave to a crosstalk noise of Vdd/2 with significant time duration. It is expected that on increasing the driver strength of the buffer, height of bump obtained at output will decrease among different drive strengths. A crosstalk noise of Vdd/2 is considered as this voltage can flip the data stored on/transmitted by the global wire.

4.1. Standalone buffer behaviour to crosstalk noise

An input voltage bump of height Vdd/2 (0.6V) and width of 200ps is considered as the input crosstalk bump. We will analyse how different buffer drive strengths respond to this voltage bump and how much suppression we observe at the output of the output.

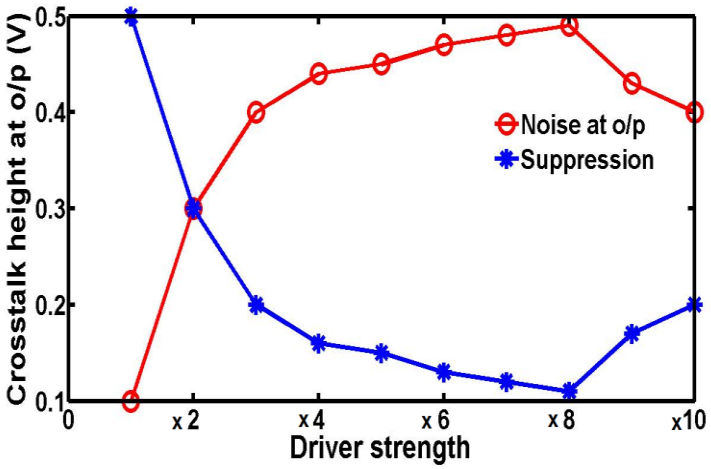

Fig. 3. Crosstalk noise and amount of noise suppressed at the output of standalone buffer. The noise suppression is not entirely linear as speculated

Figure 3 shows the crosstalk noise suppressed at the output of a standalone buffer. We can observe from the figure that the smaller drive strength buffer have lesser noise height at the output of the inverter as compared to the higher driver strength inverters. In other words, the crosstalk noise suppression is more for lower buffer strengths. This is because; the lower buffer drive strength has transistors with less width (or less number of pull-down transistors) which contribute to low capacitance but very high resistance value, resulting in a high RC time constant. This means that the output capacitance will not charge quickly to give a sharp output noise level, rather it will charge slowly. The time for which the crosstalk noise occurs is not enough for the output load capacitance to get significantly charged.

In addition to this, we also notice that for some buffers which have higher drive strengths, start suppressing crosstalk noise. The reason for this phenomenon is that their own parasitic output capacitance made them slower than their counterparts, and thus less responsive to input crosstalk noise.

The crosstalk noise that affects the wire in system-on-chip does not only vary in amplitude, but also in duration. Thus, analysing the effect of buffer strengths on crosstalk noise duration also needs to be taken care of. For this part of the experiment we have kept the crosstalk noise amplitude constant and varied the crosstalk noise duration. Figure 4 shows the effect of buffer size on crosstalk noise of varying crosstalk noise duration. We can observe from the figure that as the crosstalk duration increases the crosstalk noise suppression increases. This is because, larger sized buffers have large parasitic capacitance values and thus their effective RC is too high. This makes them response slowly to the already slow varying crosstalk noise. Thus, it seems that the suppression by the higher buffer driver strengths is more.

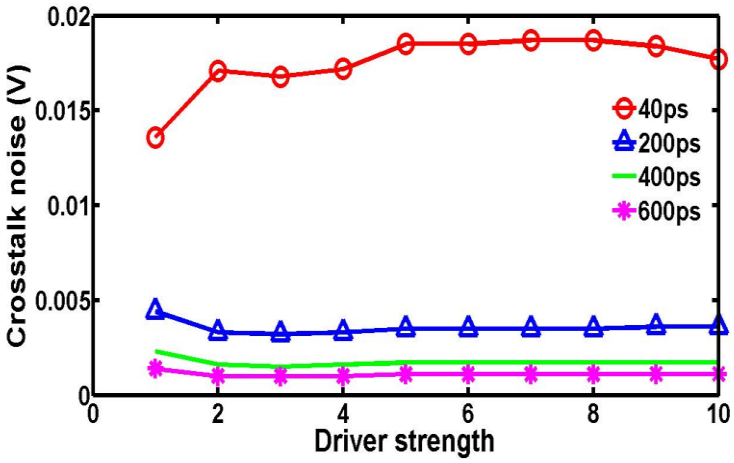

Fig. 4. Crosstalk noise voltage with varying crosstalk noise duration. The crosstalk noise amplitude is constant at 40% Vdd

2.2. Buffered global wire behaviour to crosstalk noise

In previous section, the input crosstalk noise was provided manually. This leaves out the provision of varying crosstalk noise which is generated due to coupling capacitance between the wires and the signal transmitted on the victim and the aggressor wires. The simulations done in this section is taken, to observe the worst case crosstalk effect as mentioned in [7-8]. Figure 5 shows the RC equivalent of a single aggressor and a victim wire. A single victim wire can have multiple aggressor wires. Thus, the effect of aggressor wire on the victim wire becomes an important phenomenon while taking into consideration the buffer driver strength impact on crosstalk noise.

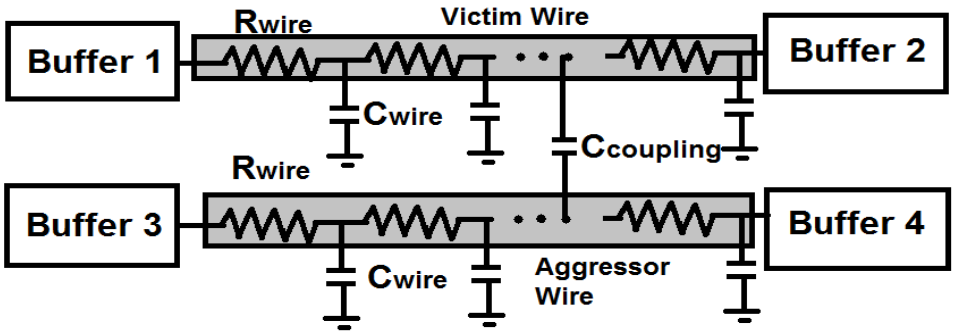

Fig. 5. RC equivalent of victim and aggressor wire showing coupling capacitance

The worst case coupling for maximum crosstalk noise effect on the buffer is taken with coupling capacitance near the receiver of the victim wire. Buffer 1 and buffer 2 is the transmitter and receiver buffer blocks of the aggressor and; buffer 3 and buffer 4 is the transmitter and receiver blocks of the victim wire. Since the crosstalk noise generated due to the coupling between the victim and the aggressor wires is to be suppressed by the victim receiver buffer driver, all the other buffer driver strengths are kept constant and only the victim buffer receiver driver strengths are changed to see the noise suppression effects. Figure 6 shows the crosstalk noise at the input and the output of the victim receiver buffer. From the plot we can observe that unlike the noise suppression trend for standalone buffer, the suppression trend for the wire setup in this section shows linear behaviour. It is also seen in figure 6 that the crosstalk noise at the input of the buffer of the victim also shows linear behaviour as the driver strength of the buffer is increased.

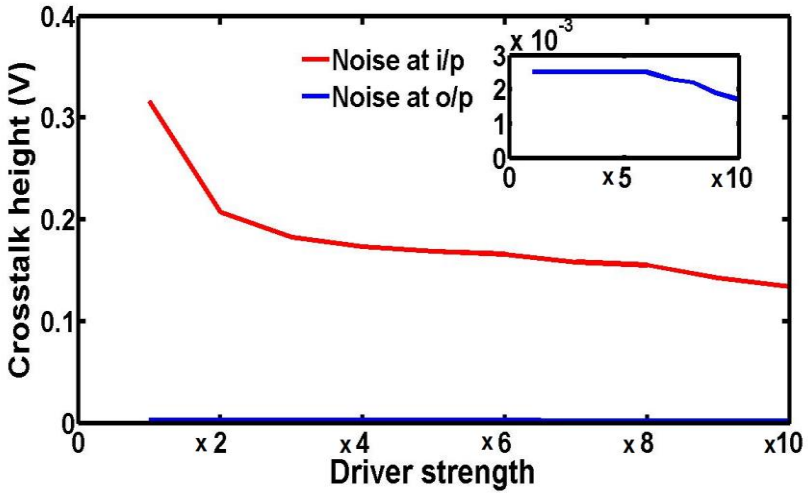

Fig. 6. Crosstalk noise at the input and the output of the victim wire buffer driver. Inset shows the trend in crosstalk noise as obtained at the output of the buffer

The linearity is due to the total resistance and capacitance contributed by the victim wire. For lower drive strengths, the capacitance value is very low but the resistance value is very high to make the total RC constant to be very high. Thus, it gives less amount of time to charge the output load capacitor resulting in suppressed bump height but larger delay at output. The linearity in this case is because of the RC of the wire. The capacitance offered by the wire provides higher capacitance for the voltage to be discharged till it reaches the receiver of the victim resulting in lower input values at the input and crosstalk noise considerably suppressed.

Figure 7 shows the crosstalk noise generation at the input of the buffer due to varying coupling capacitances and buffer drive strengths. It shows that as the buffer sizes increase, the increasing coupling capacitance will not drastically change the crosstalk noise as when the driver strengths are low. This effectively shows that the use of higher driver size is advantageous in case of circuits which are very sensitive to crosstalk noise.

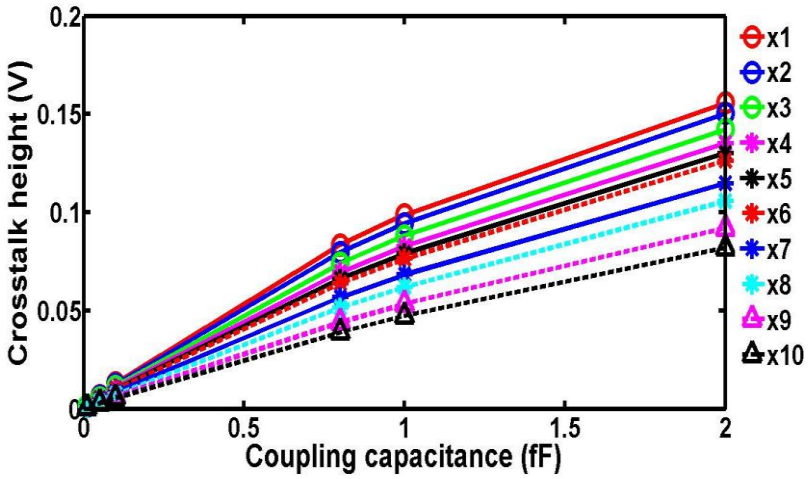

Fig. 7. Crosstalk noise generated due to varying coupling capacitances and buffer driver strengths

V. CONCLUSION

Driver strength used to drive the circuit greatly influences the suppression of crosstalk bump. Higher drive strengths though are capable of amplifying the noise bump, but their input load causes the previous stage to slow down, causing decrease in height of noise bump at input. The threshold voltage of transistors further brings down the bump height at output of cells. Thus higher drive strength drivers are better option to control noise propagation along the Noise path.

VI. FUTURE WORK

The parasitic effects associated with the technology node increases as we move to sub-nano meter technology. Therefore, the effect of understanding the importance of buffers added for static timing analysis in the chip is a significant task towards the optimization of the chip performance. In the near future, advanced driver designs and interconnects using emerging technologies [9,10] can help in further optimization of system-on-chip performance and modeling of on-chip interconnect noise for reducing the crosstalk.

REFERENCES

[1] Tianpie Zhang and Sachin S. Sapatnekar: 'Simultaneous Shield and Buffer Insertion for Crosstalk Noise Reduction in Global Routing', *IEEE Transactions on Very Large Scale Integration (VLSI Systems)*, Vol. 15. No. 6, June 2007 .

[2] S. K. Lee, S. H. Lee, D. Sylvester, D. Blaauw and J. Y. Sim, "A 95fJ/b current-mode transceiver for 10mm on-chip interconnect," *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, 2013, pp. 262-263.

[3] E. Mensink, et al., "A 0.28pJ/b 2Gb/s/ch transceiver in 90nm CMOS for 10mm on-chip interconnects," ISSCC Digest Tech. Papers, pp. 414-415, Feb. 2007

[4] D. Walter, et al., "A source-synchronous 90Gb/s capacitively driven serial onchip link over 6mm in 65nm CMOS," ISSCC Digest Tech. Paper, pp. 180-181, Feb. 2012

[5] K. Chun, et al., "A 667 MHz logic-compatible embedded DRAM featuring an asymmetric 2T gain cell for high speed on-die caches," IEEE J. Solid-State Circuits, vol. 47, no. 2, pp. 547-559, 2012

[6] L. Macchiarulo, E. Macii, M. Poncino: "Wire Placement for Crosstalk Energy Minimization", *Proceedings of the 2002 Design, Automation and Test in Europe Conference and Exhibition (DATE'02), 2002.*

[7] G. Kansal, A. Sharma, I. Raza, "Decreasing parasitic capacitance in IC layouts", *EDN Network Newsletter*, Jan 2014.

[8] C. J. Alpert, A. Devgan, S.T. Quay, "Buffer Insertion for Noise and Delay Optimization", *IEEE Trans. Computer Aided Design*, vol. 18 no.11, pp 1633-1645, 1999

[9] Mrigank Sharad, Kaushik Roy, "Spintronic Switches for Ultralow Energy On-Chip and Interchip Current-Mode Interconnects", *Electron Device Letters IEEE*, vol. 34, pp. 1068-1070, 2013, ISSN 0741-3106.

[10] Zubair Al Azim, Ankit Sharma, Kaushik Roy, "Buffered Spin-Torque Sensors for Minimizing Delay and Energy Consumption in Global Interconnects", *Magnetics Letters IEEE*, vol. 8, pp. 1-5, 2017, ISSN 1949-307X.

AUTHORS

Swatilekha Majumdar did her Masters in VLSI Technology from Indraprastha Institute of Information Technology, Delhi and did her internship at ST Microelectronics, India. She did her bachelors from Guru Gobind Singh Indraprastha University, Delhi and has been a member of IEEE and IEEE WIE since 2012. Her research interest are non-volatile memories, on-chip interconnects and analog design.

Jatinder Pal Singh Sahota did his bachelors from Punjab University in 2006 in Electronics and Communication Engineering. He worked at ST Microelectronics from 2007-2015. His research area includes ASIC Physical/Layout Design and Electrical/Electronic Manufacturing. He is currently doing his PG Diploma from University of Pune in Advanced Digital System Designs.