# DESIGN CRITERIA OF LDD MOSFET DEVICES

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## *ABSTRACT*

*In this paper we present the design criteria of Lightly Doped Drain (LDD) MOSFETs through the study of the influence of the n- doping of drain/source on the electric field, but taking into account also the impact of LDD on series resistance of the device and the channel length contribution on breakdown voltage reduction.*

## *KEYWORDS*

*MOSFET Devices, Drain Engineering, LDD MOSFET structure, TCAD Simulation.*

## I. INTRODUCTION

The silicon technology is the most important achievement in the history of modern electronic engineering. In order to consume less power, to occupy less space, to reduce costs and to obtain shorter propagation delays, many improvements have been made in the device integration process according to Moore law. The progress in the silicon fabrication technology has brought to the production of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) having sub-micrometer dimensions. However for these devices, to keep constant supply voltage, a high electric field is present near the active regions of the transistor, causing the well-known effect called *hot electrons effect*. These electrons enter in the oxide layer, accumulating over time. This accumulation degrades the device performances, producing a reduction of device lifetime and increasing the threshold voltage $V_T$ [1-3]. Moreover the MOSFET scaling produces also the *Short Channel Effects* (SCE). When SCE are present, we have a channel length modulation, due to the increase of depletion layer width in the drain area when the drain voltage increases: the channel becomes shorter, producing an increase of drain current. Moreover SCE produce a threshold voltage shift and sub-threshold voltage swing which cause difficulty to turn off device, and also the DIBL (Drain-Induced Barrier Lowering) effect [1-3].
It follows that to prevent the previous phenomenon it must act to the drain (*drain engineering*) where the high electric field locates (even if the used technological processes are also applied to the source for reasons of symmetry).
The most known structure used to reduce the electric field is the **Lightly Doped Drain** (**LDD**) structure [4-14], which has higher breakdown voltage, lower electric field near the source and drain regions, lower gate current, etc. that make it more suitable for sub-micrometer dimensions devices than conventional MOSFET. However there are some drawbacks [15]. One of the most important disadvantages is that of an increased resistance which degrades current capability of the device. In general, the gain in breakdown voltage is often accompanied by the degradation of the device [16]. This problem can be alleviated by properly designing the LDD architecture concerning doping concentration of both components and channel length. Since electrons in Si have a higher mobility than holes, n-channel devices are more negatively influenced by the effect of high electric field resulting in a greater number of hot-electrons injected into the gate oxide [11]. For this reason, we study a LDD structure for n- type MOSFETs.

In this paper we present the design criteria of LDD MOSFETs through the study of the influence of the n-doping of drain/source on the electric field, one of the most important issues of current technology, but taking into account also the impact of LDD on series resistance of the device and channel length contribution on breakdown voltage reduction when we consider drain/source light doping. In particular, through a simulation study, we have determined the optimal values of doping concentration in P-well and of channel length for which we have a sensible reduction of SCE.
The presentation of the paper is organized as follows. In Section II we present a brief review of LDD MOSFET structure. Section III is devoted to the analysis and discussion of simulation results in order to identify the technological parameters of LDD MOSFETs, which reduce the short channel effects. At last, the conclusions and future developments are described in Section IV.

## II. A BRIEF REVIEW OF LDD MOSFET STRUCTURE

In the Lightly Doped Drain technique (LDD), the drain region (and source) is formed with a first diffusion more extended of atoms at concentration N-, and then with a second diffusion at concentration N+ less extensive, but deeper. The effect is always to provide a gradual doping profile of the drain region (and source) so as to reduce the maximum electric field [1-3].
The reduction in electric-field intensity due to the LDD structure is illustrated in the two-dimensional simulation results reported in [4], where it is possible to see that the electric field in the conventional device peaks approximately at the metallurgical junction and drops quickly to zero in the drain because no field can exist in the highly conductive N+ region. On the other hand, the electric field in the LDD device extends across the N- region before dropping to zero at the drain. Since the areas under the two field curves are equal for a given voltage drop, the peak field in the LDD device, which determines the junction avalanche breakdown voltage, must be lower than in the conventional device.
In order to produce LDD MOSFET, three steps must be added to standard MOSFET production, as described in Fig. 1.

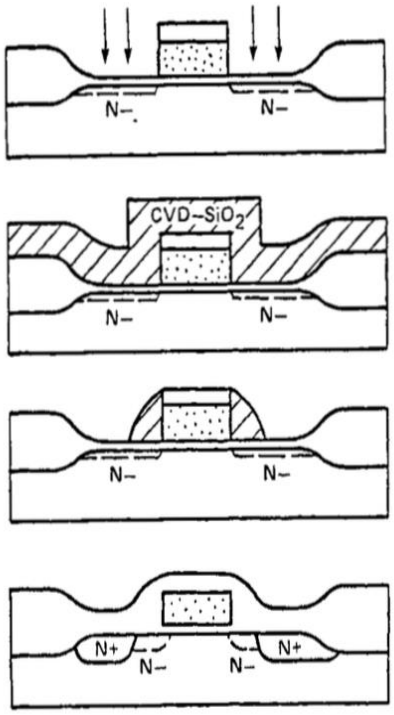


**Figure 1.** Schematic Process for LDD MOSFET Structure (*from [2]*).

After poly-silicon gate definition using Vertical Reactive Ion Etching (RIE), a little implant of N- is performed to form LDD regions. Then 450 nm of SiO2 is deposited with Chemical Vapor Deposition (CVD). Directional RIE is used to remove SiO2 leaving sidewall spacers which will act as a mask for the Source/Drain Implants. This process is followed by N+ implant to establish Source/Drain wells.

## III. ANALYSIS AND DISCUSSION OF DEVICE SIMULATIONS

The following simulations, obtained with SILVACO® TCAD Software, show the LDD MOSFET drain current trends for different channel doping doses and for different channel lengths.

The LDD MOSFET under investigation has been realized on Silicon substrate with <100> crystallographic orientation and a doping dose of phosphor atoms of $10^{14}$ $cm^{-3}$. The P-well region is obtained implanting a dose of $8 \cdot 10^{12}$ $cm^{-3}$ boron atoms with 100 KeV of energy. Source and drain regions are obtained with N+ arsenic implant of $5 \cdot 10^{15}$ $cm^{-3}$ concentration and 50 KeV energy with polysilicon gate as mask. LDD implants are made with a doping dose of phosphor atoms of $3 \cdot 10^{13}$ $cm^{-3}$.

### 3a) Simulations at a Fixed Channel Length (246 nm)

The first step is to determine the optimal doping concentration in the channel to have lower Short Channel Effects (SCE) in LDD MOSFET Structure.

The first simulation has been obtained considering a boron doping concentration in P-well equal to **$3 \cdot 10^{12}$ $cm^{-3}$**.

Fig. 2 shows the electric field, while Fig. 3 shows the $I_D$-$V_{DS}$ characteristic for three different gate voltages (i.e. $V_{GS}$ = 1.1V, 2.2V and 3.3V).

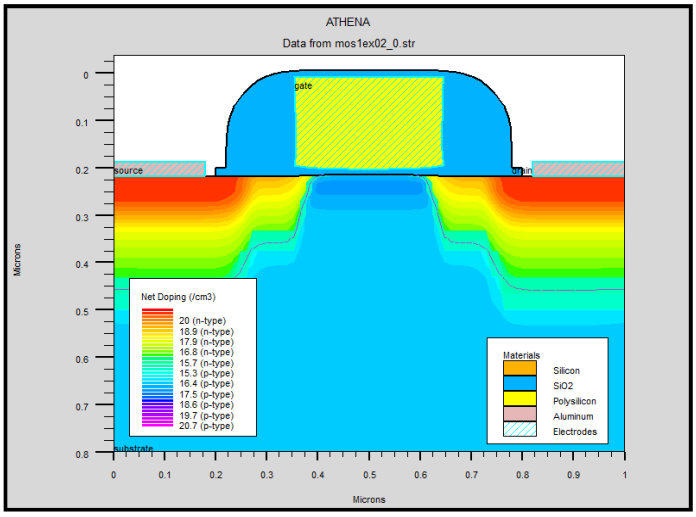


**Figure 2.** Electric field for LDD MOSFET structure with a boron doping concentration in P-well equal to $3 \cdot 10^{12}$ $cm^{-3}$.

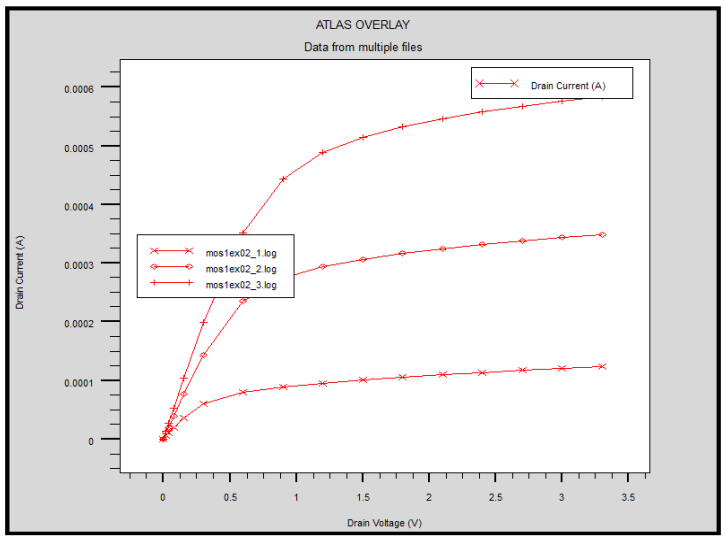


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**Figure 3.** $I_D$-$V_{DS}$ characteristic for $V_{GS}$ = 1.1V, 2.2V and 3.3V.

Similarly, Fig. 4 shows the electric field, while Fig. 5 the $I_D$-$V_{DS}$ characteristic for a boron doping concentration in P-well equal to $\mathbf{8 \cdot 10^{12}\ cm^{-3}}$.

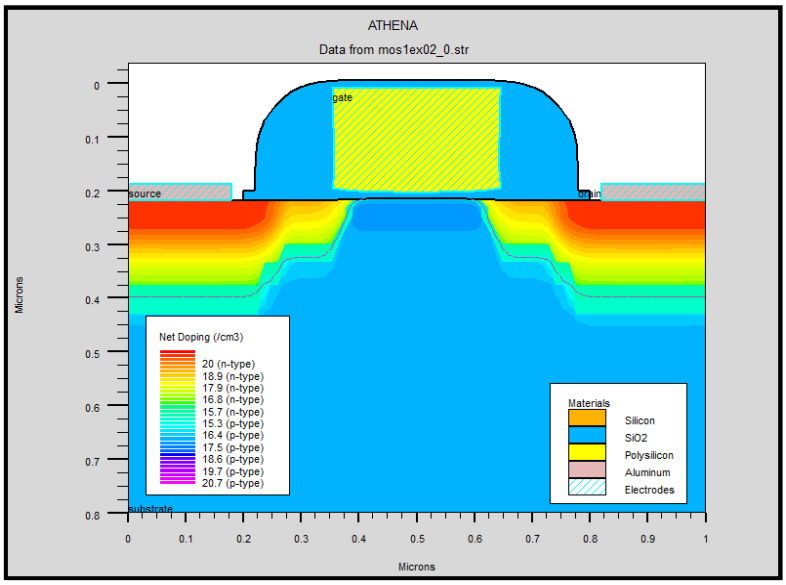


**Figure 4.** Electric field for LDD MOSFET structure with a boron doping concentration in P-well equal to $8 \cdot 10^{12}$ $cm^{-3}$.

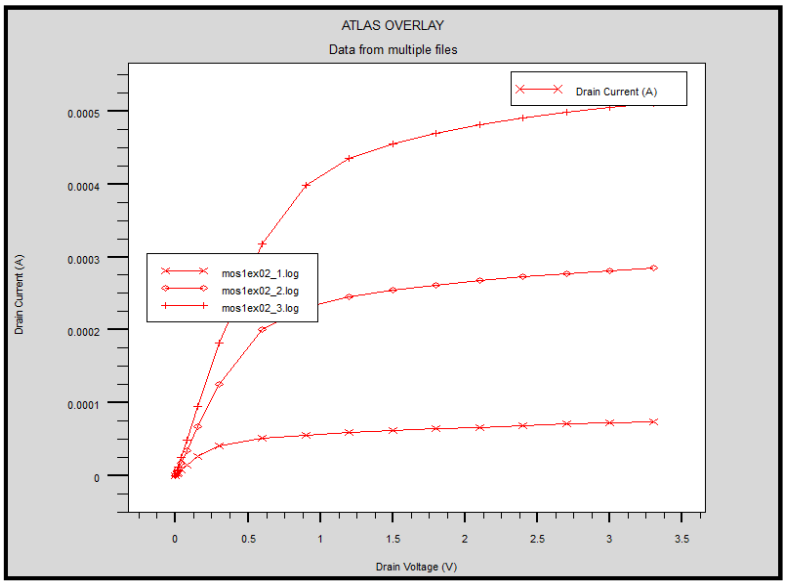


**Figure 5.** $I_D$-$V_{DS}$ characteristic for $V_{GS}$ = 1.1V, 2.2V and 3.3V (boron doping concentration equal to $8 \cdot 10^{12}$ $cm^{-3}$).

We have repeated the simulations considering a boron doping concentration equal to $\mathbf{2 \cdot 10^{13}\ cm^{-3}}$ and $\mathbf{3 \cdot 10^{13}\ cm^{-3}}$, and the relative results are reported in Figures 6, 7, 8 and 9 respectively

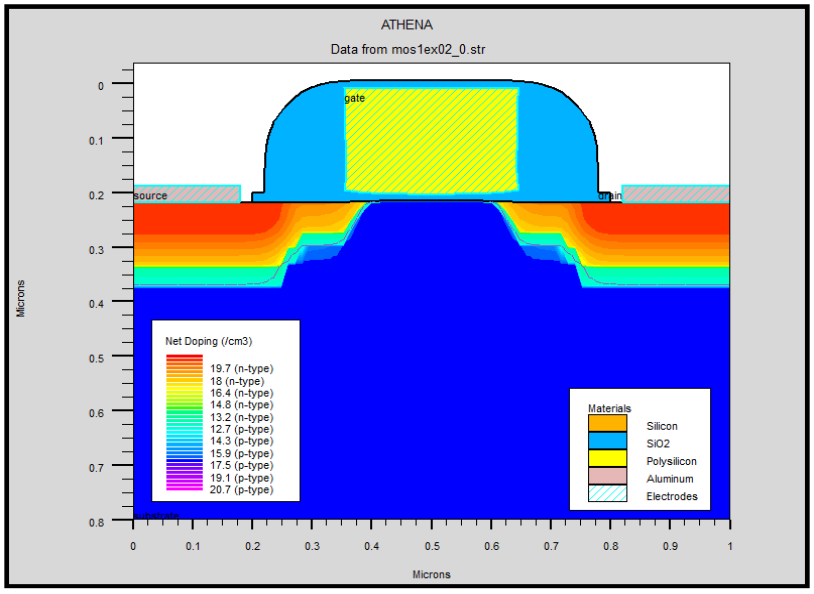


**Figure 6.** Electric field for LDD MOSFET structure with a boron doping concentration equal to $2 \cdot 10^{13}$ $cm^{-3}$.

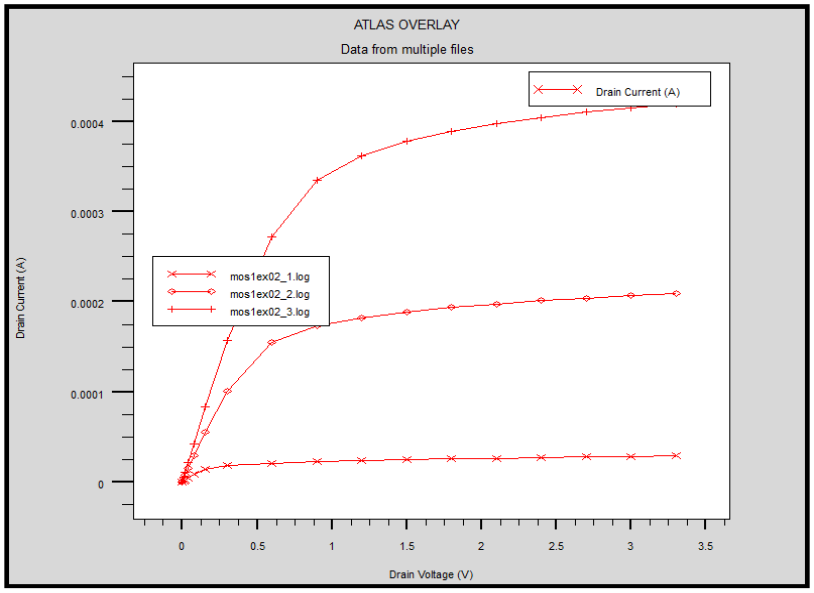


**Figure 7.** $I_D$-$V_{DS}$ characteristic for $V_{GS}$ = 1.1V, 2.2V and 3.3V (boron doping concentration equal to $2 \cdot 10^{13}$ $cm^{-3}$).

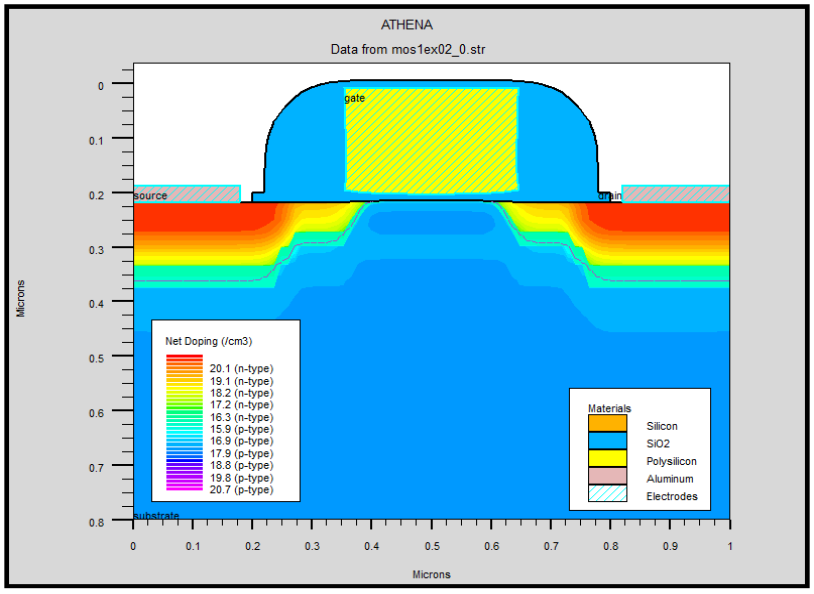


**Figure 8.** Electric field for LDD MOSFET structure with a boron doping concentration equal to $3 \cdot 10^{13}$ $cm^{-3}$.

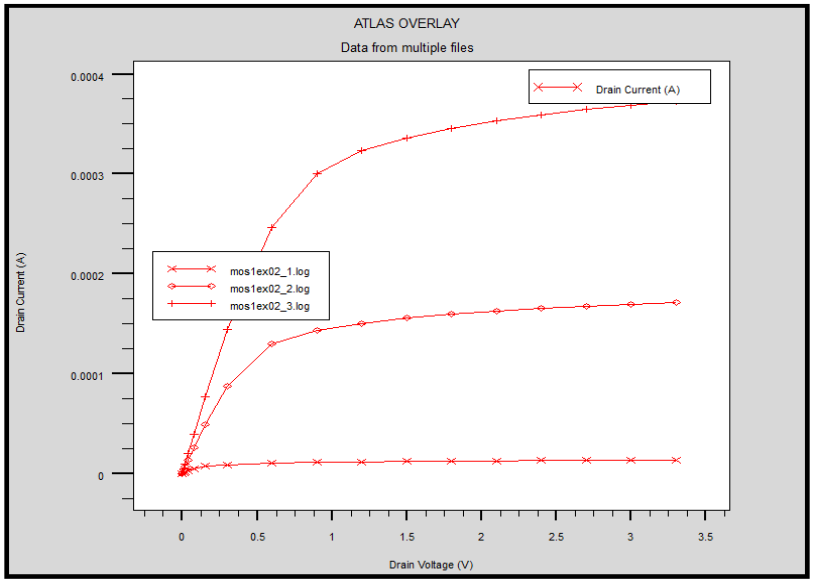


**Figure 9.** $I_D$-$V_{DS}$ characteristic for $V_{GS}$ = 1.1V, 2.2V and 3.3V (boron doping concentration equal to $3 \cdot 10^{13}$ $cm^{-3}$).

From the analysis of these figures we can affirm that with a boron doping concentration of $3 \cdot 10^{13}$ $cm^{-3}$ and for $V_{GS}$ = 1.1V, LDD MOSFET remains in OFF state. This effect is due to the increase of the threshold voltage [1-2]. For this reason it is not appropriate to go beyond this doping concentration. Moreover the trade-off between doping concentration and SCE is evidently for a boron doping concentration of $2 \cdot 10^{13}$ $cm^{-3}$, which results therefore the optimal value.
The second step is to determine the optimal channel length to have lower SCE.

### 3b) Simulations at a Fixed Doping Concentration ($2 \cdot 10^{13}$ $cm^{-3}$)

In order to not complicate the discussion, we only report the simulations results for channel lengths of 153 nm and 300 nm. Fig. 10 shows the electric field, while Fig. 11 shows the $I_D$-$V_{DS}$ characteristic for three different gate voltages (i.e. $V_{GS}$ = 1.1V, 2.2V and 3.3V), for a channel length of 153 nm.

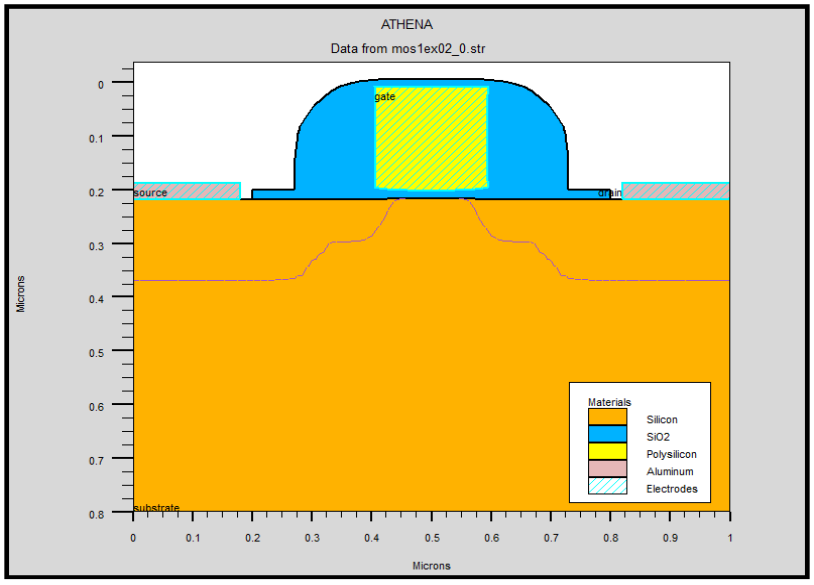


**Figure 10.** Electric field for LDD MOSFET having a channel length of 153 nm.

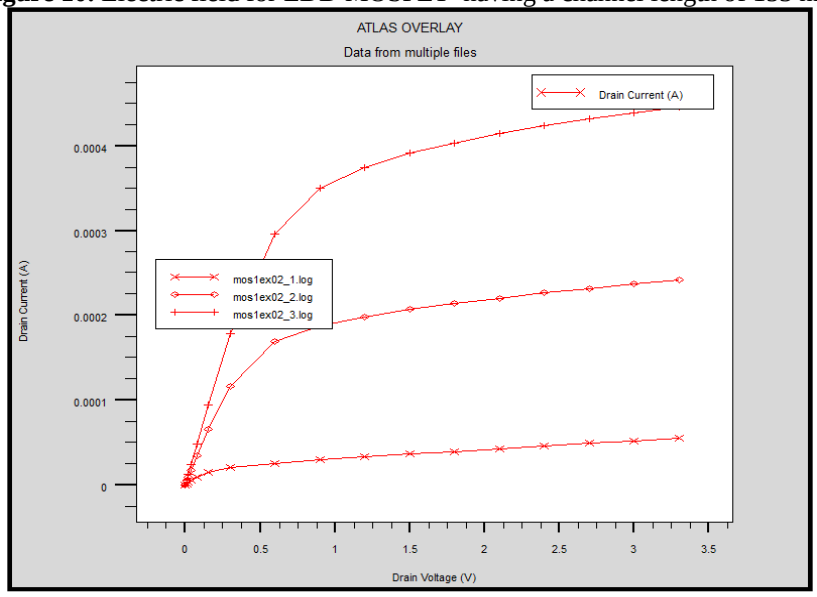


**Figure 11.** $I_D$-$V_{DS}$ characteristics for $V_{GS}$ = 1.1V, 2.2V, 3.3V (channel length of 153 nm).

Similarly, Figures 12 and 13 shows the electric field and the output characteristics for a channel length of 300 nm.

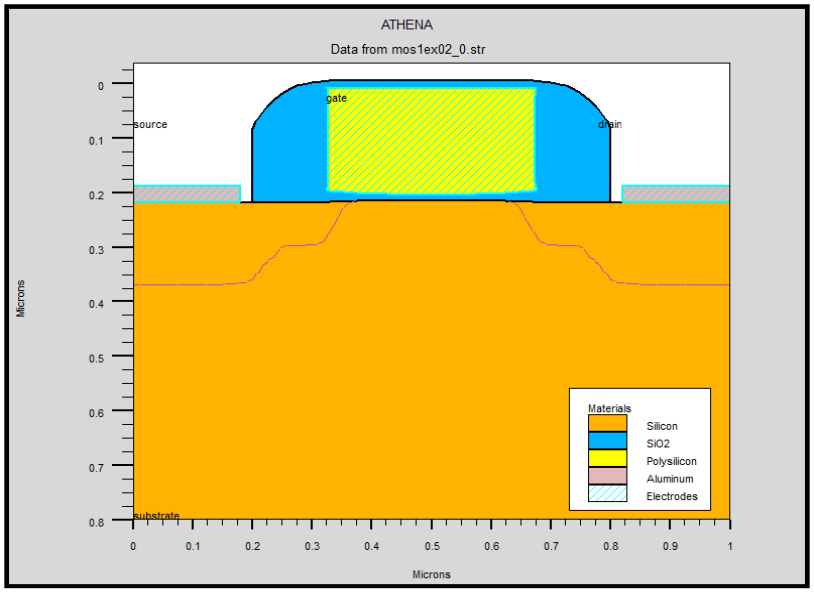


**Figure 12.** Electric field for LDD MOSFET having a channel length of 300 nm.

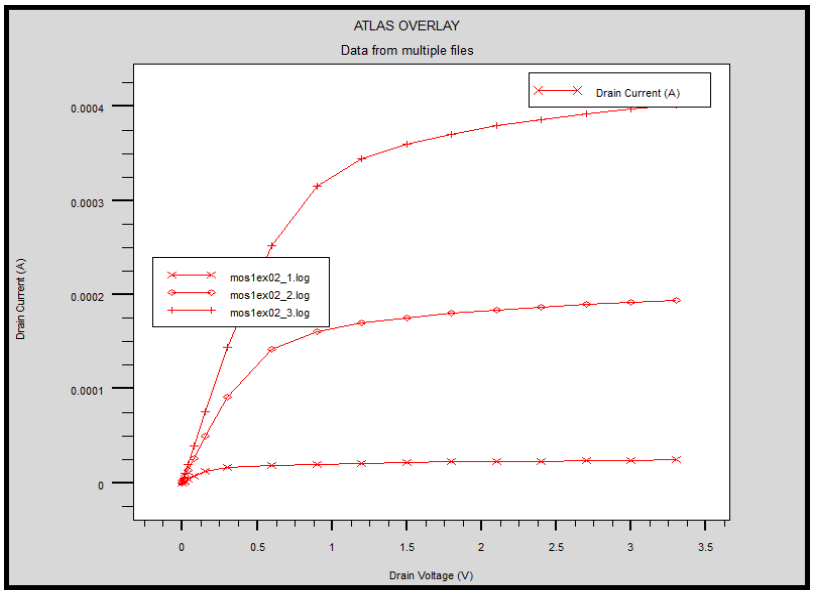


**Figure 13.** $I_D$-$V_{DS}$ characteristics for $V_{GS}$ = 1.1V, 2.2V, 3.3V (channel length of 300 nm).

In the light of the obtained results, in order to have SCE lower, 246 nm and 300 nm are the optimal channel lengths to be chosen. Evidently, for 300 nm, SCE effects are even lower but, on the other hand, device will be larger.

## IV. CONCLUSIONS AND FUTURE DEVELOPMENTS

Since miniaturization became an important issue in current technology process, the importance of lightly doped regions near drain and source increased.

In this paper we have studied the influence of the n- doping of drain/source on the electric field, one of the most important issues of current technology, but taking into account also the impact of LDD structure on series resistance of the device and the channel length contribution on breakdown voltage reduction when we consider drain/source light doping. In particular, through a simulation study, we have determined the optimal values of doping concentration in P-well and of channel length for which we have a sensible reduction of SCE.

Nowadays the continuous need to have littler and faster consumer devices such as laptops, smart-phones, cameras and so on, drive companies to develop smaller and smaller electronic components. Si technology almost reached its physical limits and a further scaling is practically impossible. A new kind of devices, known as CNTFETs (Carbon Nanotube Field Effect Transistors), seems to satisfy the market demand and the need to scaling all the electronic components (17-28).

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