AN EFFECTIVE PERFORMANCE OF COMBINATIONAL AND SEQUENTIAL LOGIC CELLS USING CURRENT SOURCE MODELING

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ABSTRACT

Current source model has become a good concern in logic cells. These standard cells must be presented for performing noise and delay analysis. Current source modeling is effectively considered for the traditional static timing analysis. The existing CSMs are only applicable for combinational logic cell. It is possible to handle any input waveform circuit and overcome the noisy inputs such crosstalk induced noisy waveforms. The proposed methods were implementing all logic cells. In this model output waveform can be computed even setup and hold times are violated. CSMs are differing from existing CSMs because of parasitic effects. It is implemented in both DC and AC analysis. Logic cells can take arbitrary shapes inputs like step and ramp signals but ramp signal only applied here. This arbitrary voltage waveforms with near-SPICE accuracy at speeds tens of thousands of times faster than other platform. In this paper described about the circuit parameters simulate in effective spice and determine the noise, time, delay waveforms with SPICE accuracy & it consider incorrect critical path and discontinuous delays during circuit optimization. It considers single dimensional with each iteration. We can able to compute the RMSE values from the SPICE and CSM voltage values. RMSE values calculated from the theoretical value of CSM & practical value of Spice voltage values. The proposed method computes the correct RMSE values from different logical circuits using CSM and compares their results. We can able to choose which circuit is better than other circuits from these circuit parameters measurements. So more number of circuits are possible to tested and we can easily identified logical errors from these circuits. Here applicationaly implemented ECG circuit and analyze these parameters also.

KEYWORDS: *Current source model (CSM), static timing analysis (STA), Performance verification, combinational and sequential logic cells.*

I. INTRODUCTION

The static timing analysis (STA) identified the signal transitions with arrival and transition times such saturated ramps. To check whether the circuit meets its timing goal. The required time for each circuit node is calculated by using backward propagation method. This signal pruning is a key to the linear run time of STA. In the initial backward traversal, we construct delay tables which record the required time at a node as a function of the transition time at that node.

This is followed by a forward traversal where signals are pruned not based on arrival times but based on slack. The proposed algorithm corrects the accuracy problems of the arrival time based pruning while at the same time maintaining the linear run time of STA. Since only a single arrival time is propagated for each node in the circuit, the linear run time of STA is preserved. We demonstrate that the proposed approach computes circuit delays that match those computed with an exact STA algorithm, while incurring only a modest run time increase over the traditional STA approach [2]. Slope propagation identifying the critical path of the circuit and posing a severe problem for circuit optimization methods. Two approaches are commonly used to verify the timing analysis. Dynamic simulation and static timing analysis. A demerit of dynamic simulation is that it requires the user to

generate a set of input vectors which exhaustively exercise all possible paths in a circuit. It has two fundamental assumptions.

First assumption is when calculating the delay of a gate, only one input of the gate is assumed to be switching at a time, ignoring the effects of simultaneous switching of a gate input signals.

Second assumption is given the single switching assumption, the signal arriving with the latest arrival time at a particular node is assumed to result in the longest path delay. Noise analysis has critical concern in advanced chip designs. Linear summation of the noise that is propagated through the driver of a net with the noise injected by capacitive coupled aggressor nets will significantly underestimate the actual noise on a net.

The majority of the cell models used in today's IC design flows consist of lookup tables or characteristic equations that on ramp (linear) voltage inputs and simplified loads and that create ramp output voltage waveform approximations [4]. Interconnect models are conjunction with more complex input voltage waveform representation. The first to present a real CS model (CSM) of a CMOS logic cell (called Blade) in which a pre-characterized current source is utilized to capture the non-linear behavior of the cell with respect to the input and output voltage values.

Effective current source model (ECSM) is the industry's first and only production-proven current source modeling standard for timing, power, noise, and variation. The ECSM and CCSM is the identical model. This highly accurate open-source model delivers accuracy to SPICE and is a critical component of today's advanced low-power and nanometer design flows. Other common models are only within particular values of SPICE. Spice model is very accurate model. The benefits of ECSM are given below.

• Ideal for advanced low-power designs – Supports advanced low-power techniques (state-retention power gating, dynamic voltage and frequency scaling, multi-supply multi-voltage)
• Provides accurate, holistic modeling of timing, power, noise, and variation.
  – Non-linear transistor behavior.
  – Receiver pin-cap modeling.
  – Time quantized Ceff.
  – Voltage impact on delay.
• Approved and maintained by Si2 as an open standard
  – Supported by several major library.

Recent advances in process technology scales the aspect ratio of wires to be taller and thinner to control wire resistance. A side effect of this scaling is that coupling capacitance between wires becomes the dominant portion of the total wire capacitance. The problem of delay calculation in the presence of crosstalk can be formulated as finding the worst-case delay among all possible alignments and aggressor waveforms. However, the computation of delay in the presence of noise is a challenging problem due to the following factors: (i) delay is sensitive to aggressor/victim alignment, (ii) linear model for a switching driver and effective capacitance principle may become inadequate and (iii) waveform becomes irregular in the presence of noise, making the conventional metric of delay measurement non-robust.

II. CS-COMBINATIONAL LOGIC CELL

We first deals with our CSM for combinational logic cells. This will become us to a traditional appreciation of our new sequential circuit elements. Various CSMs for logic cell is similar to that all output model of the logic cell with a voltage dependent current source. Analysis, a saturated ramp is applied to the input, while the output node is connected to a AC voltage source, and the input current is measured. Although the input capacitance, Ci, is a function of the input and output voltage values, in practice, an input-voltage-dependent Ci is all that can be efficiently utilized. This is because when calculating the output voltage waveform of a logic cell, the output voltage values of its fan out cells are unknown, and therefore, calculation of Ci values of the fan out cells cannot make use of any information about the output voltage levels of these fans out cells. In previous section described about the channeled noise.

2.1 Major participation of our work

- An effective accurate current source model for logic cell is presented.

- Current source modeling is address for all logic cells also. A main investigation is conducted for different circuit elements in logical cells and their effects on the output voltage waveform calculation process.
- Here we can calculate every node voltages and it produced net list also. The output of the cell can be predicted even when large circuits are presented.

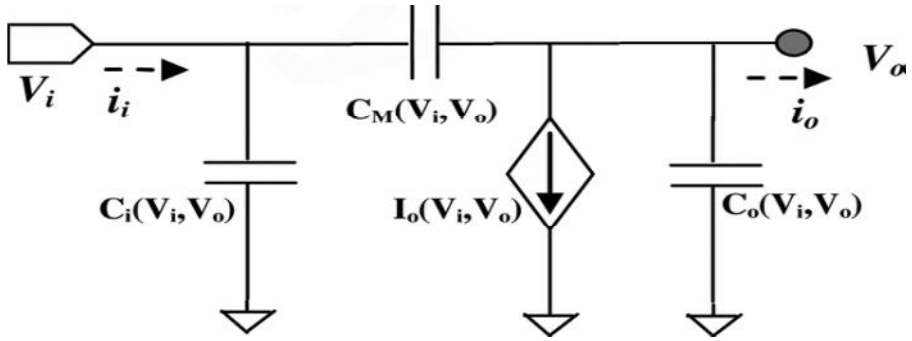

Figure 1. CSM for combinational logic cell

Fig.1, described to the three compressed nonlinear capacitances namely input and output parasitic capacitance Ci and Co to capture the capacitive loading at input and output nodes of the cell and a miller capacitance Cm, to capture the capacitive coupling effect between the input and output nodes. "(1)", is define the current source is characterized with DC analysis on the output while the output and miller capacitances are characterized by using KCL equation.

$$io + Io(Vi,Vo) + Co,Cm\frac{dvo}{dt} - Cm\frac{dvi}{dvt} = 0 \quad (1)$$

2.2 Pre characterized parameter values

Fig.2, shows the pre characterization step in CSMs for a given process/voltage/temperature corner involves two steps as mentioned before. First the DC current sourced by the gate is modeled as a function of active input pin and output pin voltages. In the second step, the parasitic behavior is modeled with a capacitance-based or charge-based model. In this work, we focus on CSMs. These circuits are controlled the voltage levels. We define easily so we get various parameters are get from the circuits. Channel1 and channel2 are dc voltage sources since output voltage and input voltage do not change because all derivative function becomes zero. (i.e.). "(2)", is used to calculate the input current for CSM.

$$i0 + Io(Vi,Vo) = 0 \quad (2)$$

Unknown parameter for each VCH1 of the ramp and VCH2 of the output dc voltage source. Already characterized Cm values. The parasitic capacitances at the input as follows, "(3)", define the input capacitance.

$$Ci = Io - Cm \quad (3)$$

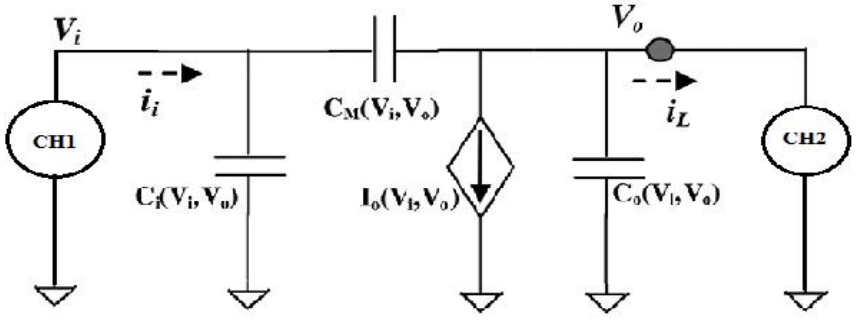

Figure.2 Characterization step for a combinational logic cell

Here Ci is characterized a ac source is connected to VCH2, when saturated ramp drives VCH1 resulting in, "(4)", define the output capacitance.

$$Co = -io - Io - Cm \tag{4}$$

In our model Co and CM are dependent only on the input and output voltages. Therefore, according to this model, the slew of the ramp signal waveforms used in the transient analysis should not affect CM(Vi,Vo) and Co(Vi,Vo) values. However, in (3) for example, the dVi/dt term represents the slope of the ramp signal applied to VCH1, which may assume different values. If we change the input slew, the measured io value (for the same level of Vi and Vo) will also change.
For modeling the transient, we show that a simple parasitic capacitance model with a time shift parameter is sufficiently accurate. Second we propose a solution for fast and accurate run time waveform analysis utilizing the CSM. We calibrate two capacitance values each for rise and fall transitions. For a given gate for a rise/fall transition, we calibrate the capacitance parameters for minimum error across a set of input slew rate and output load capacitance combinations. The maximum output load capacitance is such that the output slew does not exceed 8 for any input slew.

2.3 Output voltage calculation

Our CSM model benefit is using any type of load model. KCL at the output node voltage results in the following equation. "(5)", use the output voltage equation for CSM.

$$Vo = io + Io + Ci + cm \tag{5}$$

III. PROPOSED MODELING TECHNIQUE

In sequential cell construct three modes. Transparent, hold, transition**.** The proposed method can also capture complex sequential cells such as bare-input latches. A latch schematic and the corresponding simulation waveforms near setup time condition when the falling clock edge arrives close to data. This situation is simulated quite frequently in setup time characterization or transistor-level timing flows to determine the setup time to obtain margins. It is essential to capture all the complex nonlinear behavior of the circuit for correct analysis. The new model is able to match accurate device-level analysis for the shown latch. Hence it is possible to take advantage of faster macro model analysis during setup and hold time calculation in a timing or characterization flow instead of using device-level simulations on large fully extracted net lists of the sequential cells.

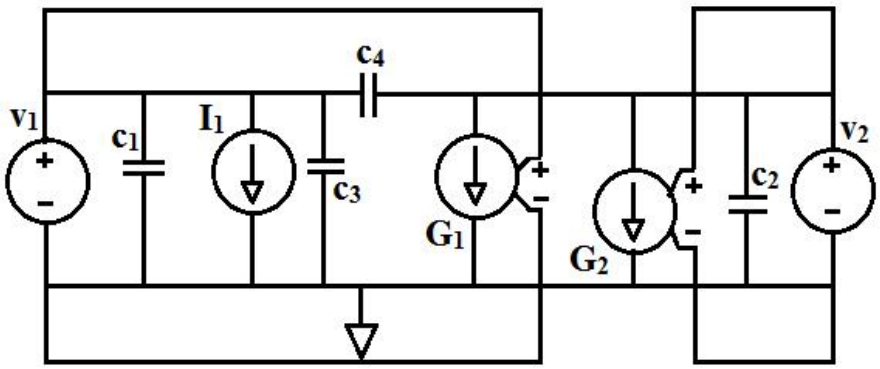

Figure.3 Logic cell using CSM

Fig.3, shows the proposed logic cell using CSM. It can be possible to connect the CSM for the inverter and transmission gates in series. Voltage dependent CS, which is dependent on the voltage value. This is how the model captures the effect of input node voltage.
In "Fig4", shown the logic cell is the mode based analysis. This mode exists we can able to get the every node voltage each devices can produce respective voltages. Here feedback loop is closed and the two cross coupled inverters are connected back to back in the transition mode. In transition mode current will be zero otherwise it will be equal to the output current of the feedback inverter. In this

case transmission gate is conducting so CSM should be good appreciation of the transparent mode. Here we can obtain every node voltage, current and frequency.

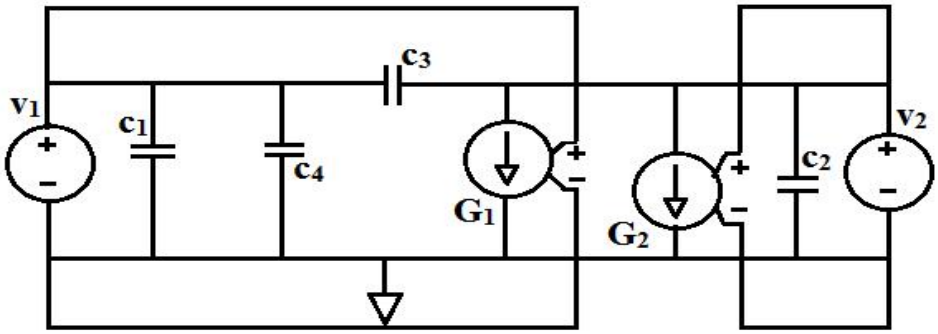

Figure.4 CSM of Logic cell

3.1 Pre characterized values

The logic cell characterization steps of the model are load-independent, because the model components are characterized as a function of the input, output and internal node voltage values rather than the input slew and output effective capacitance. Therefore the output voltage waveform can be constructed for a given input voltage waveform in the presence of an arbitrary load. Note that the current drawn by the load can always be written as a function of the output voltage of the logic cell and the load components. Using this current component for the load, a KCL equation at the cell output node can be written, which is a function of the cell output and input voltages, the pre-characterized cell components, and the load electrical parameters. Derivative terms become zero because channel1and channel2 is DC sources. (6)", shows input current equation for the sequential cell.

$$iq + iq_{\_bar(Vi,Vo)} = 0 \quad (6)$$

So a miller capacitance value is zero.

3.2 Output voltage

The internal node effect is smaller when the fan out load is significantly larger than the diffusion capacitances of the driver cell. This is due to the fact that whether or not some additional output current is needed to charge the internal capacitances becomes less significant when the output current is large. The complete CSM can be used selectively for different logic cells based on the output load. Using this selective modeling, one can use the simple CSM of the logic cells that drive a relatively large load. Otherwise, the complete CSM used. In sequential cell load model is applied and this load has independent model given input is the ramp input signal. The following KCL equations are used to calculate the output voltage. "(7)" shows the output voltage of the sequential cell.

$$Vq = iq_{\_bar} + Iq_{\_bar} + Cq + Cm \quad (7)$$

3.3 Applications

Our CSM were implementing to the combinational and sequential cell models these modeling are used to the ECG circuit. Because we computing different voltage and current levels in various nodes and electronic devices with SPICE accuracy.

Programmable gain	1,100,200,500,1000
CMRR	130db
Gain bandwidth	25MHz
Input offset	25µv

"Fig.5", shown the constant ECG circuit. This implementation is very useful for various levels of current and voltage in entire circuit. In previous more combinational circuits were implemented. We can possible to implement any of the circuit and get different voltages for these respective circuits.

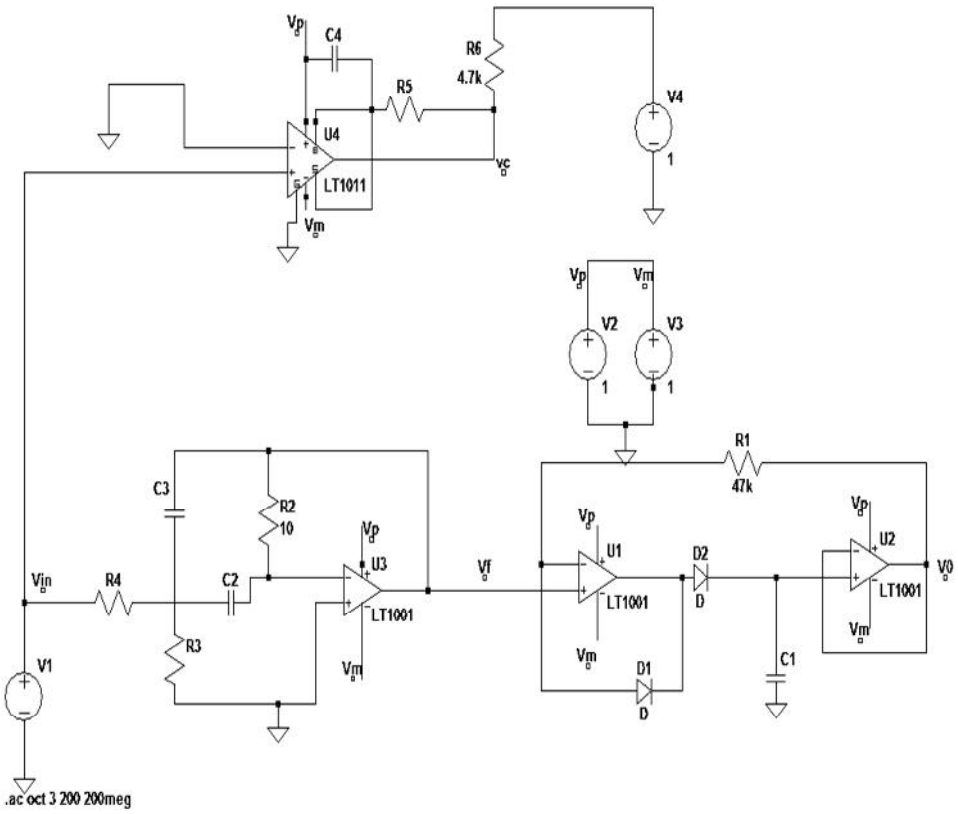

Figure.5 ECG Circuit with Spice

3.4. Experimental results

Our CSM simulator was implemented using 'c' language in LINUX operating system. Logical circuits were simulated in LT-spice here we can get every node voltage levels and it produced net list also. These net list is given to the input of H-spice here we can identified various parameter values in different circuits.

3.4.1 CSM for combinational cells evaluation

The effectiveness of our CSM for combinational logic cells. It deals with HSPICE waveforms of arbitrary shapes. RMSE values shows the noise injection of the logical circuits whether it have minimum or maximum. The shape of the waveform greatly impacts the accuracy of timing analysis; therefore, delay and output slew metrics may not be sufficient to construct shape of the waveform. Our model is able to compute close-to- SPICE output waveforms in terms of their actual shape. "(8)" shows the Root Mean Squared Error (RMSE) as a metric to compare waveform similarities. RMSE is defined as:

$$RMSE = \sqrt{VSPICE - VCSM} \quad (8)$$

Where Vspice and Vcsm are the voltage values of the output of the logic cell at a given time. To generate different noisy waveforms for this experiment.

3.4.2 CSM for proposed logic cell evaluation

Similarly to what we did for the combinational cell models. We calculate the RMSE for the latch model to measure its waveform similarity to Hspice. Latches and registers are basic building blocks in synchronous circuit design; in essence, they are circuits where a clock edge is used to sample and store a logic value on a data line . The setup time is the minimum time before the active edge of the clock that the input data line must be valid for reliable latching. Similarly, the hold time represents the

minimum time that the data input must be held stable after the active clock edge. The active clock edge is the transition edge (either low-to-high or high-to-low) at which data transfer/latching occurs.

TABLE 1 VARIES PARAMETERS ARE OBTAINED FROM DIFFERENT CIRCUIT

180nm				
Circuits	**Power Dissipation**	**Total memory used**	**CPU time**	**Voltage**
Logic cell1	50mw	24kB	0.27s	5v
Logic cell2	360mw	24kB	0.28s	4v
ECG	0-125mw	25kB	0.30s	2.5v

TABLE II RMSE VALUE COMPARISON WITH SPICE FOR SEQUENTIAL CELL

LIBRARY	**CELL**	**RMSE**
180nm	Cell1	2.2360
	Cell2	2.0000
	ECG	1.5811

Table I shows the various parameters for some of these cases in 180nm library. These values which confirms that our voltage waveform closely matches that produced by HSPICE.

Table II Shows the normalized RMSE for Same cases in 180nm library. It obtained from Hspice voltage and Theoretical value of CSM. In these two tables shown the overall noise injection and error values from the logical circuits because we can implement the any of the circuits if it is accurate parameters.

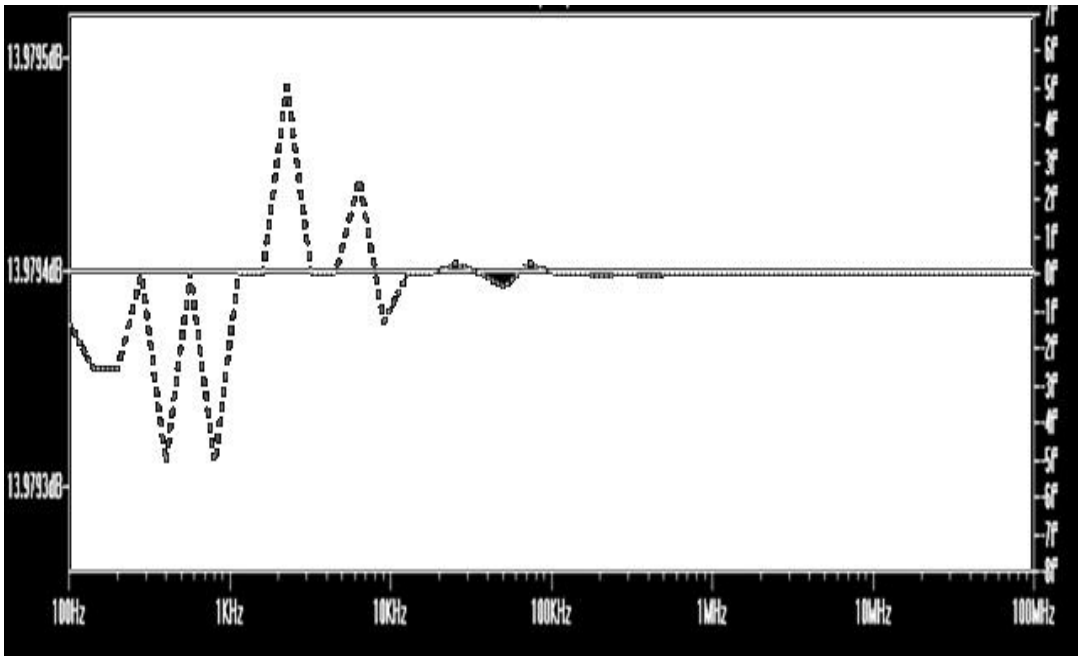

Figure.6 Output waveform for logic circuit1 using CSM

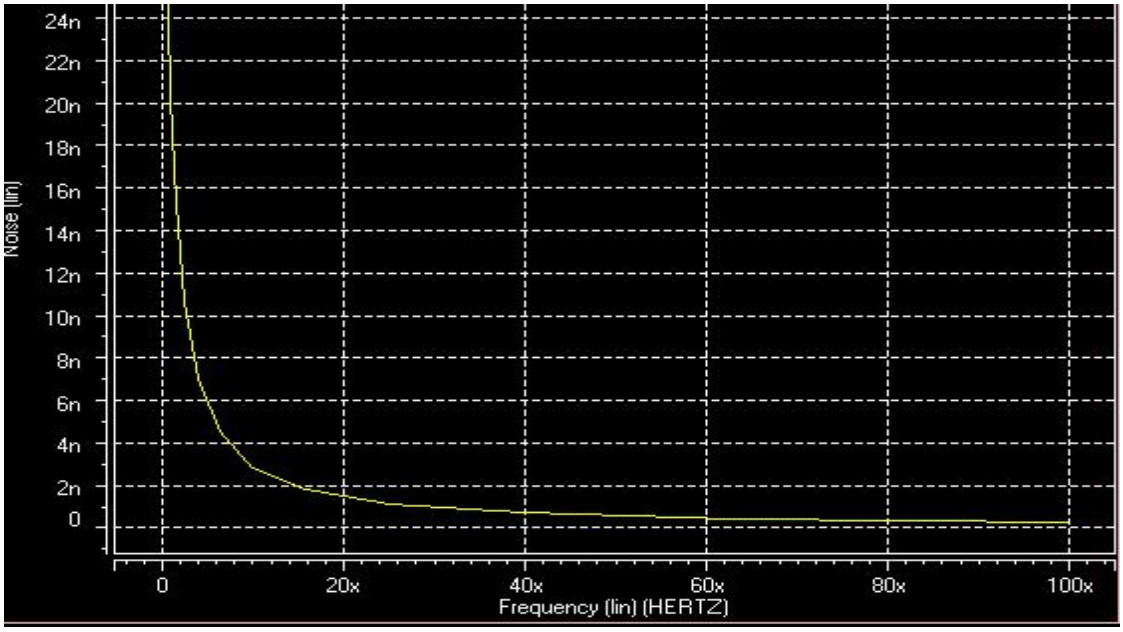

Figure.7 noise waveform for the ECG circuit with SPICE

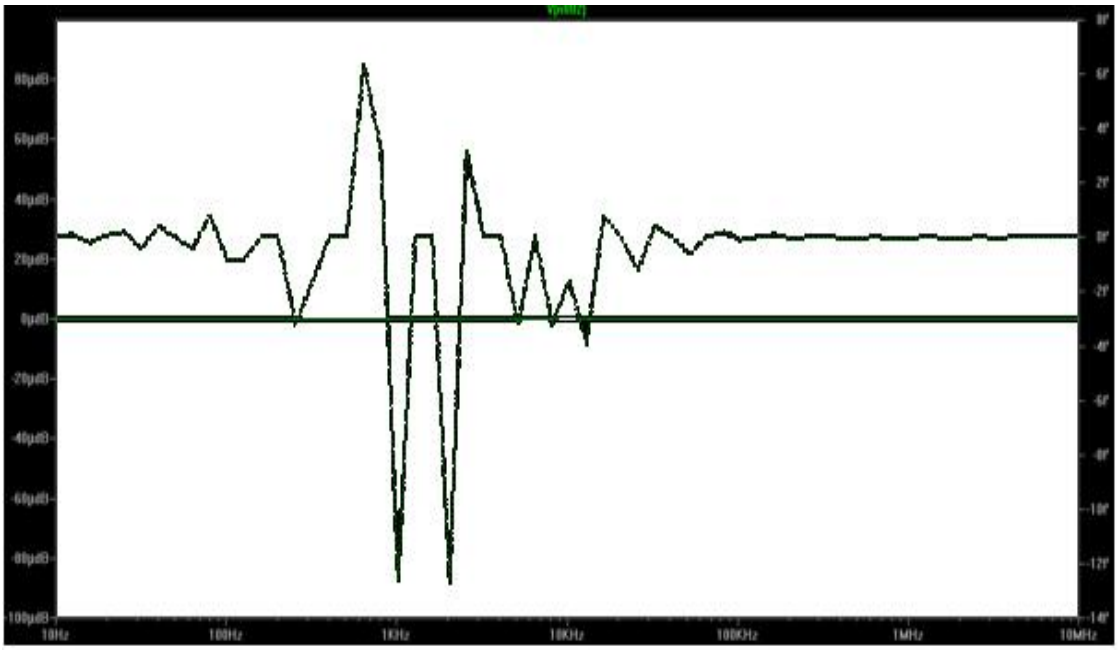

Figure.8 output waveform for logic circuit2

IV. CONCLUSION

In this paper we presented an accurate current source model for logic cell. Our proposed technique is compute RMSE values from Spice voltage and CSM voltage. We showed that the accuracy of our proposed technique is computing the output voltage waveform of the Logic cells. Given the input and clock voltage waveforms of arbitrary shapes, our model can accurately compute the output voltage waveform of register cell, and hence the timing and noise parameters associated with the cell. Modeling requirements for accurate analysis of nanometer designs are growing faster than the ability to create models using the traditional characterization process. Together these innovative models set a new standard foe cell and interconnect timing analysis. It has been demonstrated that the minimum timing and noise of our model. Cells differ from one another in the way that they respond to voltage waveforms that include distortions due to noise. Results for our CSM sequential cell model HSPICE waveforms with significant runtime speedup. We can use different technologies without presence of

noise. This noise rejection filter conditions the input signal to correct for the lost noise immunity model.

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