HARMONIC REDUCTION IN CASCADED MULTILEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES USING GENETIC ALGORITHMS

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ABSTRACT

In this paper, a new topology of cascaded multilevel inverter using a reduced number of switches is proposed. The new topology has the advantage of reduced number devices compared to traditional configurations and can be extended to any number of levels. This topology results in reduction of installation area, cost, computational time and has simplicity of control system. This structure consists of series connected sub-multilevel inverter blocks. The GA technique finds the optimal solution set of switching angles, if it exits, for each required harmonic profile. Both simulation results and experimental verification of the proposed inverter topology for different number of levels and different harmonic profiles are presented.

KEYWORDS: *Multilevel inverter, Cascaded multilevel inverter, H –bridge, Full-bridge, Sub-multilevel inverter, Selective harmonic elimination, Programmed PWM, Genetic algorithms.*

I. INTRODUCTION

A Multilevel inverter is a power electronic system that synthesizes a desired output voltage from several DC voltages as inputs. The concept of utilizing multiple small voltage levels to perform power conversion was presented by a MIT researcher [1,2]. Advantages of this approach include good power quality, good electro-magnetic compatibility, low switching losses and high voltage capability. The first introduced topology is the series H-bridge design [1]. This was followed by the diode-clamped inverter [2–4] which utilizes a bank of series capacitors to split the dc bus voltage. The flying-capacitor (or capacitor clamped) [5] topology uses floating capacitors to clamp the voltage levels. Another multilevel design, involves parallel connection of inverter phases through interphase reactors [6].

One particular disadvantage of multilevel inverter is the great number of power semi-conductor switches needed. So, in practical implementation, reducing the number of switches and gate driver circuits is very important.

Genetic algorithms (GAs) are stochastic optimization techniques. Genetic Algorithms are applied in this to compute the switching angles in a cascaded multilevel inverter to produce the required fundamental voltage while, at the same time, 3rd and 5^{th} harmonics are reduced. It is shown in [7–9] that the problem of harmonic elimination is converted into an optimization task using binary coded genetic algorithms (GA).Various components of GAs such as chromosomes, fitness function, reproduction, crossover and mutation are illustrated as applied to the present work.

II. CONVENTIONAL CASCADED MULTILEVEL INVERTER

The cascaded multilevel inverter consists of series connections of n full bridge topology fig.1shows the configuration of cascaded multilevel inverter.

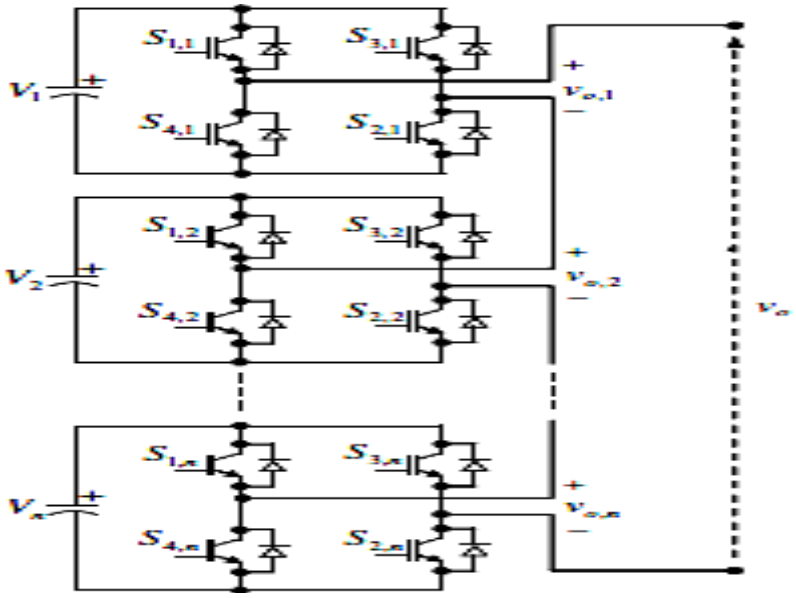

Fig. 1. Configuration of cascaded multilevel inverter

III. SUGGESTED TOPOLOGY

Fig. 2 shows the suggested basic unit for a sub-multilevel inverter. This consists of a capacitor (with dc voltage equal to Vdc) with two switches S1 and S2. Table 1 indicates the values of Vo for states of switches S1 and S2. It is clear that both switches S1 and S2 cannot be on simultaneously because a short circuit across the voltage Vdc would be produced. It is noted that two values can be achieved for Vo.

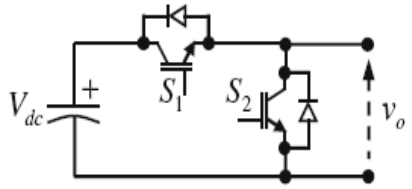

Fig. 2. Suggested basic unit for a sub-multilevel inverter.

Table 1
Values of v_o for states of switches S_1 and S_2.

State	Switches states		v_o
	S_1	S_2	
1	On	Off	V_{dc}
2	Off	On	0

The basic unit shown in Fig. 2 can be cascaded as shown in Fig. 3.

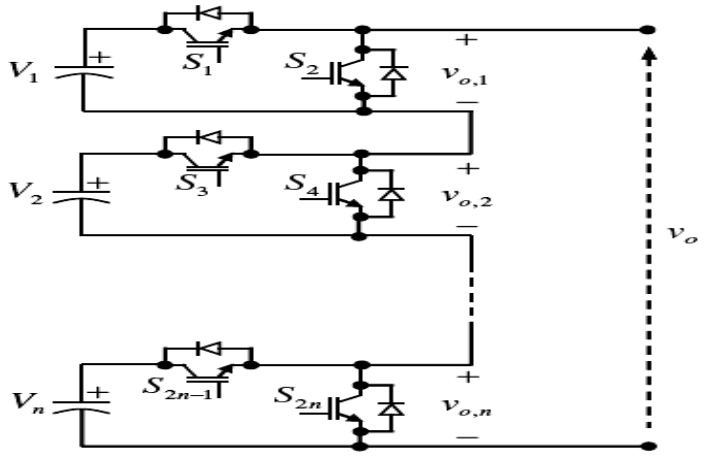

Fig. 3. Cascaded basic unit

Table 2
Values of v_o for state of switches.

State	Switches states							v_0
	S_1	S_2	S_3	S_4	⋯	S_{2n-1}	S_{2n}	
1	Off	On	Off	On	⋯	Off	On	0
2	On	Off	Off	On	⋯	Off	On	v_1
3	Off	On	On	Off	⋯	Off	On	v_2
4	On	Off	On	Off	⋯	Off	On	$V_1 + V_2$
⋮	⋮	⋮	⋮	⋮	⋯	⋮	⋮	⋮
2^n	On	Off	On	Off	⋯	On	Off	$\sum_{i=1}^{n} v_1$

The output voltage of conventional multilevel inverter for all times has zero or positive value. In the following, we propose a new method for determination of magnitudes of dc voltage sources which are used in the proposed multilevel inverter.

The number of maximum output voltage steps of the n series basic units can be evaluated by,

$$Nstep=n+1$$

The maximum output voltage is given by,

$$Vo,max=n*Vdc$$

IV. EXTENDED STRUCTURE

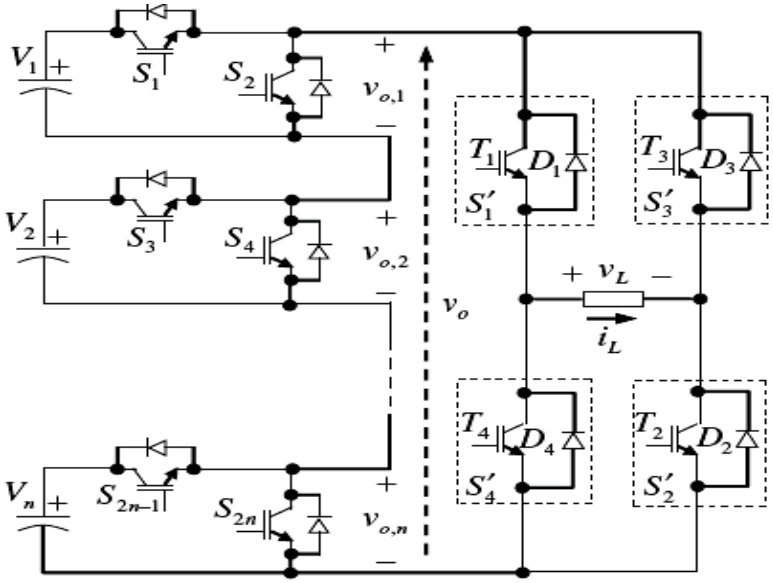

Fig 4. The proposed structure for generating both positive and negative voltages

Table 3
Switches states for a full-bridge.

State	Switches states				v_L	Components conducting
	S'_1	S'_2	S'_3	S'_4		
1	On	On	Off	Off	v_o	T_1 and T_2 if $i_L > 0$ D_1 and D_2 if $i_L < 0$
2	Off	Off	On	On	$-v_o$	D_3 and D_4 if $i_L > 0$ T_3 and T_4 if $i_L < 0$
3	On	Off	On	Off	0	T_1 and D_3 if $i_L > 0$ D_1 and T_3 if $i_L < 0$
4	Off	On	Off	On	0	D_4 and T_2 if $i_L > 0$ T_4 and D_2 if $i_L < 0$

V. COMPARISON OF THE SUGGESTED STRUCTURE WITH THE CONVENTIONAL MULTILEVEL INVERTER

Table 4
Comparison of power component requirements among conventional cascaded multilevel inverters.

	Symmetrical	Symmetrical	
		Binary	Trinary
Maximum output voltage	$V_{dc}\left(\frac{N_{step}-1}{2}\right)$	$V_{dc}\left(\frac{N_{step}-1}{2}\right)$	$V_{dc}\left(\frac{N_{step}-1}{2}\right)$
Number of switches, IGBTs and gate drivers	$2(N_{step}-1)$	$4\left[\frac{\ln(N_{step}+1)}{\ln 2}-1\right]$	$\frac{4\ln N_{step}}{\ln 3}$
Number of capacitors	$\frac{N_{step}-1}{2}$	$\frac{\ln(N_{step}+1)}{\ln 2}-1$	$\frac{\ln N_{step}}{\ln 3}$
Variety of magnitudes of dc voltage sources	1	$\frac{\ln(N_{step}+1)}{\ln 2}-1$	$\frac{\ln N_{step}}{\ln 3}$
Standing voltage	$2V_{dc}(N_{step}-1)$	$2V_{dc}(N_{step}-1)$	$2V_{dc}(N_{step}-1)$

Table 5
Comparison of power component requirements for suggested multilevel inverter.

	First method	Second method	Third method
Maximum output voltage	$V_{dc}\left(\frac{N_{step}-1}{2}\right)$	$V_{dc}\left(\frac{N_{step}-1}{2}\right)$	$V_{dc}\left(\frac{N_{step}-1}{2}\right)$
Number of switches, IGBTs and gate drivers	$N_{step}+3$	$\frac{2\ln[2(N_{step}+1)]}{\ln 2}$	$\frac{N_{step}+9}{2}$
Number of capacitors	$\frac{N_{step}-1}{2}$	$\frac{\ln(N_{step}+1)}{\ln 2}-1$	$\frac{N_{step}+1}{4}$
Variety of magnitudes of dc voltage sources	1	$\frac{\ln(N_{step}+1)}{\ln 2}-1$	2
Standing voltage on S_1–S_{2n}	$V_{dc}(N_{step}-1)$	$V_{dc}(N_{step}-1)$	$V_{dc}(N_{step}-1)$
Standing voltage on S'_1—S'_4	$2V_{dc}(N_{step}-1)$	$2V_{dc}(N_{step}-1)$	$2V_{dc}(N_{step}-1)$
Standing voltage on all of the switches	$3V_{dc}(N_{step}-1)$	$3V_{dc}(N_{step}-1)$	$3V_{dc}(N_{step}-1)$

Tables 4 and 5 compare the power component requirements among the conventional and suggested multilevel inverters for the same number of the output voltage steps, respectively.

VI. SIMULATION DIAGRAM OF 11-LEVEL (CONVENTIONAL) CASCADED MULTILEVEL INVERTER

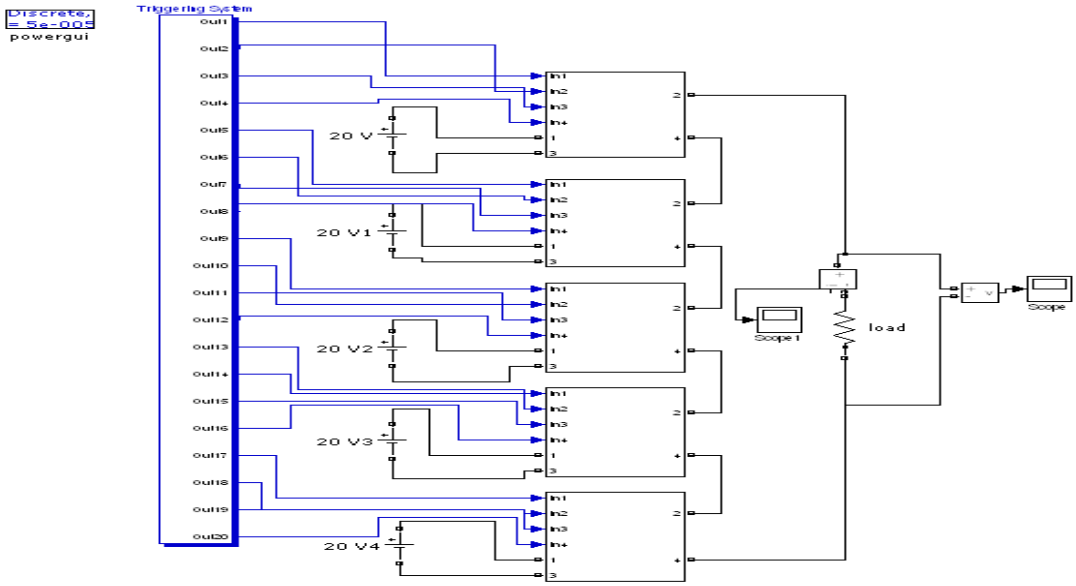

Fig 5. 11-level Cascaded Multilevel inverter(Cascaded)

Table 5: Switching sequence for Conventional topology

	S1	S2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1.	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2.	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
3.	1	0	0	1	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1
4.	1	0	0	1	1	0	0	1	1	0	0	1	0	0	1	1	0	0	1	1
5.	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	0	0	1	1
6.	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
7.	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	0	0	1	1
8.	1	0	0	1	1	0	0	1	1	0	0	1	0	0	1	1	0	0	1	1
9.	1	0	0	1	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1
10.	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
11.	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12.	0	1	1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
13.	0	1	1	0	0	1	1	0	0	0	1	1	0	0	1	1	0	0	1	1
14.	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	1	0	0	1	1
15.	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	1
16.	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
17.	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	1
18.	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	1	0	0	1	1
19.	0	1	1	0	0	1	1	0	0	0	1	1	0	0	1	1	0	0	1	1
20.	0	1	1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

VII. OUTPUT WAVEFORMS (CONVENTIONAL)

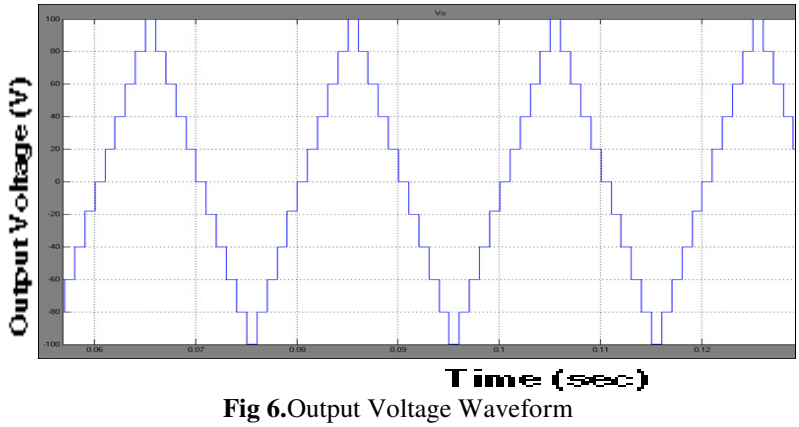

Fig 6. Output Voltage Waveform

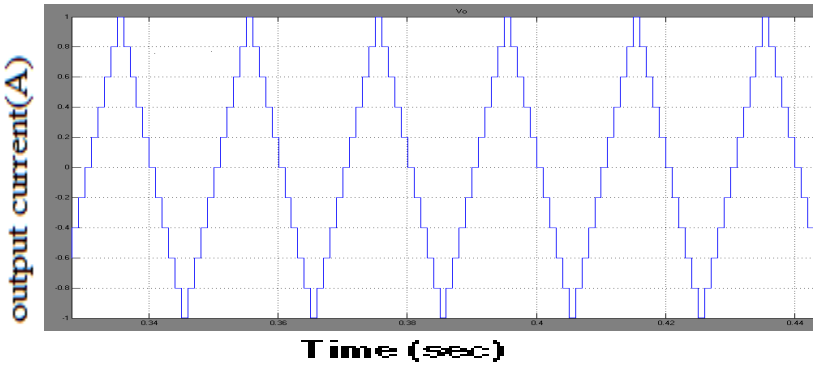

Fig 7. Output Current waveform

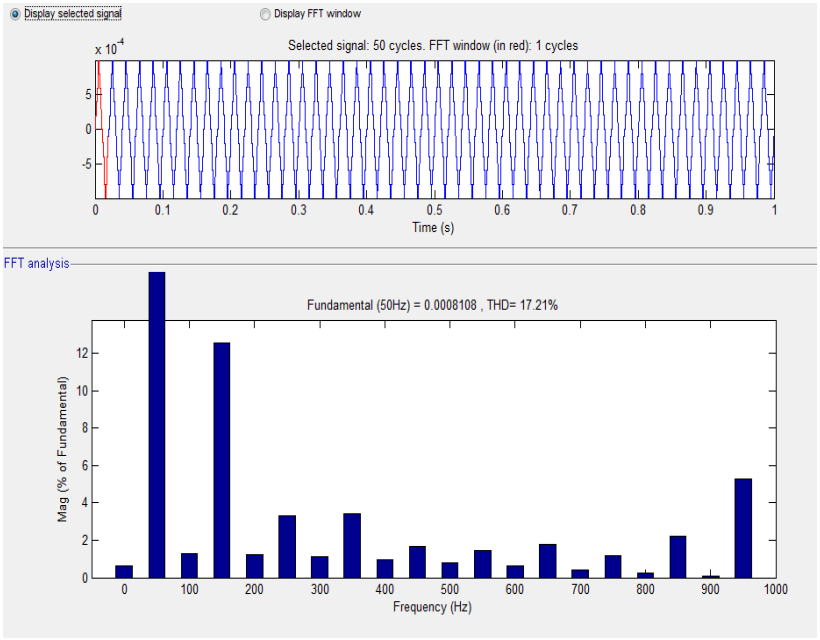

Fig 8.THD Analysis(Conventional)

VIII. SIMULATION DIAGRAM OF 11-LEVEL (PROPOSED) CASCADED MULTILEVEL INVERTER

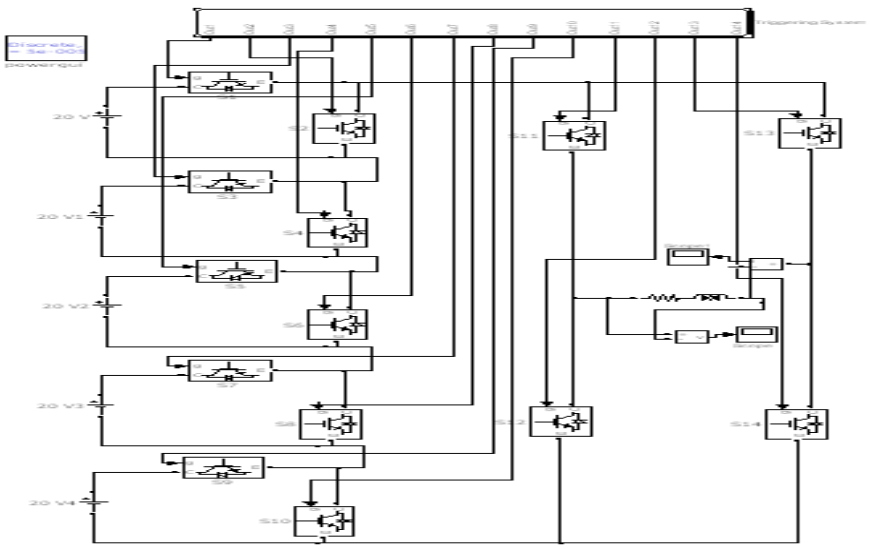

Fig 9. 11-level Cascaded Multilevel inverter(proposed)

Table 6: Switching sequence for proposed topology

	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20	1	0	0	1	0	1	0	1	0	1	1	0	0	1
40	1	0	1	0	0	1	0	1	0	1	1	0	0	1
60	1	0	1	0	1	0	0	1	0	1	1	0	0	1
80	1	0	1	0	1	0	1	0	0	1	1	0	0	1
100	1	0	1	0	1	0	1	0	1	0	1	0	0	1
80	1	0	1	0	1	0	1	0	0	1	1	0	0	1
60	1	0	1	0	1	0	0	1	0	1	1	0	0	1
40	1	0	1	0	0	1	0	1	0	1	1	0	0	1
20	1	0	0	1	0	1	0	1	0	1	1	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-20	1	0	0	1	0	1	0	1	0	1	0	1	1	0
-40	1	0	1	0	0	1	0	1	0	1	0	1	1	0
-60	1	0	1	0	1	0	0	1	0	1	0	1	1	0
-80	1	0	1	0	1	0	1	0	0	1	0	1	1	0
-100	1	0	1	0	1	0	1	0	1	0	0	1	1	0
-80	1	0	1	0	1	0	1	0	0	1	0	1	1	0
-60	1	0	1	0	1	0	0	1	0	1	0	1	1	0
-40	1	0	1	0	0	1	0	1	0	1	0	1	1	0
-20	1	0	0	1	0	1	0	1	0	1	0	1	1	0

IX. OUTPUT WAVEFORMS (PROPOSED)

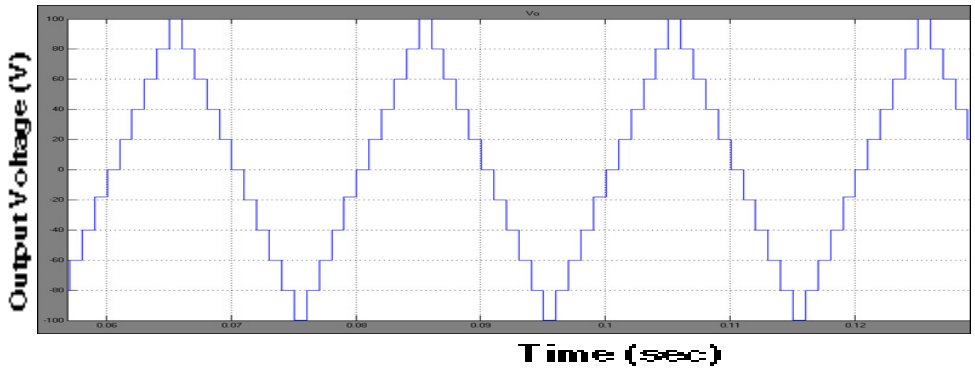

Fig 10. Output Voltage Waveform

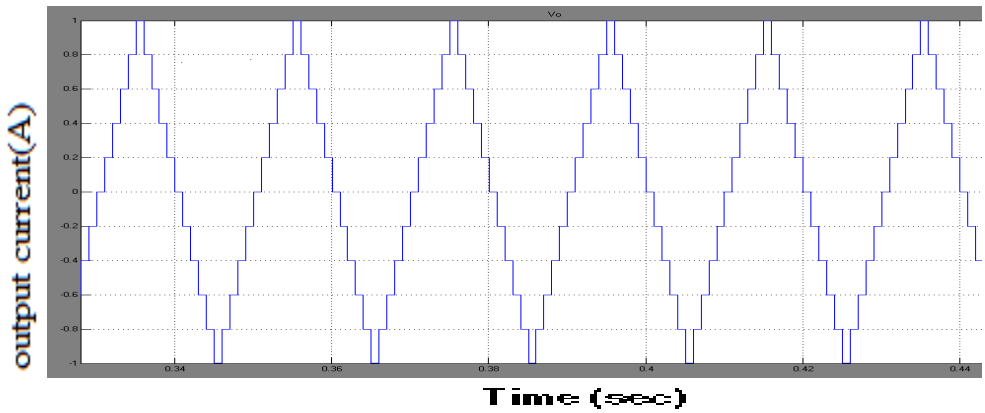

Fig 11. Output Current waveform

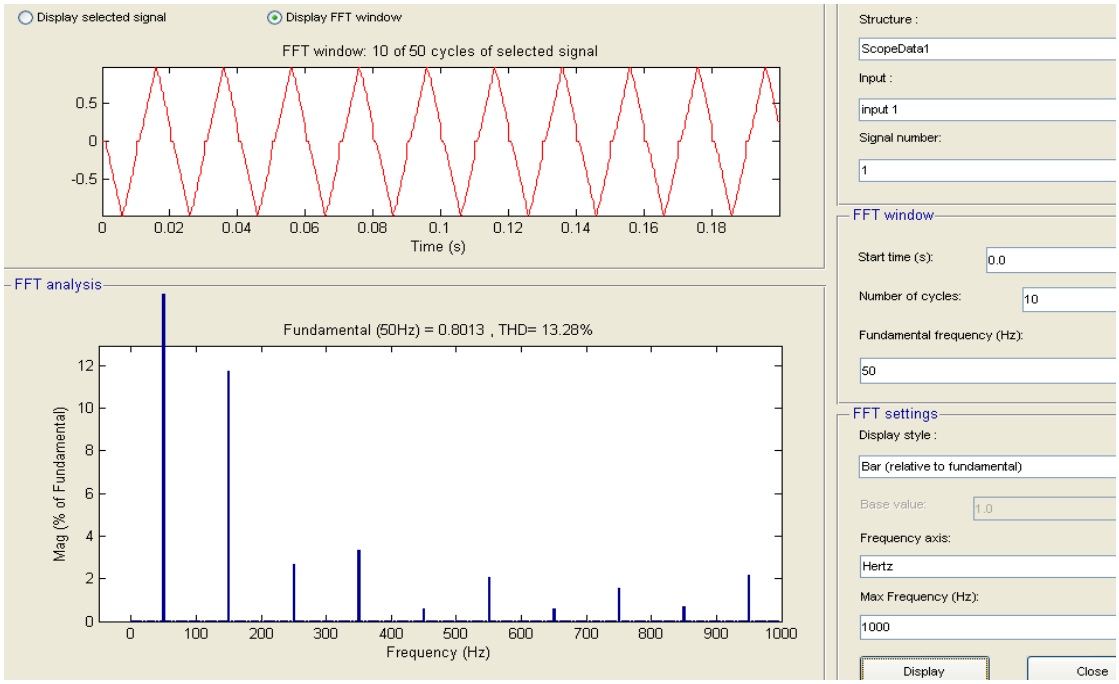

Fig 12.THD Analysis (Proposed)

X. MATHEMATICAL METHOD OF SWITCHING

The control of the new family of multilevel inverters is to choose a series of switching angles to synthesize a desired sinusoidal voltage waveform synthesized by a 2s + 1 level inverter, where s is the number of switching angles, which also equals the number of dc sources.
To reduce 3rd and 5th order harmonics in the 11-level inverter, three nonlinear equations can be set up as follows:

$$\cos(\alpha(1))+\cos(\alpha(2))+\cos(\alpha(3))+\cos(\alpha(4))+\cos(\alpha(5))=M$$
$$\cos(3\alpha(1))+\cos(3\alpha(2))+\cos(3\alpha(3))+\cos(3\alpha(4))+\cos(3\alpha(5))=0$$
$$\cos(5\alpha(1))+\cos(5\alpha(2))+\cos(5\alpha(3))+\cos(5\alpha(4))+\cos(5\alpha(5))=0$$

Where,

Modulation index, M = Vm/5Vdc

XI. SOLUTION USING GENETIC ALGORITHMS

A GA for optimization is different from ‘‘classical “optimization methods in several ways: random versus deterministic operation, population versus single best solution and selecting solutions via ‘‘survival of the fittest’’.The solution to the harmonic elimination problem is five switching angles α1, α2, α3, α4, α5. Each switching angle is called a gene. A chromosome consists of all the genes and in this case there are five genes in one chromosome. Thus, each chromosome represents a possible solution to the problem

A. Encoding of a Chromosome

The population size remains constant throughout the whole process.. The most used way of encoding is a binary string. Indeed, there are many other ways of encoding. The encoding depends mainly on the problem considered. In this study, a binary coding system is used. A string then could look like this (in the binary case):

String 1 1101100100110110
String 2 1101111000011110

A string in GAs may be divided into a number of substrings. The number of sub-strings, usually, equals the number of problem variables.

B. Fitness Function

The fitness function is the function responsible for evaluation of the solution at each step. The objective here is determining the switching angles such that some selected harmonics are minimized or put equal to zero.

C. Selection

The GA performs a selection process in which the ‘‘most fit’’ members of the population survive, and the ‘‘least fit’’ members are eliminated.

D. Crossover

Crossover operates on selected genes from the parent chromosomes and creates new offspring. Crossover can be illustrated as follows :(j is the crossover point):

Chromosome 1 11011j00100110110
Chromosome 2 11011j11000011110
Offspring 1 11011j11000011110
Offspring 2 11011j00100110110

E. Mutation

After performing crossover, mutation takes place. Mutation is used to prevent all the solutions in the population falling into a local optimum of the solved problem.. In case of binary encoding, we can switch a few randomly chosen bits from 1 to 0 or from 0 to 1.

Mutation can be illustrated as follows:

Original offspring 1 1101111000011110
Original offspring 2 1101100100110110
Mutated offspring 1 1100111000011110
Mutated offspring 2 1101101100110110

The technique of mutation (as well as crossover) depends mainly on the encoding of the chromosomes.

XII. SIMULATION DIAGRAM WITH GA CONTROLLER

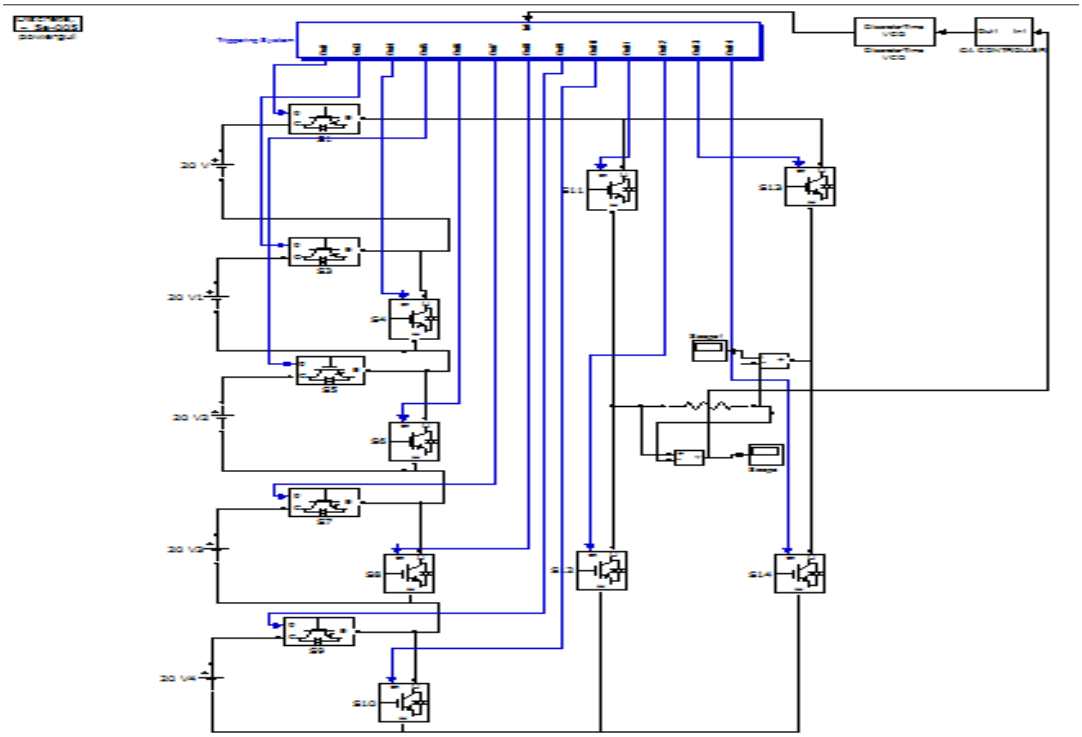

Fig .13 11-level Cascaded Multilevel inverter with GA Controller

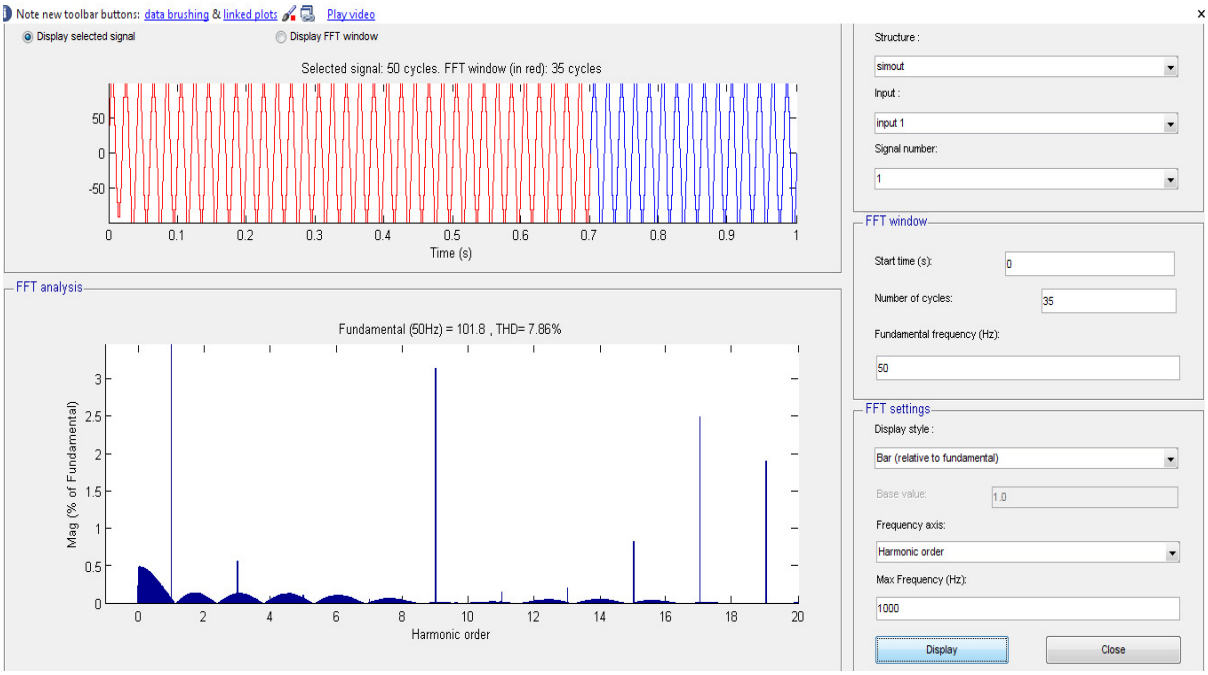

Fig 14.THD Analysis (with GA)

XIII. RESULTS OBTAINED

Table 7: THD Comparison

TYPE	THD	3rd HARMONIC	5th HARMONIC
CONVENTIONAL	18.75%	13.57%	4.9%
PROPOSED	13.27%	11.8%	2.8%
PROPOSED WITH GA	7.86%	0.6%	Eliminated

In Conventional Cascaded multilevel inverter, the observed THD is **17.2 %.**In our proposed topology of multilevel inverter with reduced number of switches ,the observed THD value is **13.2%** and then with GA control techniques, the THD is further reduced to 7.86% and the **3rd and 5th Order harmonics** has been eliminated.

XIV. CONCLUSION

The selective harmonic elimination of a new family of multilevel inverters using GA has been presented. The new configuration has the advantage of a reduced number of switching devices compared to traditional configurations of the same number of levels. The GA technique usually produces more than one possible solution set for each harmonic profile and a given specific modulation index. For multiple solutions, the solution that gives the lowest THD is selected. Both simulation and experimental results show that the algorithm can be effectively used for selective harmonic elimination of the new family of multilevel inverters and results in a dramatic decrease in the output voltage THD.

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