AN OPTIMAL FLIP FLOP DESIGN FOR VLSI POWER MINIMIZATION

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ABSTRACT

The power consumption is critically important in modern VLSI circuits especially for low-power applications. Optimization of power at the logic level is one of the most important tasks to minimize the power. Among logic components, latches and flip-flops are critical to the performance of digital systems. It is important to reduce the power dissipation in both clock distribution networks (CDN) and flip-flops. This paper presents a comparison of existing flip-flop classes in terms of transistor count, parasitic values and power dissipation. The operation of each flip-flop is analyzed and it is simulated using Tanner EDA in 250nm technology at room temperature in schematic level. And it reveals that the proposed design features the best performance in four FF designs under comparison.

KEYWORDS: *Flip flops, Power consumption, Pulse triggered.*

I. INTRODUCTION

In the past, the major concerns of the VLSI designer were area, performance, cost and reliability. Power consideration was mostly of only secondary importance. In recent years however, this has begun to change and, increasingly, power is being given comparable weight to area and speed considerations. Several techniques to reduce the dynamic power have been developed, of which clock gating is predominant [1]. The major fraction of the total power consumption in highly synchronous systems, such as microprocessors, is due to the clock network. One of the challenges of low power methodologies for synchronous systems is the power consumption of the flip-flops and latches. It is important to save power in these flip-flops and latches without compromising state integrity or performance [2].

This paper presents an approach to minimize the power consumption in flip flop design. Analysis is done on several existing designs. And modifications are done on the proposed design by adopting clock gating .Section II details the existing flip flop designs and its limitations. Section III deals with the proposed design which is explained along with working, its advantages, and applications and so on. Section IV includes the simulation results. The results are concluded along with the future scope.

II. EXISTING DESIGNS

Flip-Flops and latches are the basic elements for storing information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. Pulse-triggered FF (P-FF) has been considered a popular alternative to the conventional master–slave-based FF in the applications of high-speed operations. Besides the speed advantage, its circuit simplicity is also beneficial to lowering the power consumption of the clock tree system.

A P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Since triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master–slave configuration, is needed. The three existing pulse Triggered flip flops are implicit data close to output (ip-DCO), Master Hybrid Latch Level Triggered flip flop (MHLLF), Single Ended Conditional Capture Energy Recovery (SCCER).

1. Implicit Pulse Triggered DCO Flip Flop

A state-of the- art P-FF design, named ip-DCO, is given in Fig.1 [6].It contains an AND logic-based pulse generator and a semi dynamic structured latch design. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3.In ip-DCO the clock signal and complement of the clock signal generates a narrow pulse of short pulse width. During this pulse the output follows the input.
Two practical problems exist in this design. First, during the rising edge, NMOS transistors N2 and N3 are turned on. If data remains high, node x will be discharged on every rising edge of the clock. This leads to a large switching power. The other problem is that node x controls two larger MOS transistors (P2 and N5). The large capacitive load to node 'x' cause's speed and power performance degradation. When the x as denoted floating node, The node x controls two larger transistors P2 and N5, this leads to large capacitive load to node x causes power performance degradation.

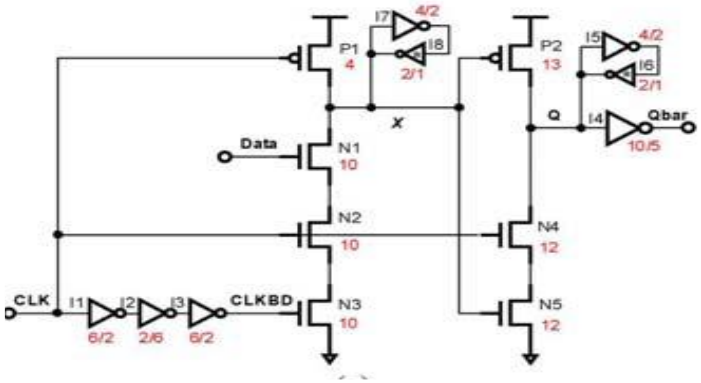

Figure 1.implicit Data Close to Output

2. Master Hybrid Latch Level Triggered Flip Flop

Fig.2 shows an improved P-FF design, named Master Hybrid Latch Level Triggered Flip-flop (MHLLF), by employing a static latch structure [7],[8]. Node X is no longer precharged periodically by the clock signal. A weak pull-up transistor P1 controlled by the FF output signal Q is used to maintain the node X level at high when Q is zero.

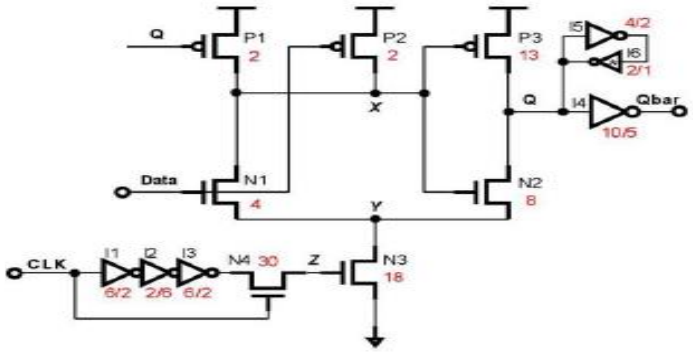

Figure2. Master Hybrid Latch Level Triggered Flip-flop

This design eliminates the unnecessary discharging problem at node X. However, it encounters a longer Data-to-Q (D-to-Q) delay during "0" to "1" transitions because node X is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node X becomes floating when output Q and input Data both equal to "1". Extra DC power emerges if node X is drifted from an intact "1"

3. Single Ended Conditional Capture Energy Recovery FF

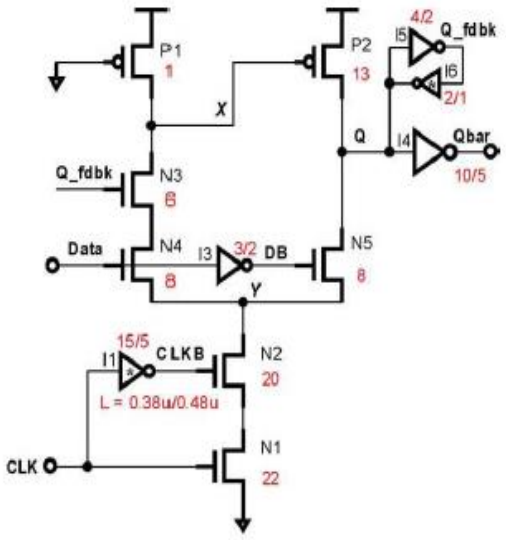

Figure 3. Single Ended Conditional Capture Energy Recovery FF

Fig. 3 shows a refined low power P-FF design named Single Ended Conditional Capture Energy Recovery (SCCER) using a conditional discharged technique[7],[9]. In this design, the keeper logic (back-to-back inverters) I7 and I8 in Fig. 1 is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node X. The discharge path contains nMOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node X, an extra nMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is "1" and node X is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed to ensure node X can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

III. PROPOSED DESIGN

The P-FF design with pulse control scheme, as shown in Fig. 4 adopts two measures to overcome the problems associated with existing P-FF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." Refer to Fig. 4the upper part latch design is similar to the one employed in SCCER design[5]. As opposed to the transistor stacking design in Fig. 1 and 3, transistor N2 is removed from the discharging path. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at zero most of the time. When both input signals equal to "0" (during the falling edges of the clock), temporary floating at node Z is basically harmless.

At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at node Z can be reduced due to a diminished voltage swing. Unlike

the MHLLF design, where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors (N2 and N3) speeds up the operations of pulse generation.
With this design measure, the number of stacked transistors along the discharging path is reduced and the sizes of transistors N1- N5 can be reduced also. In this design, the longest discharging path is formed when input data is "1" while the Qbar output is "1."To enhance the discharging under this condition, transistor P3 is added. Transistor P3 is normallyturned off because node X is pulled high most of the time. It steps in when node X is discharged to lVTPl below the VDD. This provides additional boost to node Z (from VDD_VTH to VDD). The generated pulse is taller, which enhances the pull-down strength of transistor N1. After the rising edge of the clock, the delay inverter I1 drives node Z back to zero through transistor N3 to shut down the discharging path.

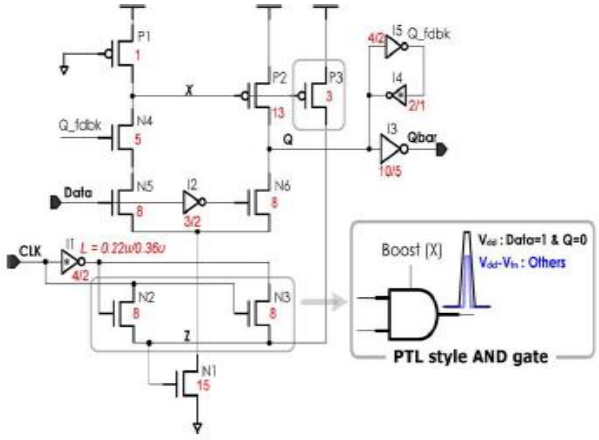

Figure 4. Schematic of proposed P-FF

The voltage level of Node X rises and turns off transistor P3 eventually. With the intervention of P3, the width of the generated discharging pulse is stretched out. This means to create a pulse with sufficient width for correct data capturing, a bulky delay inverter design, which constitutes most of the power consumption in pulse generation logic, is no longer needed. It should be noted that this conditional pulse enhancement technique takes effects only when the FF output Q is subject to a data change from 0 to 1. The leads to a better power performance than those schemes using an indiscriminate pulse width enhancement approach. Another benefit of this conditional pulse enhancement scheme is the reduction in leakage power due to shrunken transistors in the critical discharging path and in the delay inverter.

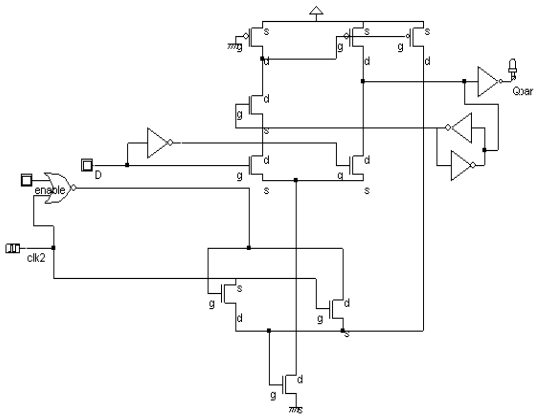

Figure 5. Schematic of modified P-FF

To reduce the power consumption to the minimum level clock gating technique is employed as shown in Fig 5.[3],[7].This is done by using a NOR gate instead of NOT gate in the pulse generating part . If 0 is applied to enable input then this circuit works normally. When enable pin is 1 then circuit goes to clock gating mode thereby reduce total power in ideal mode.

IV. SIMULATION RESULTS

The simulation setup model is to mimic the signal rise and fall time delays, input signals are generated through buffers. Considering the loading effect of the FF to the previous stage and the clock tree, the power consumptions of the clock and data buffers are also included. The output of the FF is loaded with a 20-fF capacitor. An extra capacitance of 3 fF is also placed after the clock buffer. The power consumption and timing behaviour of these FF designs is calculated. The power consumption of the enhanced pulse triggered flipflop design is the lowest in all test patterns because of shorter discharging path [11].

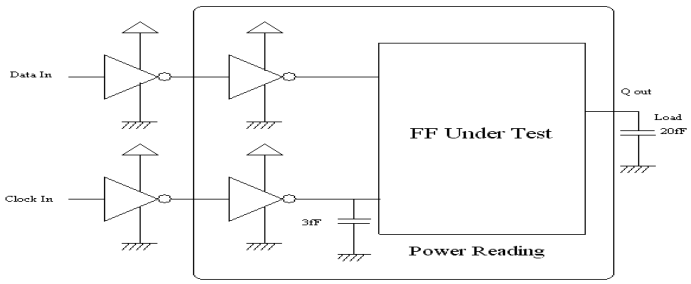

Figure 6 Simulation setup model

The simulation result for the above various types of flip flop were obtained from Tanner EDA in 250nm technology at room temperature. The supply voltage VDD is 5V. Simulation result for the various designs is shown below. The power consumed is more in ip-DCO design[10].

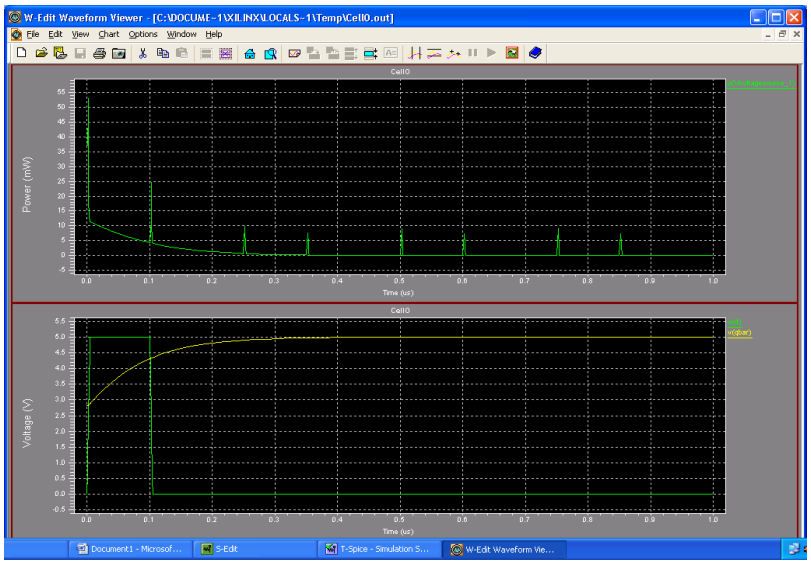

Figure 7. Simulation result for ip-DCO design

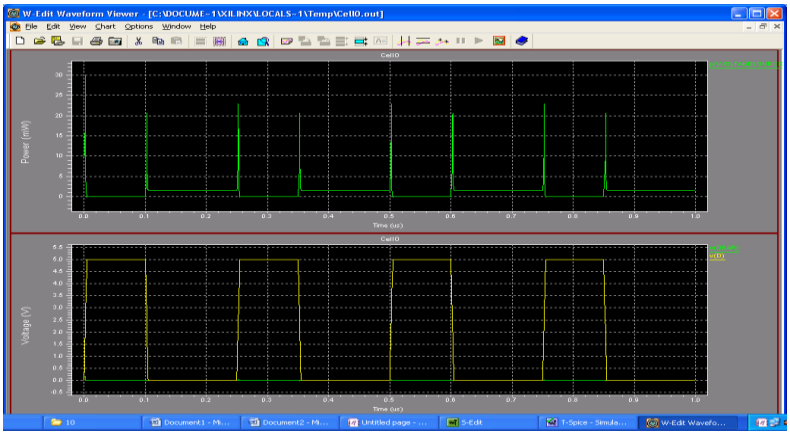

Figure 8. Simulation result for MHLLFF design

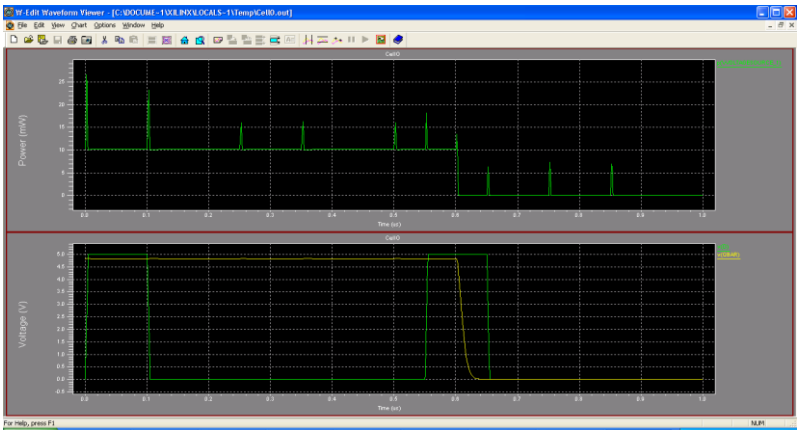

Figure 9 . Simulation result for SCCER Design

By compairing with all other designs the proposed design have less power consumption .

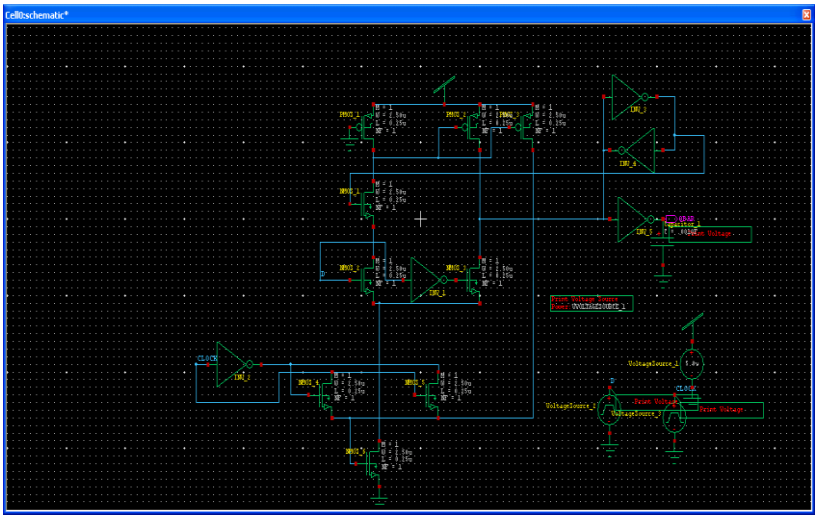

Figure 10. Proposed P-FF Design in Tanner EDA

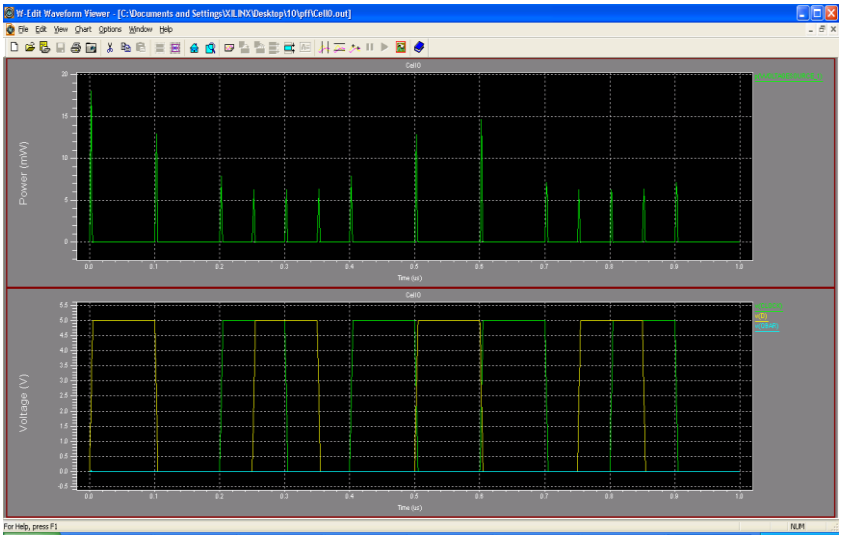

Figure 11 . Simulation result for proposed P-FF Design

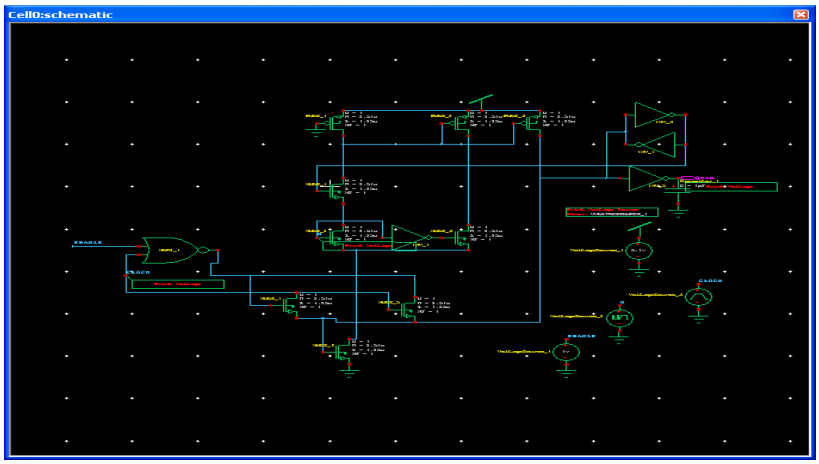

Figure 12 . Modified P-FF Design in Tanner EDA

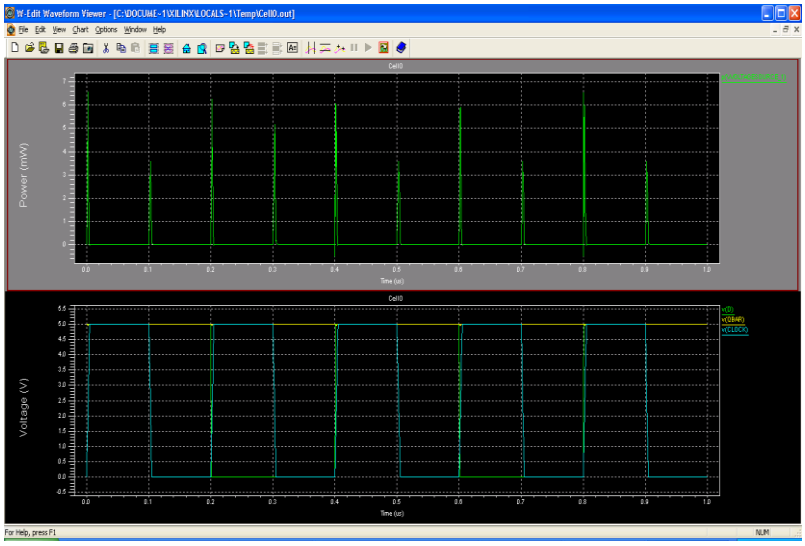

Figure 13. Simulation result for modified P-FF Design

Table 1. Feature Comparison of Various P-FF

Index	Ip-DCO	MHLLF	SCCER	Proposed P-FF
No. of Transistors	**23**	**19**	**19**	**19**
Power Consumption (mW)	**55**	**30**	**25**	**18**

Table 1 summarizes important performance indexes of various designs. A trade-off in performance occurs in the proposed P-FF design.

V. CONCLUSIONS

In this paper, the various Flip flop design like, ip-DCO, MHLLF and SCCER are discussed. These were been also designed in Tanner EDA tool and those result waveforms are also discussed. The comparison table is also added to verify the designed methods. With these all result the proposed P-FF performed better than all other designs. The proposed design used two new design measures. The first one successfully reduces the number of transistors stacked along the discharging path by incorporating a PTL-based AND logic. The second one supports conditional enhancement to the height and width of the discharging pulse so that the size of the transistors in the pulse generation circuit can be kept minimum. Thus the power consumption of the proposed pulse triggered flip-flop design is the lowest because of shorter discharging path. By modifying the design, the power consumption can be lowered to the minimum level.

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