FAULT TOLERANCE IN FPGA THROUGH KING SHIFTING

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ABSTRACT
A wide range of fault tolerance methods for FPGAs have been proposed. Approaches range from simple architectural redundancy to fully on-line adaptive implementations. The homogeneous structure of field programmable gate arrays (FPGAs) suggests that the defect tolerance can be achieved by shifting the configuration data inside the FPGA. All methods and schemes are qualitatively compared and some particularly promising approaches are highlighted. The applications of these methods also differ; some are used only for manufacturing yield enhancement, while others can be used in-system. This survey attempts to provide an overview of the current state of the art for fault tolerance in FPGAs.In this paper we have discussed the king shifting allocation method.

KEYWORDS: *Fault tolerance, Field programmable gate array (FPGA), King allocation.*

I. INTRODUCTION

As process technology scaling continues, manufacturing large defect-free integrated circuits become increasingly difficult. There is also the added problem of degradations over time after a device has been successfully deployed in the field. These reliability issues are particularly acute with FPGAs.
Recently, the defect and fault tolerance in FPGA has been subject in several researches [2]. But the makers are still searching more reliable chips with low cost (area, hardware, complexity, delay, etc.) and high yield improvement. On the other hand for the user side point of view, the requirement of systems with fault tolerance becomes a real necessity, especially for some applications where the time required for the reparation process (downtime) have a critical impact on the system. A recent study suggested that future FPGAs at and beyond the 45nm technology node will have such low yield that defect tolerance scheme will be unavoidable in large FPGAs [1].
By the application of king shifting allocation method, the proposed design makes 3 selections of chip usage possible as follows:

1. Defect-free chips which can be used as a maximum array size of N × N CLBs,
2. Defect-free chips which can be used as fault-tolerant chips of an array size M × M CLBs, where M < N,
3. Defective chips (which are avoidable by the proposed design) can be used as an array size of M × M CLBs.

To reach this goal, the FPGA’s SRAM part is modified so that it will be able to shift the on-chip data vertically and horizontally. It means that the whole user data can be shifted vertically by one row or horizontally by one column. The user data is shifted on-chip, but not modified. Some CLBs are reserved as spare and distributed regularly among the whole FPGA area. When the defect is detected and located by one testing method it can easily be avoided by shifting the whole user data so that the data corresponding to the most nearest spare is shifted in the defective CLB. Consequently the defective CLB will not be used. In this paper the allocation of the spare CLBs within the 2-dimensional arrays, which is named as king-shifting allocation is introduced. In this, when a defect is observed, the data can be shifted in the convenient direction so that the defect is avoided. In the below section we have given the overview of FPGA architecture and discussed the fault, especially the stuck-at-fault associated with it. Thereafter the basic idea of implementation is given and the king allocation method is discussed. The result of the method has been shown along with the conclusion.

II. BACKGROUND

2.1 FPGA Architecture

An FPGA is an integrated circuit composed of programmable routing resources and programmable logic resources. The programmable logic, called configurable logic blocks (CLBs), are composed of k-input lookup tables and flip-flops. Each lookup table can implement any k-input logic function, and connects with a designated flip-flop. Together, the lookup table and flip-flop pair form a basic logic element (BLE). Figure 1 shows a CLB with I inputs and N BLEs. Programmable routing can be further divided into three parts: the wires, the switch blocks (S blocks) and the connection blocks (C blocks). Together, the logic blocks, wires, S blocks and C blocks for modern commercial FPGAs are organized into island-style architecture as shown in Figure 2.2. This architecture has proven to be very successful in modern FPGA architectures and in VLSI. As such, the island-style architecture was also used as the foundation for the new defect-tolerant architecture.

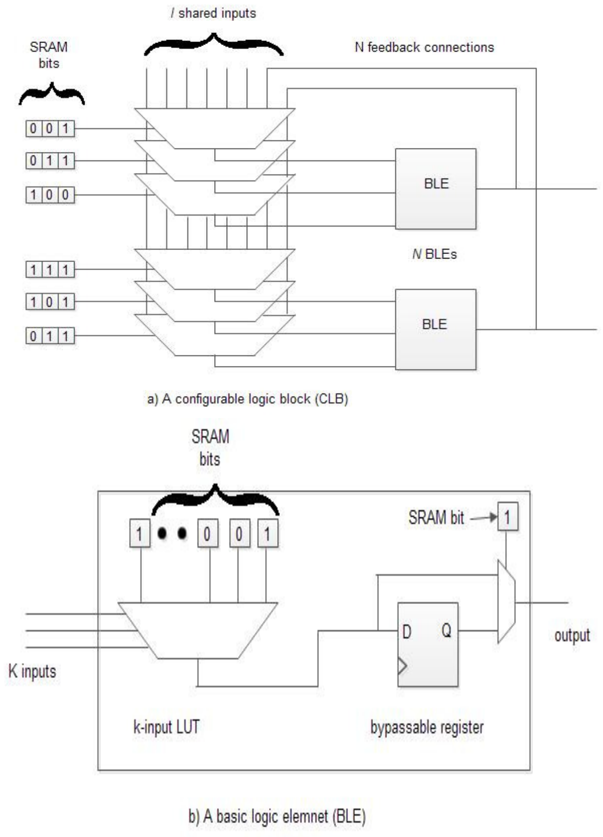


Fig.1 Overview of Fine-Grain Hardware Redundancy

Wires within an FPGA reside in routing channels and are indexed by track numbers. A channel, as shown in Figure 2, spans the width or height of the FPGA and has its boundaries defined by the CLBs. A wire’s track number is based on its position relative to the width of the channel. The convention of this paper is that a wire at the bottom-most/leftmost position in each channel is assigned a track number of 0. Similarly, wires at the top-most/right-most position are assigned a track number of channel width – 1.

2.2 Other types of fault

In addition to degradation, there are two other types of faults which can affect FPGAs. These are highly relevant to this study as some of the techniques which have been developed in response to them can also be applied to faults caused by degradation. The first of these is manufacturing defects. Manufacturing defects can be exhibited as circuit nodes which are stuck-at 0 or 1 or switch too slowly to meet the timing specification. Defects also affect the interconnect network and can cause short or open circuits and stuck open or closed pass transistors. Test and repair of manufacturing defects is well established in VLSI. The second type of fault which is widely discussed in relation to FPGAs comprises of Single Event Upsets (SEUs) and Single Event Transients (SETs) caused by certain types of radiation.

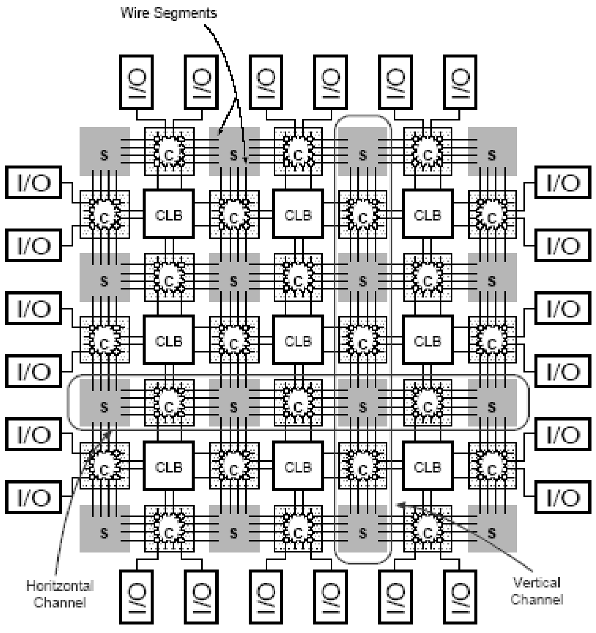


Fig.2 Island-style Architecture

III. THE BASIC IDEA OF IMPLEMENTATION

This design aims at giving the FPGA the possibility to shift the data of the configurations cells corresponding to the unit elements serially, vertically, and horizontally.

1. With the serial shifting, the FPGA can load the original configuration data into the SRAM serially.
2. With the horizontal shifting, the FPGA shifts in parallel the original configuration data of each unit column (one CLB column with its adjacent switching column) to the next unit column. Therefore, by shifting the data of one unit column, the data of column 1 will be shifted to the column 2 and the data of column 2 to the column 3, and the data of the last column will be shifted to the first column.
3. With the vertical shifting, the FPGA will be able to shift in parallel the original configuration data of each unit row (one CLB row with its adjacent switching row) to the next unit row. Therefore, by shifting the data of one unit row, the data of row 1 will be shifted to the row 2 and the data of row 2 to the row 3, and so on, and the data of the last row will be shifted to the first row.

For achieving this goal, the original hardware of the SRAM must be slightly modified in a new design. Since the column SF (stuck-at-fault) at the right side and the row SF at the bottom are not constructed into unit elements, we divide the SRAM into 3 parts: the homogeneous part, the non homogeneous part and the IOB part as shown in Fig. 3. The first part is constructed by the configuration cells of the unit elements only, and the second part is constructed by the configuration cells of the most right column and the row at the bottommost. In addition all configuration cells corresponding to the same unit element are juxtaposed in one set serially. For the SRAM part (Fig. 3

(a)) corresponding to each unit element, one multiplexer is added. These multiplexers allow the data corresponding to each unit element to be shifted serially or vertically or horizontally following the multiplexers.

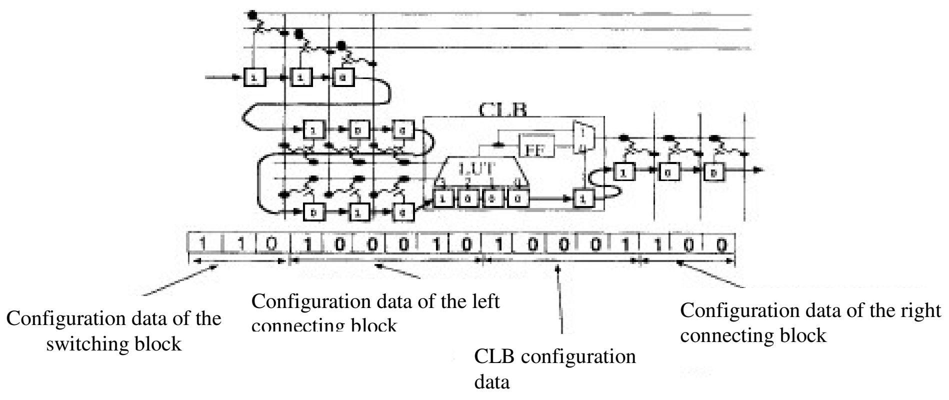
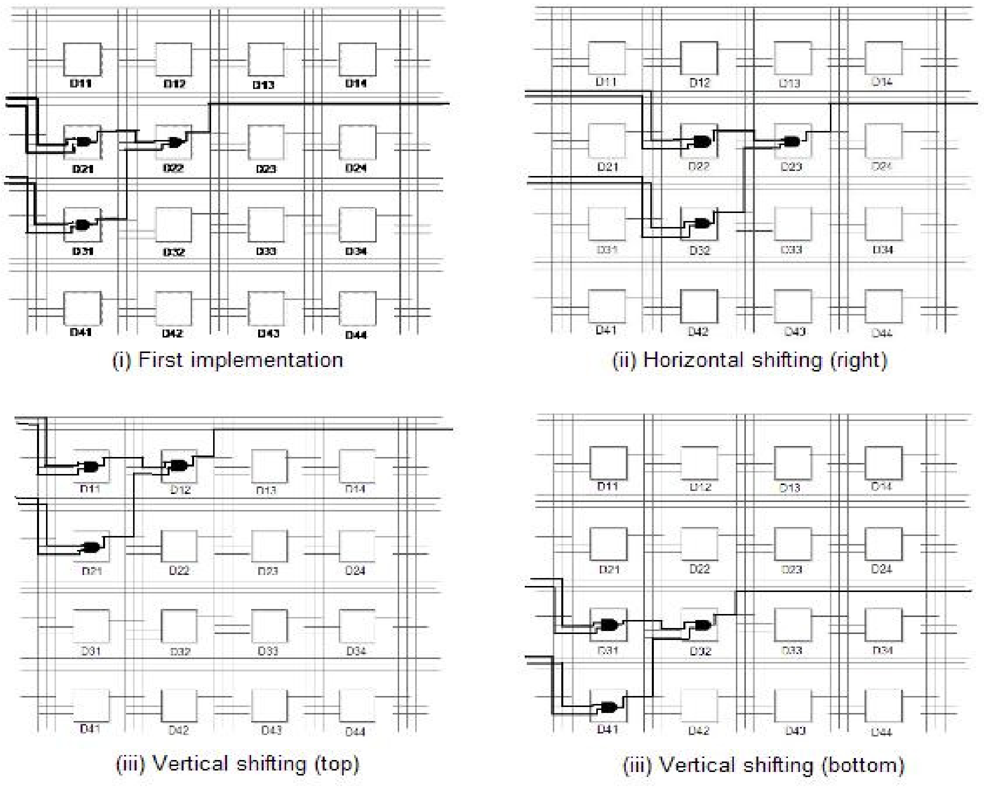

CLB
FF
LUT
1 1 0 1 0 0 0 1 0 1 0 0 0 1 1 0 0
Configuration data of the switching block
Configuration data of the left connecting block
CLB configuration data
Configuration data of the right connecting block

Fig.3(a) Example of unit element configuration data

The data in the homogeneous part can be shifted, while the non-homogeneous part does not allow the shifting. The separation between the homogeneous part and non homogeneous part is assured by one control signal commanding to one pass transistor.


D11 D12 D13 D14
D21 D22 D23 D24
D31 D32 D33 D34
D41 D42 D43 D44
(i) First implementation
(ii) Horizontal shifting (right)
(iii) Vertical shifting (top)
(iii) Vertical shifting (bottom)

Shifting the configuration data vertically and horizontally

Fig.3(b) Basic example of shifting the configuration data.

Based on the same idea, the configuration cells corresponding to the IOBs at every side (north, south, west and east) of the chip are gathered serially as shown in Fig. 3(b). One multiplexer permits to the data to be looped serially in each side separately. The multiplexer in each side are controlled by the shift controller. The memory cells corresponding to the IOBs in all sides are connected serially with the memory cells corresponding to the unit elements. The shift controller controls the additional hardware as the additional multiplexers, additional switches, etc.

IV. KING SHIFTING ALGORITHM FOR ALLOCATION OF SPARE RESOURCES

Fault tolerance is achieved only by shifting the original configuration inside the FPGA. King-shifting algorithm provides an effective way of distribution of spare allocation. In the chess game, the king has the possibility to protect the 8 cells around the cell where it is standing. Inspiring from this fact, the king-shifting distribution shown in Figure 5(a) reserves the CLB in the middle of each 3 x 3 CLBs within the chip as spare and gives the possibility to each spare cell to cover the 8 cells around it position. The original configuration data, which is mapped in the usable cells, can be shifted on-chip by some columns. When a defect/fault is detected the whole user data is shifted by one of the 8 directions. The defect/fault wherever it is situated within the 2-dimensional arrays, is assured to be covered by this shifting.

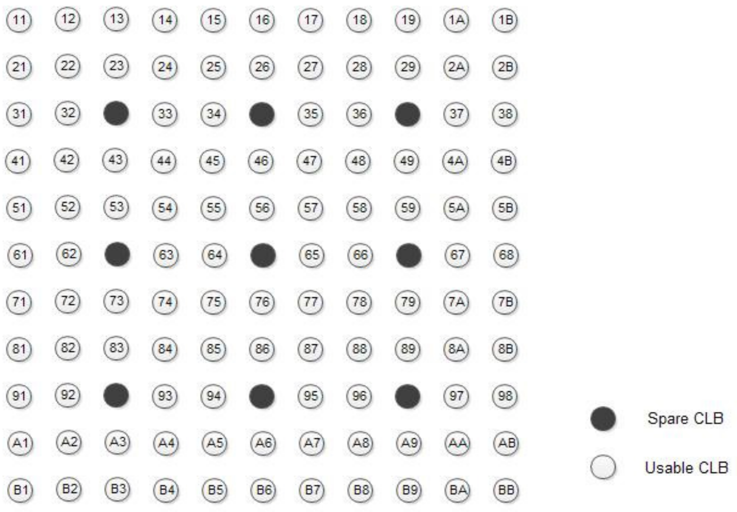
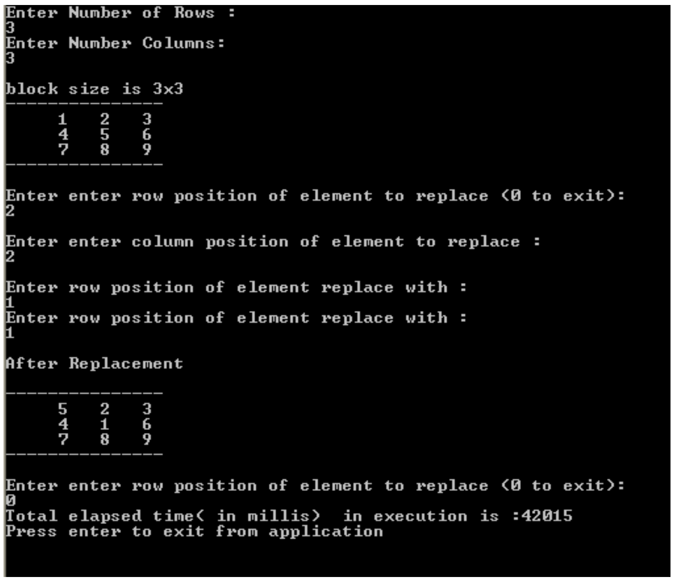


Figure 4: King Shifting Allocation

The basic algorithm for King-shifting method is shown below:
1. Create the CLBs block size of 3 X 3.
2. Each 3 X 3 are having 9 CLBs.
3. Allot one spare CLB in each 3 X 3 block.
4. If one of the 9 CLB is faulty then it should get swap with the spare CLB present in 3 X 3.

V. EXPERIMENTAL RESULTS

In all the previous work that has been done in this research area, parameters like yield, memory overhead and CLB overhead has been taken into account. In our paper we have highlighted on the execution time of this algorithm. We have implemented the proposed algorithm by writing a code using C language. The result that we are getting is according to the above algorithm, the swapping of the CLBs has been achieved. The spare blocks in this case are dependent on the number of CLBs and we didn’t take any spare CLBs across the rows and columns as it was taken in the previous algorithm.



```
Enter Number of Rows :
3
Enter Number Columns:
3

block size is 3x3
---------------
     1   2   3
     4   5   6
     7   8   9
---------------

Enter enter row position of element to replace (0 to exit):
2

Enter enter column position of element to replace :
2

Enter row position of element replace with :
1
Enter row position of element replace with :
1

After Replacement

---------------
     5   2   3
     4   1   6
     7   8   9
---------------

Enter enter row position of element to replace (0 to exit):
0
Total elapsed time( in millis)  in execution is :42015
Press enter to exit from application
```

Figure 5: Result of King Shifting Allocation

VI. CONCLUSIONS

In this paper, a novel fault tolerant technique for FPGA-based systems is presented. Here fault tolerance is achieved by only shifting the design data automatically, without changing the physical design of the running application, without loading other configurations data from the on-chip FPGA. This paper highlights on the King-Shifting algorithm for the effective distribution of spare resources. In our paper we have computed the execution time of our algorithm and thus has taken into account the timing overhead associated with it.

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