CNTFET-BASED DESIGN OF ANALOGUE CIRCUITS

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ABSTRACT

In this paper we implement a semi-empirical compact model for CNTFETs already proposed by us to simulate typical analogue circuits both in SPICE, using ABM library, and in Verilog-A. The obtained results are the same in static simulations and comparable in dynamic simulations. However using Verilog-A the simulation run time is much shorter and the software is much more concise and clear than schemes using ABM blocks in SPICE. Moreover we present, through the design of a basic current mirror, a comparison between CNTFET and MOS technology. For every simulation we evaluate parameters of merit in order to show the differences between CNTFET and MOS technology and the advantages of the first for analog VLSI circuits.

KEYWORDS

CNTFET-based design, Modelling, Analog Circuits, MOS Technology, Verilog-A, SPICE..

I. INTRODUCTION

Prediction through modelling forms the basis of engineering design. Engineers need models which relate to their design area and are adaptable to new design concepts. They also need efficient and friendly ways of presenting, viewing and transmitting the data associated with their models.
With reference to Carbon Nanotube Field Effect Transistors (CNTFETs) [1], which are regarded as an important contending device to replace conventional silicon transistors, most of their models available in literature are numerical and make use of self-consistency and therefore they do not allow an easy implementation in circuit simulators, such as SPICE, Verilog or VHDL-AMS, which instead must be the main characteristic in the field of Computer Aided Design (CAD).
In Refs. [2-10] we have already proposed a compact, semi-empirical model of CNTFET, in which we introduced some improvements to allow an easy implementation both in SPICE, using ABM library, and in Verilog-A.
In this paper we implement our CNTFET model to simulate typical analog circuits both in SPICE and in Verilog-A. The obtained results are the same in static simulations and comparable in dynamic simulations, in which the differences are due to the better implementation in Verilog-A of the intrinsic capacitance model.
Moreover, through the design of a basic current mirror, we present a comparison between CNTFET and MOS technology. The simulation results, carried out with the simulator Advanced Design System, allow to show the differences between CNTFET and MOS technology and the advantages of the first for analog VLSI circuits.
The presentation is organized as follows. At first we briefly describe our compact, semi-empirical model of CNTFET, with reference to the main equations on which the CNTFET model is based.
Then typical analogue circuits are simulated and the results are presented to validate the implementation of our CNTFET model both in Verilog-A and in SPICE**.**

At last we present the design of a basic current mirror, together with the discuss of the relative results, conclusions and future developments

II. A BRIEF REVIEW OF OUR CNTFET MODEL

IIa) I-V Model

An exhaustive description of our model is in our Refs [2-7]. In this sub-Section we just describe the main equations on which our I-V model is based.

When a positive voltage is applied between drain-source (V_{DS} > 0 V), the hypothesis of ballistic transport [3] allows to assert that the current is constant along the CNT and therefore it can be calculated at the beginning of the channel, near the source, at the maximum of conduction band, where electrons from the source take up energy levels related to states with positive wave number, while the electrons from the drain take up energy levels related to states with negative wave number.

When a positive voltage is applied between gate-source (V_{GS} > 0 V), the conduction band at the channel beginning decreases by qV_{CNT}, where V_{CNT} is the surface potential and q is the electron charge. With the hypothesis that each sub-band decreases by the same quantity along the whole channel length, the drain current for every single sub-band can be calculated using the Landauer formula [11]:

$$I_{DSp} = \frac{4qkT}{h}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \tag{1}$$

where k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, ξ_{Sp} and ξ_{Dp} have the following expressions:

$$\xi_{Sp} = \frac{qV_{CNT}-E_{Cp}}{kT} \qquad \xi_{Dp} = \frac{qV_{CNT}-E_{Cp}-qV_{DS}}{kT} \tag{2}$$

being E_{Cp} the sub-bands conduction minima.

Therefore the total drain current can be expressed as:

$$I_{DS} = \frac{4qkT}{h}\sum_{p}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \tag{3}$$

The surface potential, V_{CNT}, is evaluated by the following approximation [2]:

$$V_{CNT} = \begin{cases} V_{GS} & \text{for } V_{GS} < \dfrac{E_C}{q} \\ V_{GS} - \alpha\left(V_{GS} - \dfrac{E_C}{q}\right) & \text{for } V_{GS} \geq \dfrac{E_C}{q} \end{cases} \tag{4}$$

where E_C is the conduction band minima for the first sub-band.

The parameter α, depending on V_{DS} voltage, CNTFET diameter and gate oxide capacitance C_{ox}, has been extracted from the experimental device characteristics [2-3] and has the following expression [12]:

$$\alpha = \alpha_0 + \alpha_1 V_{DS} + \alpha_2 V_{DS}^2 \tag{5}$$

IIb) C-V Model

An exhaustive description of our C-V model is widely described in our Ref. [2] and therefore the reader is requested to consult it. Now we just describe the main equations on which is based our C-V model.

To determine the quantum capacitances C_{GS} and C_{GD}, it is necessary to know the total channel charge Q_{CNT}, having the following expression:

$$Q_{CNT} = q\sum_{p}\left(n_{Sp} + n_{Dp}\right) \tag{6}$$

where n_{Sp} and n_{Dp} are electron concentrations by the source and the drain respectively in the p-th sub-band. Having:

$$N_0 = \frac{4kT}{3\pi a_0|\gamma|} \tag{7}$$

where a_0 is the carbon-carbon (C-C) bonding distance (≈ 0.142 nm) and γ the C-C bonding energy (≈ 3 eV), the number of carrier n_{ip} (i = S or D), which increases almost linearly as ξ_{ip} greater or equal than zero and falls off exponentially as ξ_{ip} becomes negative, can be derived from the following relationship [12]:

$$n_{ip} = N_0 \begin{cases} A_p \exp \xi_{ip} & \text{for } \xi_{ip} < 0 \\ B_p \xi_{ip} + A_p & \text{for } \xi_{ip} \geq 0 \end{cases} \qquad i = S, D \tag{8}$$

where the parameters A_p and B_p, depending on E_{Cp}, for $E_{Cp} < 0.5\,eV$, have the following empirical expressions [12]:

$$\begin{cases} A_p = -5.3E_{Cp}^2 + 10E_{Cp} + 1 \\ B_p = 0.34E_{Cp} + 1 \end{cases} \tag{9}$$

Therefore the quantum capacitances C_{GD} and C_{GS} are given by:

$$\begin{cases} C_{GD} = q\sum_{p}\dfrac{\partial n_{Dp}}{\partial V_{GS}} = q\sum_{p}\dfrac{\partial n_{Dp}}{\partial \xi_{Dp}}\dfrac{\partial \xi_{Dp}}{\partial V_{CNT}}\dfrac{\partial V_{CNT}}{\partial V_{GS}} \\ C_{GS} = q\sum_{p}\dfrac{\partial n_{Sp}}{\partial V_{GS}} = q\sum_{p}\dfrac{\partial n_{Sp}}{\partial \xi_{Sp}}\dfrac{\partial \xi_{Sp}}{\partial V_{CNT}}\dfrac{\partial V_{CNT}}{\partial V_{GS}} \end{cases} \tag{10}$$

The CNTFET equivalent circuit, reported in Fig. 1, is similar to a common MOSFET and is characterized by the generator V_{FB}, for accounting the flat band voltage, and by the resistors R_D and R_S, in which the parasitic effect due to the electrodes are also included.

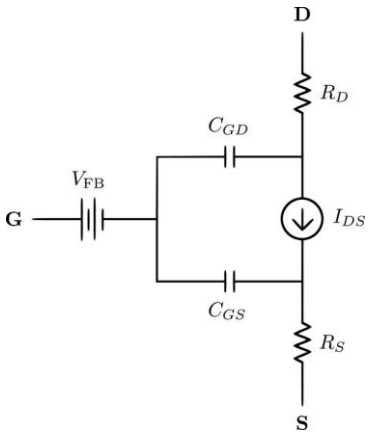


Figure 1. Equivalent Circuit of a n-type CNTFET [2-3].

Fig. 2a compares the $I_{DS} - V_{DS}$ characteristics (denoted by continuous lines) of numerical simulations with Verilog-A language and the experimental ones[13] (denoted by ●), in which we have assumed the same values for V_{FB}, CNT diameter, R_D and R_S reported in [13], while Fig. 2b compares the same with SPICE.

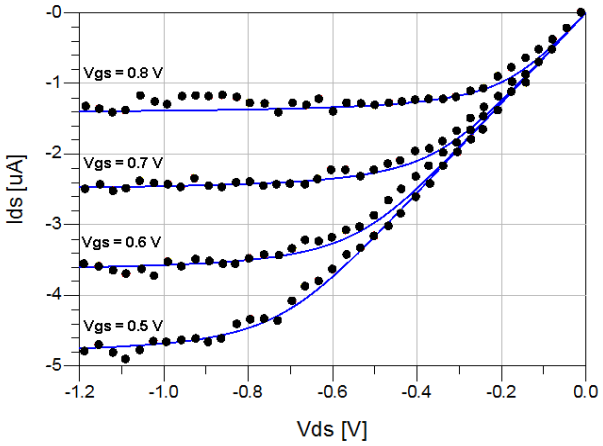


Figure 2a. Simulated $I_{DS} - V_{DS}$ characteristics (denoted by continuous lines) with Verilog-A and experimental $I_{DS} - V_{DS}$ characteristics [13] (denoted by ●).

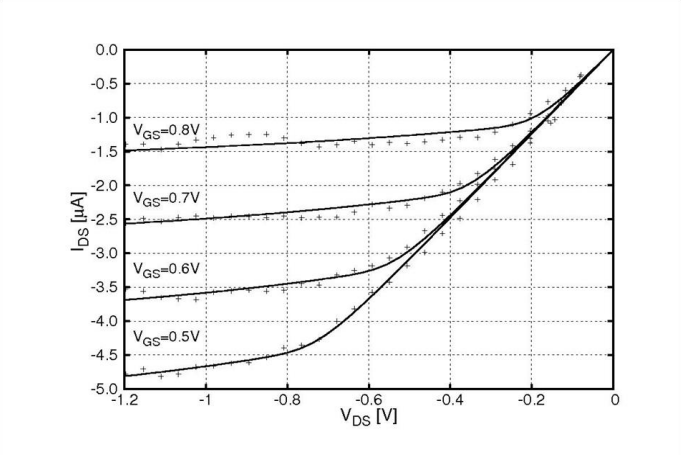


Figure 2b. Simulated $I_{DS} - V_{DS}$ characteristics (denoted by continuous lines) with SPICE and experimental I_{DS}–V_{DS} characteristics [13] (denoted by +).

It is easy to see that the obtained results are practically the same in static simulations. In particular the small difference around the knees of the I-V characteristics is due to the implementation issues, because in SPICE we have implemented a simplified formula using SOFTLIM block from the ABM library, unlike Verilog-A [3], [7-8].

Figures 3a and 3b show the implementation of the gate-drain and gate-source capacitances respectively using our C-V model in Verilog-A language, in which we have assumed V_{FB} = 0 V, CNT diameter d = 1.4 nm, $R_D = R_S = 0\ \Omega$ and C_{ox} = 3.8 pF/cm.

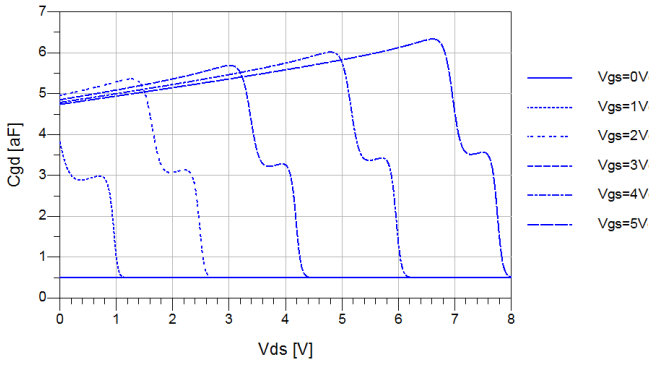


Figure 3a. Simulations of C_{GD} vs V_{DS} for different values of V_{GS} in Verilog-A.

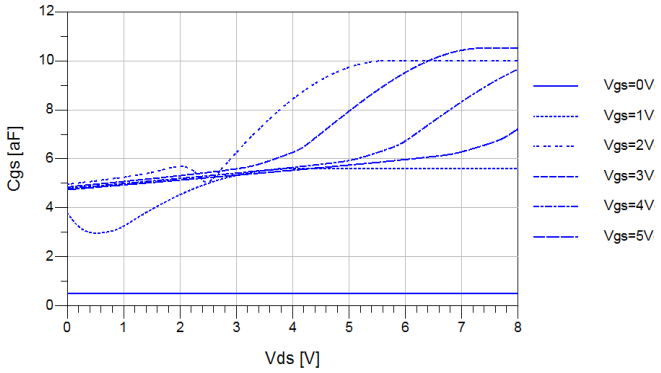


Figure 3b. Simulations of C_{GS} vs V_{DS} for different values of V_{GS} in Verilog-A.

The implementation of the same capacitances in SPICE has been reported in our Refs. [2-3], where we have obtained different values of gate-drain and gate-source capacitances, because in SPICE only one band in the capacitance model has been considered. In particular, the difference between the capacitance models comes from some simplifications we have adopted in our SPICE model [2-3], in order to do not weigh down the software further, unlike Verilog-A implementation.
However these differences have no influence on I-V characteristics, which are practically the same, as illustrated previously.

III. DISCUSSION OF ANALOG CIRCUIT SIMULATIONS

In all following simulations we have considered CNTFETs having a diameter of 1.42 nm, length of 100 nm and quantum capacitances depending on polarization voltages.
As first example, Fig. 4 shows a phase-shift oscillator, which includes three identical RC networks.

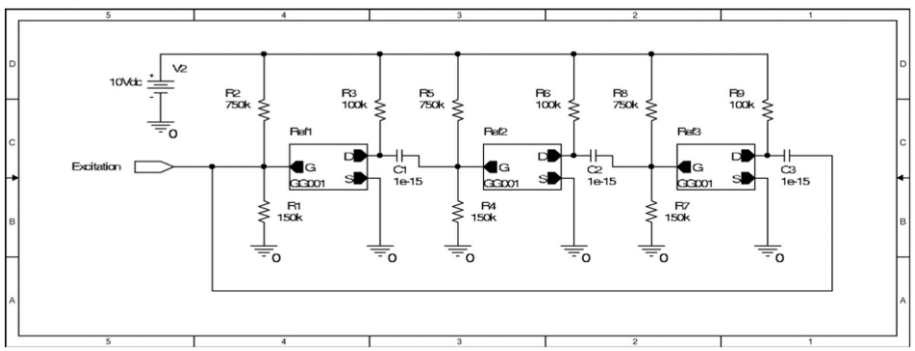


Figure 4. Phase-shift oscillator employed three CNTFETs.

In Fig. 5 we have reported the output voltage of Verilog-A simulation, while in Fig. 6 the same obtained with SPICE.

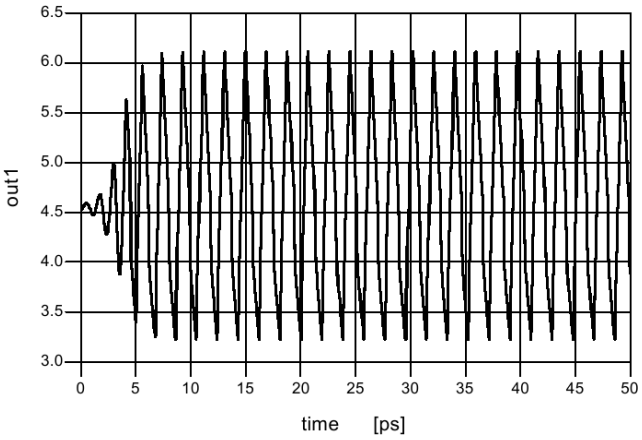


Figure 5. Output voltage of Verilog-A simulation for the phase-shift oscillator.

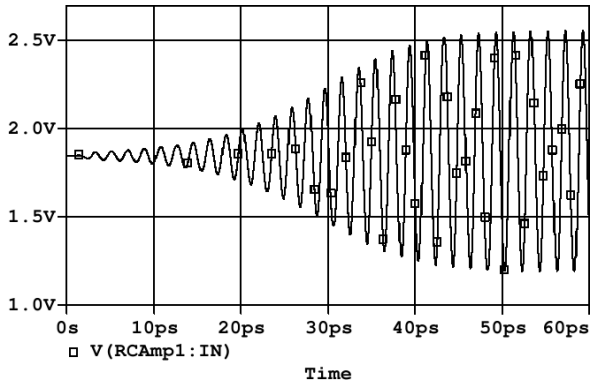


Figure 6. Output voltage of SPICE simulation for the phase-shift oscillator.

This simulation shows a small differences for the oscillation frequency (0.5 THz for SPICE [2-3], 0.53 THz for Verilog-A) and a larger difference in amplitude (1.3 V for SPICE, 2.9 V for Verilog-A). We think that these differences are mainly due to the fact that in the SPICE implementation it has been considered only one sub-band for the capacitance model, while in our Verilog-A implementation the number of sub-bands p can be defined as a parameter settable by the user. In particular we have set p equal to 3.

Moreover in Verilog-A it has been necessary to reduce the supply voltage, and therefore to modify the circuit, in order to reduce the parasitic gate source capacitances, while, since under SPICE the oscillator was pushed to the highest frequency, the circuit became very sensible to the model parameter variations.

However, using Verilog-A implementation the development time in writing the model is shorter, the simulation run time is much shorter and the software is much more concise and clear than schemes using ABM blocks in SPICE.

As second example, we analyze the design of a basic current mirror both in CNTFET and MOSFET technology.

The simulations are performed with Agilent Advanced Design System © 2009 SPICE simulation tool using the CNTFET model previously illustrated and MOSFET BSIM4 SPICE model of internal components library.

The CNTFETs in any proposed simulation have a diameter of 15 nm and a channel length of 32 nm.

Fig. 7 shows a basic current mirror, where a current sink is based on n-type C-CNTFET.

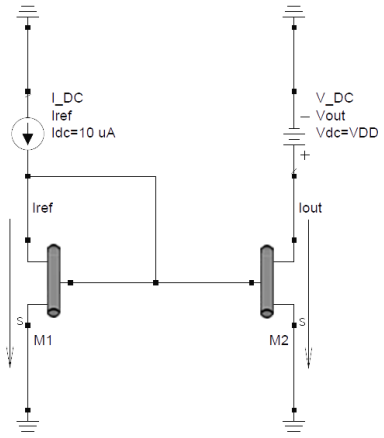


Figure 7. Basic current mirror circuit with a n-type CNTFET.

The I_{REF} reference current of 10 μA is provided by an ideal current supply on the left branch of the circuit. This current imposes the quiescent point of M1 in saturation region and provides the bias voltage on gate M2, which must faithfully follow the I_{REF} as long as output voltage $V_{DD} \geq V_T$, the voltage required to switch M2 on.
The drain voltage of M2 is swept in order to evaluate how well the output current replicate an ideal current supply.
The expected current value comes out from the general I-V characteristic of a FET device in saturation region, which is generally given by the following relation [1]:

$$I_{out} = k'(V_G - V_T)^2(1+\lambda V_{DD}) \tag{11}$$

where V_T is the threshold voltage and k' is a technology related constant depends by particular dimensional and construction features. Presence of λV_{DD} term calls out the second order effect of channel modulation, where λ is the channel length modulation constant. This unwanted phenomenon affects the behaviour of current mirror as non-ideal current supply on account of drain bias. Since M1 is a technologically equal device to M2, reference current should be mirrored as expected.
Afterwards the two n-type C-CNTFETs are substituted with an NMOS pair formed by devices with different sizes in order to compare MOSFET technology performances with CNTFET ones.
The I_{OUT} values are shown in Fig. 8 where a comparison with MOSFETs having different channel length L and constant aspect ratio, W/L = 2, is illustrated.

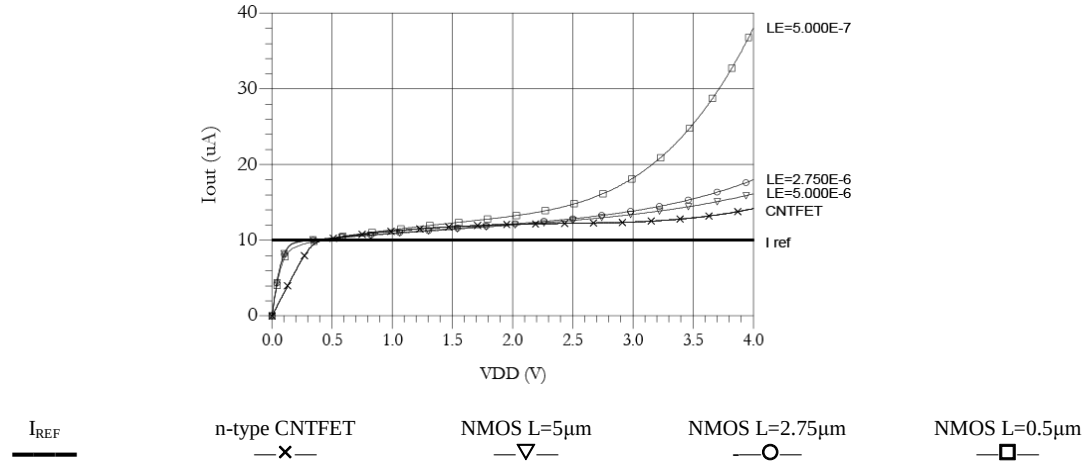
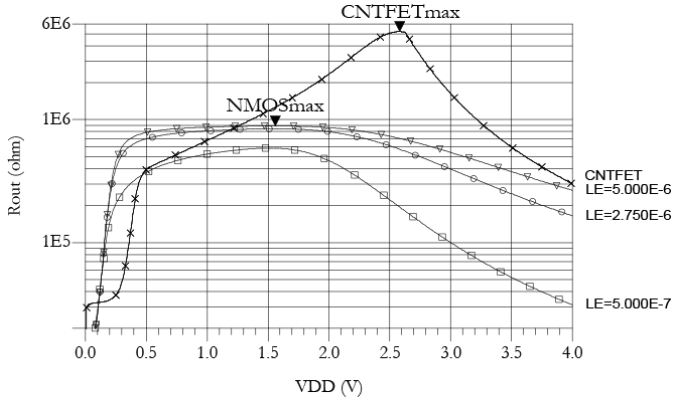


Figure 8. Reference current vs V_{DD} in a n-type basic current mirror.

The simulation underlines that n-type CNTFET works better then MOSFETs of larger size in current replication in a basic current mirror. However, NMOS shows a lower threshold voltage that allows to keep easier the device in saturation region, when current mirror function begins to operate[8].
Another feature we would to analyze is the output resistance R_{OUT} seen from the M2 drain to ground (ideal case is R_{OUT} tending to ∞). For the proposed mirror R_{OUT} is given by:

$$R_{out} = \frac{1+\lambda V_{DD}}{\lambda I_{out}} \cong \frac{1}{\lambda I_{out}} \tag{12}$$

where I_{OUT} in saturation region is given by Eq. (11). Therefore, R_{OUT} is a sensitive quantity to the variation of M2 drain-source voltage. In effect it exhibits its maximum value as long as I_{OUT} is maximally consistent with respect of V_{DD} changes.
The trend of R_{OUT} versus V_{DD} is shown in Fig. 9.



CNTFETmax
V_{DD} = 2.6 V, R_{OUT} = 5.2 MΩ
n-type CNTFET NMOS L=5μm

NMOSmax
V_{DD} = 1.6 V, R_{OUT} = 890 kΩ, L = 5 μm
NMOS L=2.75μm NMOS L=0.5μm

Figure 9. Output resistance of a n-type basic current mirror.

We notice that n-type CNTFET-based basic mirror behaves better than NMOS one because of the larger CNTFET small-signal output resistance seen from drain to source. A resistance value of 5.2 MΩ is achieved by n-CNTFET compared to the 890 kΩ of the longer NMOS proposed in simulation. Overall we observe that n-type CNTFET mirror obtained resistance exceeds about five times the performance related to MOS devices with channel length of about two orders of magnitude higher.
This simulation is repeated choosing pairs of NMOS with L = 5 μm, characterized by the best shown simulated performances, and changing the MOSFET device aspect ratio in order to increase channel width W, and MOSFET trans-conductance given by [1]:

$$g_m = \sqrt{2k'\frac{W}{L}|I_{out}|(1+\lambda V_{DD})} \tag{13}$$

where $k_n' = \mu_n C_{oss}'$ depends of the depth of the thin oxide. As Eq. (13) indicates, an increment of aspect ratio W/L corresponds to a slowly increment of the device trans-conductance. This means that for larger MOSFETs a lower driving source-gate voltage is allowed for achieve 10 μA of reference current, then the same for the replication in case of equal devices in mirror.
In Figs. 10, 11 and 12 we have reported the results of our simulations.
As we can easily see, NMOS current mirrors provide better performances in terms of current replication error and output resistance, for lower values of W/L. In spite of this analysis we can assume the n-type C-CNTFET behaviour in current mirror similar to behaviours of NMOS with channel length of the order of μm with a very low W/L.

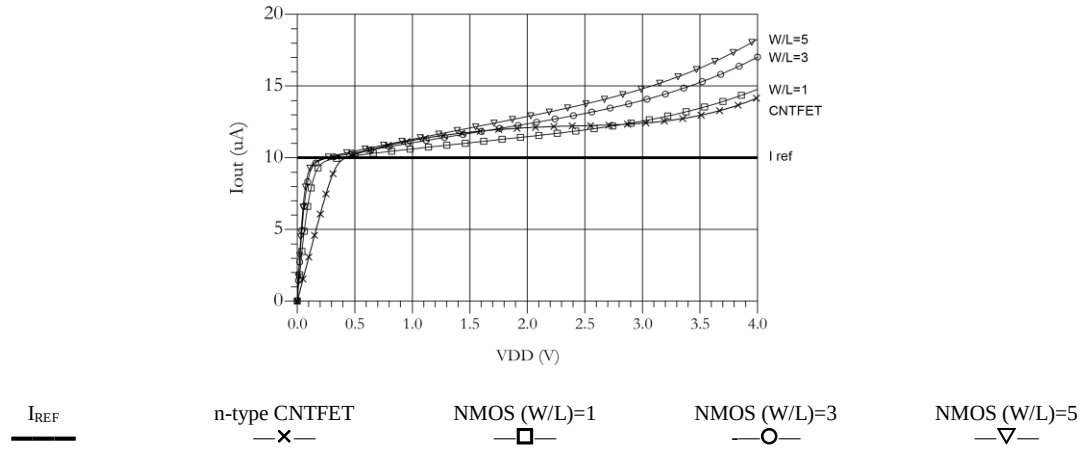


Figure 10. I_{OUT} vs V_{DD} in n-type basic current mirror for different W/L values.

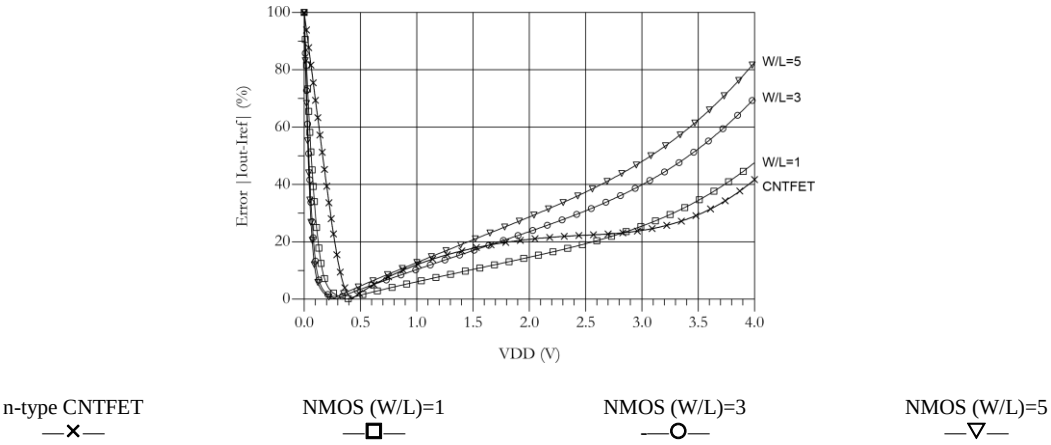


Figure 11. Relative error $|I_{OUT}-I_{REF}|$ vs V_{DD} in n-type basic current mirror for different W/L values.

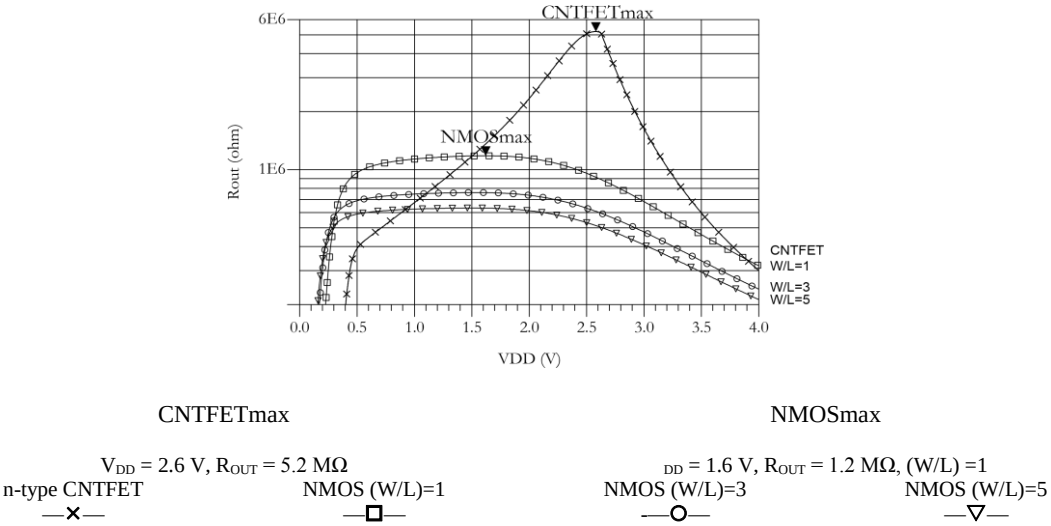


Figure 12. Output resistance of a n-type basic current mirror for different W/L values.

For the upcoming simulations we assume constant aspect ratio (W/L) = 2 to keep comparison with the previous simulation, involving the p-type configuration of basic current mirror shown in Fig. 13.

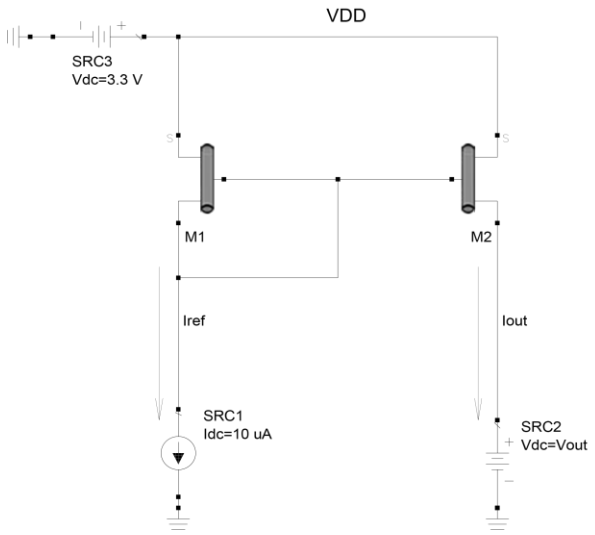


Figure 13. Schematic of the simulated basic current mirror with p-type C-CNTEFET.

Implementation of a current source with p-channel transistors needs the presence of a positive voltage supply for biasing both M1 and M2 in saturation region. Higher supply voltage of the circuit V_{DD} is pushed on to 3.3 V, and a reference current of 10 µA is provided.
Moreover the gate is taken to a constant potential and M2 lies in saturation region as long $V_{OUT} \leq V_{DD} - |V_T|$, maximum voltage to maintain M2 switched on.
The drain voltage of M2 represented by the V_{OUT} voltage supply is swept in order to evaluate output current replication. Similarly, the expected current value given by the general I-V characteristic of a p-FET device in saturation region, which is given by the relation [1]:

$$I_{out} = k'\left(V_{DD} - V_G - |V_T|\right)^2 \left(1 + \lambda V_{out}\right) \tag{14}$$

where λV_{OUT} term refers to channel length modulation, and V_{DD}-V_G is the driving voltage for p-type FET devices. Also in this case, if M1 is equal to M2 and M2 is on, mirror works properly.
Now the simulations are performed by replacing p-type C-CNTFETs with PMOS with different channel length L and constant (W/L) = 2 and the relative results are illustrated in Fig. 14.

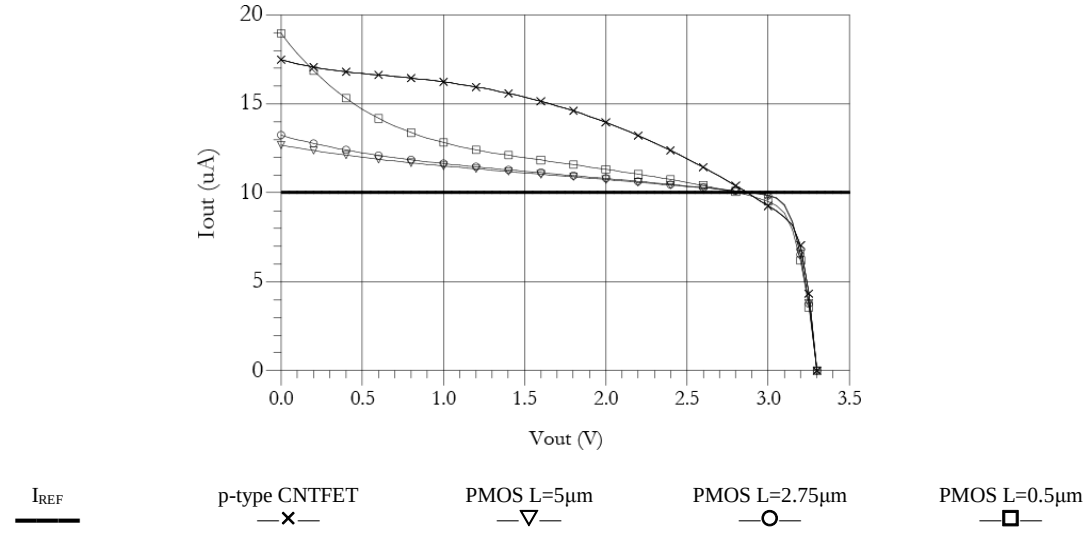


Figure 14. I_{OUT} vs V_{DD} in p-type basic current mirror for different W/L values.

We notice that p-type CNTFET-based current source badly outperform compared to the competitor, in same way as smaller p-channel MOSFET devices, as it is evident also from Fig. 15, in which the relative error in current replication is estimated.

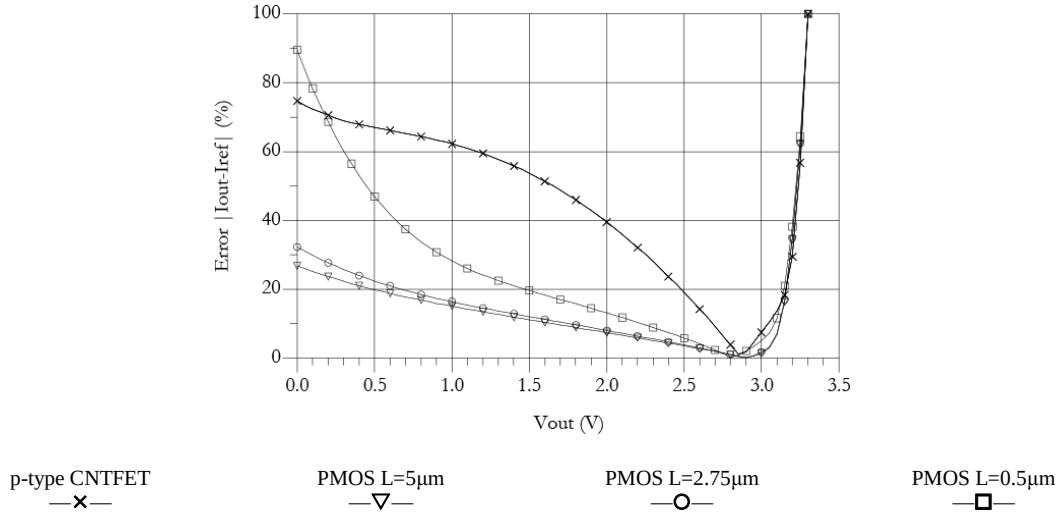


Figure 15. Relative error $|I_{OUT}-I_{REF}|$ vs V_{DD} in p-type basic current mirror for different W/L values.

As before, the output resistance R_{OUT} seen from the drain of M2 is simulated. The expected value is given by:

$$R_{out} = \frac{1+\lambda(V_{DD}-V_{out})}{\lambda I_{out}} \cong \frac{1}{\lambda I_{out}} \tag{15}$$

where I_{OUT} in saturation region is given by Eq. (14).
The relative plot is illustrated in Fig. 16.

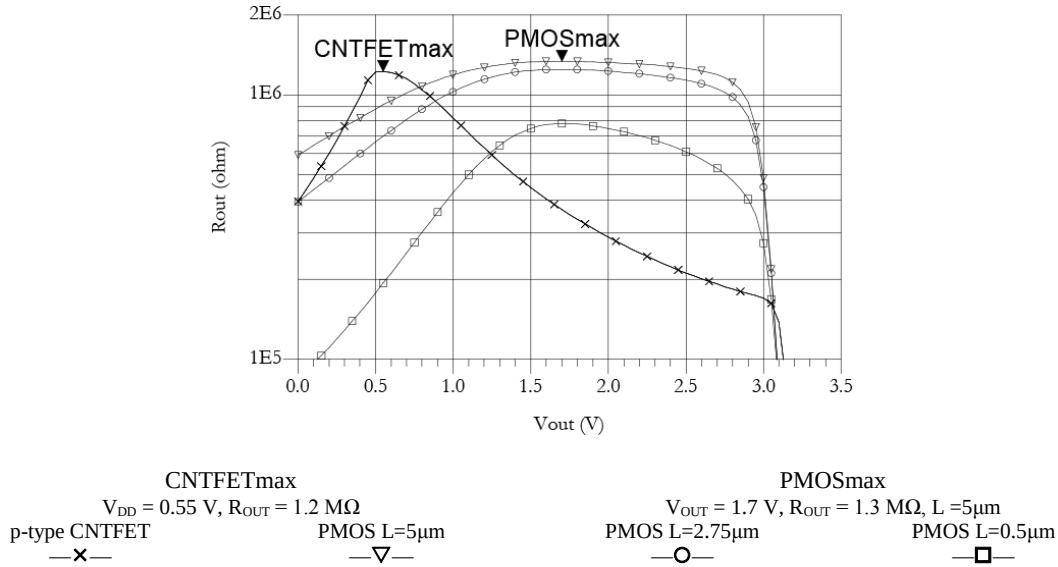


Figure 16. Output resistance of a p-type basic current mirror for different W/L values.

A resistance value of 1.2 MΩ is achieved by p-CNTFET compared to the 1.3 MΩ of the longer PMOS proposed in simulation.
We can consider the performance as comparable, so there is not an evident convenience in the implementation of p-type CNTFET current mirror after all, if not from a design requirement or constrain.

The simulations underline the following considerations:

- n-type CNTFET performances largely surpass NMOS outcomes when n-channel length does not exceed 5 μm in basic current mirror, because of output resistance exceeds about five times the performance related to NMOS devices with channel length of about two orders of magnitude higher;
- n-type CNTFET behaviour in current mirror is similar to behaviour of NMOS with channel length of the order of the μm with a very low aspect ratio;
- MOSFETs generally show a lower threshold voltage that allows to keep easier then CNTFETs the saturation region, when current mirror function begins to operate;
- performance in p-type basic current mirrors are comparable as long as p-channel length does not exceed 5 μm, so there is minor benefit in the implementation of p-type CNTFET current mirror.

IV. CONCLUSIONS AND FUTURE DEVELOPMENTS

In this paper we have implemented the semi-empirical compact model for CNTFETs already proposed by us to simulate some analogue circuits both in SPICE, using ABM library, and in Verilog-A. The obtained results have been the same in static simulations and comparable in dynamic simulations. However using Verilog-A the simulation run time has been much shorter and the software has been much more concise and clear than schemes using ABM blocks in SPICE.

Although SPICE has still an huge importance in the electronic design. since a great number of commercial devices are described by SPICE models and major chip producer distribute their simulation libraries for SPICE, we think that Verilog-A is an useful tool to help circuit designers to devise these very new nascent architectures, although its diffusion is still very limited and nowadays most of its libraries are dedicated to RF [14].

Moreover the design of current mirror circuitry allowed us to make a comparison between CNTFET and MOSFET technology. In particular we have considered basic current mirror, considering both n-type and p-type devices. For every simulation parameters of merit, such as relative error in reference current replication and small-signal output resistance, have been estimated in order to evaluate the role of CNTFET in place of the most widely used devices.

Another evidence has been given by the fact that the maximum benefits are achieved for different quiescent points between one technology and the other. In particular we have noticed that the quiescent point of CNTFET needs of a bias voltage slightly high for the correct operability due to the presence of a flat band voltage higher that increases the threshold voltage. Therefore power requirements slightly greater are needed.

Future work will involve the verification of the power requirements, the investigation of the behaviour of the circuit model used to provide a quantitative explanation of the phenomena highlighted in the simulations and the performance comparison through the electrical test on real devices.

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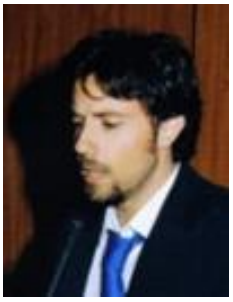

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