POWER ESTIMATION ANALYSIS FOR CMOS CELL STRUCTURES

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ABSTRACT

Increasing demand for portable electronics for computing and communication, as well as other applications, has necessitated longer battery life, lower weight, and lower power consumption. In order to satisfy these requirements, research activities focusing on low power/low voltage design techniques are underway. Since 'power' is now one of the design decision variables, the expanded design space required for low power has further increased the complexity of an already non-trivial task. Low power design basically involves two concomitant tasks: power estimation and analysis and power minimization. These tasks need to be carried out at each of the levels in the design hierarchy, namely, the behavioral, architectural, logic, circuit and physical levels. In this survey of the current state of the field, many of the salient power estimation and minimization techniques proposed for low power VLSI design are reviewed. In this paper comparison of power estimation of various basic CMOS cell structures on various technologies (TSMC 0.35um, TSMC 0.2um and TSMC 0.18um) is carried out. The research issues in order to make the low power design are also discussed in the paper. The paper is organized as follows: First, the sources of power dissipation in CMOS circuits and degrees of freedom in the low power design space are described in section-2. In section-3 various power minimization techniques are discussed. Designing of various CMOS cells and Simulation results are shown in section-4&5.Athe end of the paper conclusion is given. We have used IC Design studio, HEP2 module from Mentor Graphics to obtain the simulation for various analysis of power estimation.

KEYWORDS: *TSMC 0.12U, POWER ESTIMATION, CMOS*

I. INTRODUCTION

In the past, the major concerns of the VLSI designer were area, performance, cost and reliability; power considerations were mostly of only secondary importance. In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed. Several factors have contributed to this trend. Portable computing and communication devices demand high-speed computation and complex functionality with low power consumption. Heat generation in high-end Computer products limit the feasible packing and performance of VLSI circuits and increases the packaging and cooling costs. Circuit and device reliability deteriorate with increased heat dissipation, and thus the die temperature. Heat pumped into the rooms, the electricity consumed and the office noise diminishes with low power LSI chipset. The goal of this paper is to provide background of low power design methodologies and then compare the power estimation of CMOS cell using scaling and reducing the VDD at various technology level.

II. SOURCES OF POWER DISSIPATION

CMOS is, by far, the most common technology used for manufacturing digital ICs. There are 3 major sources of power dissipation in a CMOS circuit [9]:

$$P = P_{Switching} + P_{Short\text{-}Circuit} + P_{Leakage}$$

$P_{Switching}$, called switching power, is due to charging and discharging capacitors driven by the circuit. $P_{Short\text{-}Circuit}$, called short-circuit power, is caused by the short circuit currents that arise when pairs of PMOS/NMOS transistors are conducting simultaneously. $P_{Leakage}$, called leakage power, originates from substrate injection and subthreshold effects. For older technologies (0.8 µm and above), PSwitching was predominant. For deep-submicron processes, $P_{Leakage}$ becomes more important. Design for low-power implies the ability to reduce all three components of power consumption in CMOS circuits during the development of a low power electronic product. The trend of process scaling for CMOS technology has made subthreshold leakage reduction a growing concern for submicron circuit designers.

III. LOW POWER CIRCUIT TECHNIQUES

3.1 Scaling the Supply Voltage

VLSI technology scaling has evolved at an amazingly fast pace for the last thirty years. Minimum device size has kept shrinking by a factor k = 0.7 per technology generation. The most widely known power-reduction technique, known as power-driven voltage scaling, depending on the relative weight of performance with respect to power consumption constraints, different voltage levels can be adopted. It is important to observe, however, that transistor speed does not depend on supply voltage VDD alone, but on the gate overdrive, namely the difference between voltage supply and device threshold voltage (VDD – VT). Accurate modeling of MOS transistor currents is paramount for achieving acceptable scaled VDD and VT values.
An electronic device's overall power consumption can be represented by:

$$P_{TOT}=\alpha C_{TOT}V_{DD}^{2}f + V_{DD}I_{OFF};\ \text{where } I_{OFF}=I_{o}e^{(-qVTH/nkT)} \quad (1)$$

The first term in Equation 1 represents dynamic or "switching" power, while the second term represents static power—primarily due to leakage currents. (The short-circuit power, which forms less than 5% of the total power, is not included.) As a result of scaling over the years, the dynamic power has remained almost constant (see Figure 1), so increases in switching frequency (α), clock frequency (f) and total capacitance (CTOT) have been largely offset by the supply voltage (VDD). A reduction in supply voltage helps to reduce power but, on the flipside, it limits the clock frequency. Additionally, a reduction in supply voltage reduces the saturation current through the MOSFET, thereby cutting speed and performance. Hence, the supply voltage plays an important role in the speed vs. power tradeoff. To counter this reduction in saturation current, threshold voltage (V_{TH}) has also scaled down. This has led to a tremendous surge in sub-threshold leakage current (I_{OFF}) and static power; especially in the deep submicron process technologies (see Figure 1). Minimizing this is expected to be a significant challenge for future low-power designs. Table 1 shows the effect of scaling on various parameters

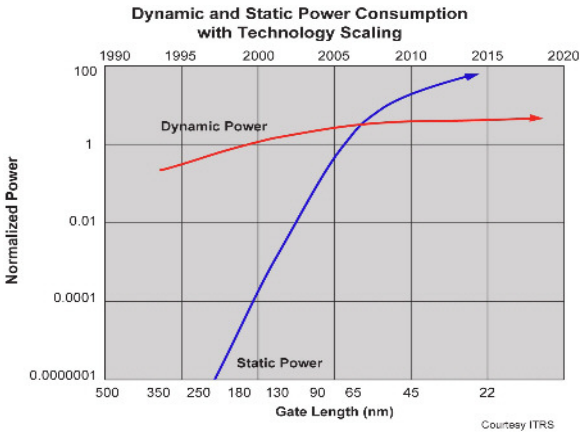

Figure 1[7]: Scaling effect on dynamic power

Table 1[7]: Effects of scaling on various parameters

Parameter	Relation	Full Scaling	General Scaling
W, L, tox	–	1/S	1/S
V_{DD}, V_{TH}	–	1/S	1/U
Area	WL	$1/S^2$	$1/S^2$
Cox	1/tox	S	S
C_L	CoxWL	1/S	1/S
I_{DSAT}	$Cox(W/L)V^2$	1/S	S/U^2
Intrinsic Delay (t_P)	CLV/I_{DSAT}	1/S	U/S^2
Avg. Power (P_{AV})	CLV^2/t_P	$1/S^2$	S/U^3
Power-Delay Product	CLV^2	$1/S^3$	$1/SU^2$

Full Scaling = Dimension and voltage scales by a factor "S" (S>0)
General Scaling = Dimension and voltage scales with different factors

3.2 Power Distribution

As the supply voltage is reduced, the noise margins are diminished, thus, small voltage drop in the power distribution may have a relatively big impact on the circuit speed. Careful power distribution is thus becoming more important at lower supply voltages. In [57], a technique for concurrent topology design and wire sizing in power distribution networks is presented. The objective is to minimize the layout area while limiting the average current density to avoid electro migration- induced reliability problems and large resistive voltage drops. This technique is based on the observation that when two sinks do not draw currents at the same time, narrow wires can be used for power distribution to those sinks, thus reducing the layout area.

3.3 Reduce Output Voltage Swing

For a further power reduction the output voltage swing can be reduce to a value less than a supply voltage. Since the delay is proportional to the signal swing (Vswing), reducing the signal swing linearly decreases the delay, as well as, for constant I_{avg} [32].To limit the swing of any static or dynamic CMOS circuit that has a rail to rail swing, extra circuitry is required as shown in fig. 2 [33]. This extra circuitry adds parasitic capacitance that add to the total effective capacitance being switched. However, the total energy is reduced because the voltage swing has been reduced. As long as the reduction in voltage swing is greater than the increase in capacitance, the energy and power will be reduced [33].

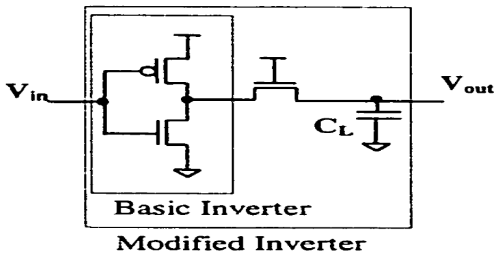

Fig.2 [33]: A reduced swing CMOS inverter

3.4 Reducing the physical Capacitance

Digital circuits have three types of capacitance: gate capacitance, diffusion capacitance and interconnect capacitance. If all the three components are scaled down as well by the same factor, then the net power dissipation is scaled down as well. Gate and diffusion capacitance are fixed during the cell design, whereas Intercell and global interconnect capacitances can be controlled by the CAD tools performing the global routing. Physical capacitance mainly reduces by the transistor sizing[42].

3.5 Reducing the switching frequency

Reducing the number of "0"to '1" power dissipating transitions minimize the switching power dissipation of the gate .Switching frequency may be reduced on several levels in the design process beginning from circuit level to the architectural level [23]. There are several logic styles to design with. Some of these styles are: Static CMOS, CPL, MCML, and a variety of dynamic logic styles. Generally, most logic styles perform delay power tradeoffs, but not always in proportional amounts. The best style is that which minimize power dissipation given a constant throughput.

IV. DESIGNING AND POWER ANALYSIS OF DIFFERENT CMOS CELLS

This section describes the design of various CMOS cell using technology scaling and reducing the supply voltage using TSMC 0.35u, TSMC 0.2u and TSMC 0.18u for simulation. First the basic CMOS inverter with a values of *W/L* for PMOS = (1.2μm/0.18 μm) and *W/L* for NMOS = (0.27 μm/0.18 μm) is analyzed using MENTOR GRAPHICS, IC DESIGN STUDIO, HEP2 software in detail and then, based on this analysis, the NAND and the NOR gates are designed and after that other circuits can also be designed by calculating the values of *W/L* at scaled Vdd.

4.1 Result for TSMC 0.18u technology with Vdd= 2v, shows power dissipation 129.54p watts for CMOS Inverter

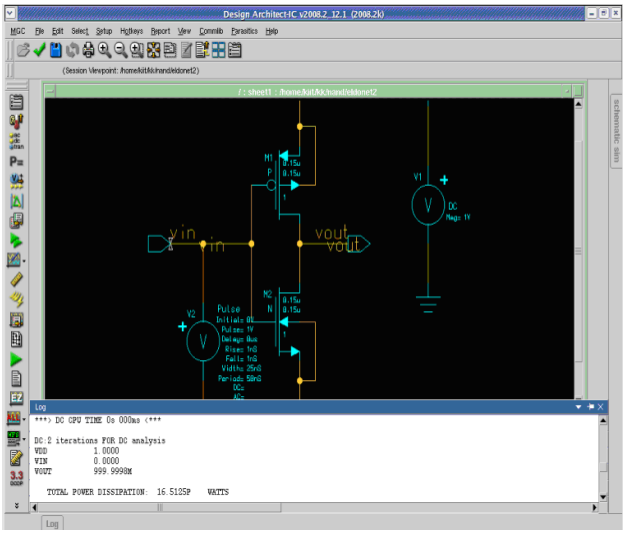

Fig. 3.1 Schematic of Inverter of 0.18u, 2V

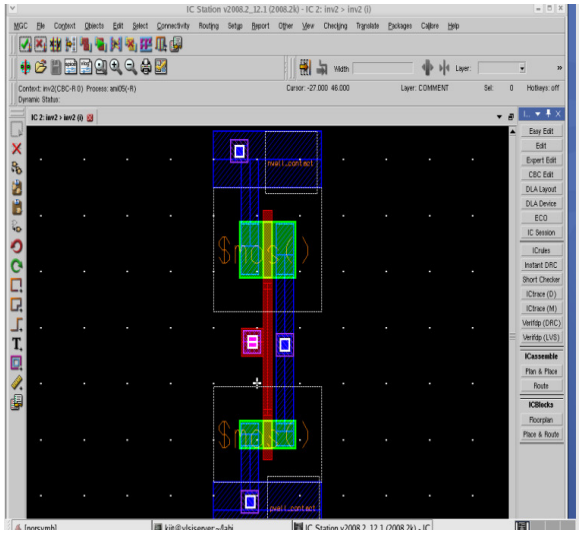

Fig.3.2 Layout of Inverter

4.2 Results for TSMC 0.18u technology with Vdd= 1v, shows power dissipation 16.5125p watts for CMOS Inverter

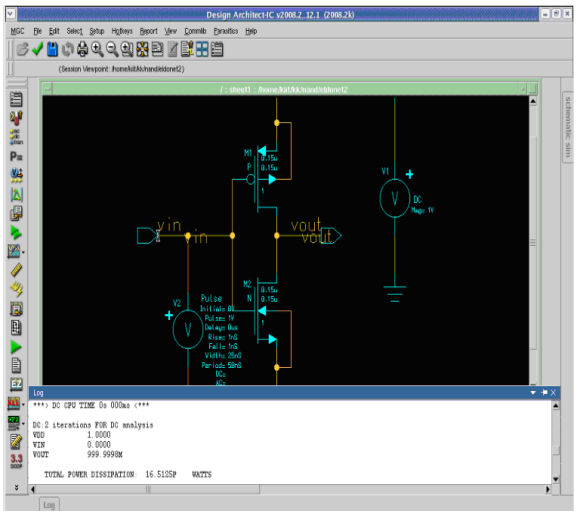

Fig. 4.1 Schematic of Inverter of 0.18 u of 1V

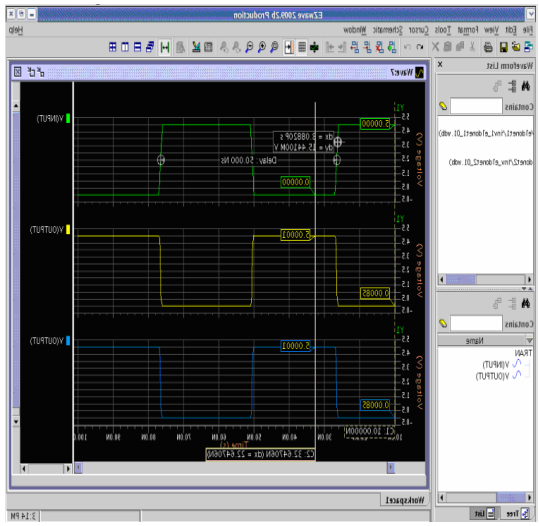

Fig. 4.2 Simulation of Inverter of 0.18 u of 1V

4.3 Results for 0.25u technology with Vdd= 1v, shows power dissipation 20.8509p watts for CMOS Inverter

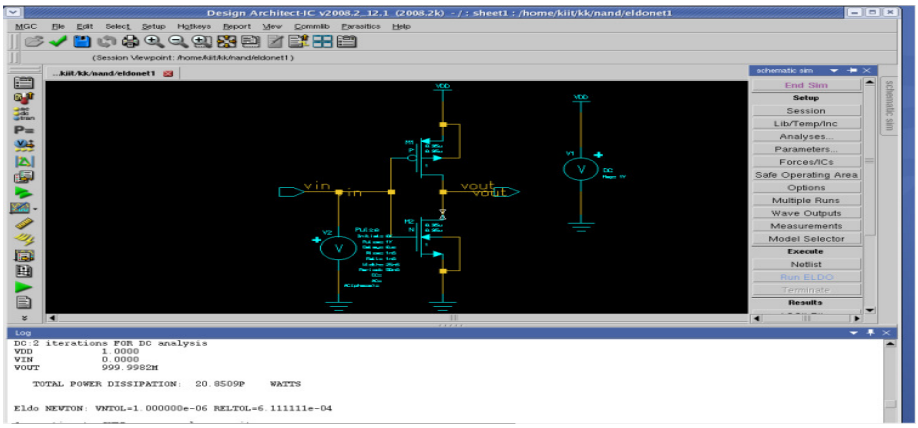

Fig. 5 Schematic of Inverter of 0.25u of 1V

4.4 Results for 0.35u technology with Vdd= 1v , shows power dissipation 38.1579p watts for CMOS Inverter

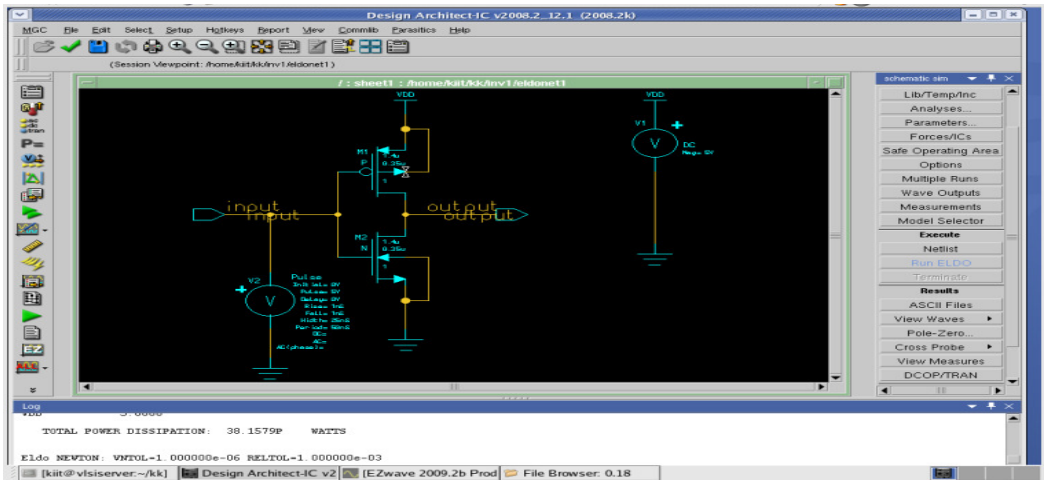

Fig. 6 Schematic of Inverter of 0.35u of 1V

V. DESIGN, LAYOUT AND SIMULATION OF DIFFERENT CMOS CIRCUITS

5.1 Two input CMOS NAND Gate

Results for 0.18u technology with Vdd= 1V , shows power dissipation 2.963p watts for CMOS NAND gate

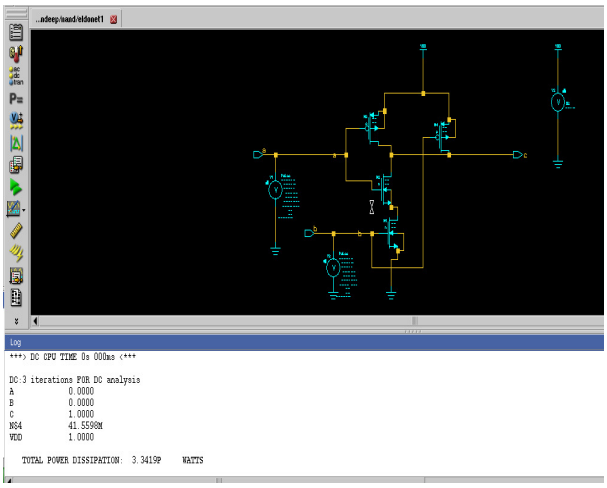

Fig. 6.1 Schematic of CMOS NAND of 0.18u of 1V

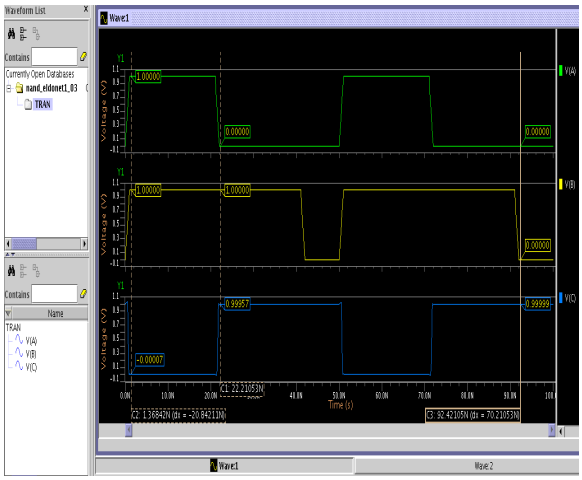

Fig. 6.2 Simulation of CMOS NAND of 0.18u of 1V

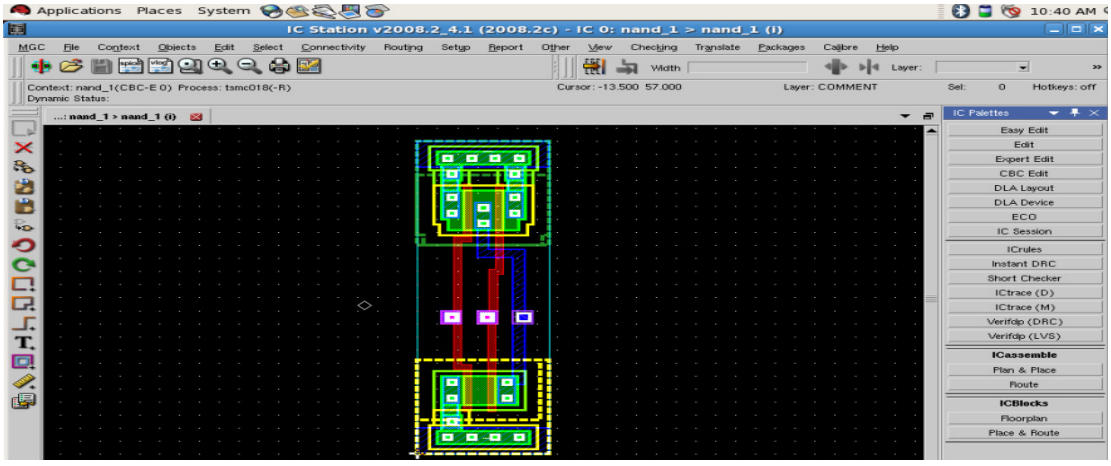

Fig. 6.3 Layout of CMOS NAND of 0.18u of 1V

5.2 Two input CMOS NOR Gate

Results for 0.18u technology with Vdd= 1V, shows power dissipation 33.12p watts for CMOS NOR gate

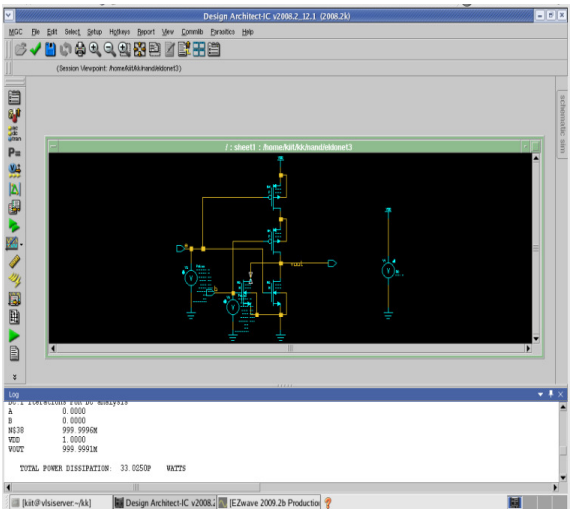

Fig. 7.1 Schematic of CMOS NOR of 0.18u of 1V

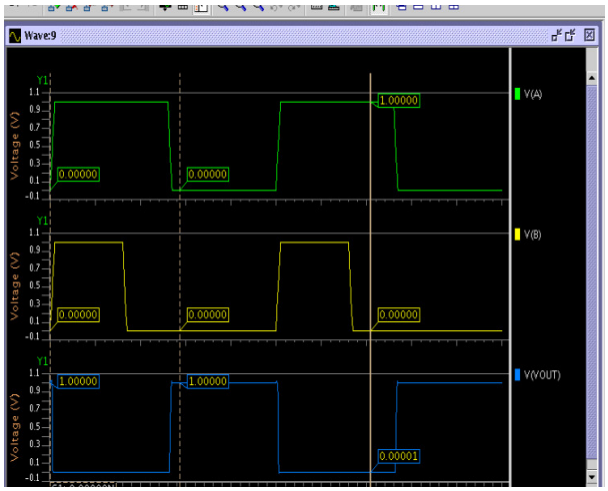

Fig. 7.2 Simulation of CMOS NOR of 0.18u of 1V

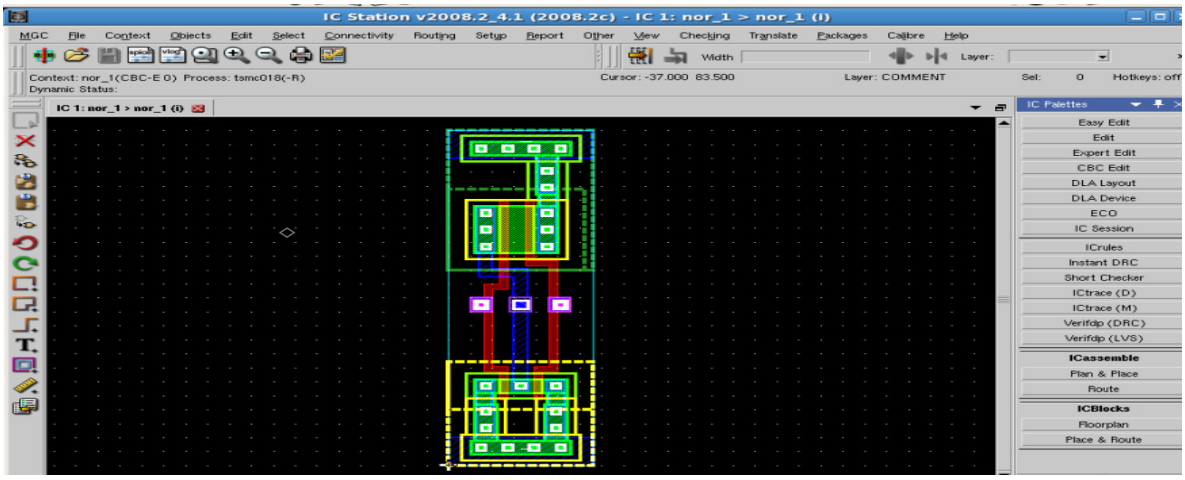

Fig. 7.3 Layout of CMOS NOR of 0.18u of 1V

Table 2: Power dissipation in Different CMOS Cell

CMOS Cell	Power Dissipation at various technology at 1V Vdd(watts)		
	TSMC 0.35u	TSMC 0.2u	TSMC 0.18u
CMOS INVERTER	38.1579p	20.8509p	16.5125p
CMOS NAND Gate	14.959p	3.9799p	2.963p
CMOS NOR Gate	45.035p	36.032p	33.250p

VI. CONCLUSION

Based on scaling various analysis of power estimation have been done and conclude that by reducing the power supply and technology scaling significant power reduction is take place. Return-On-Investment approach is through designing for low power. Unfortunately designing for low power adds another dimension to the already complex design problem; the design has to be optimized for Power as well as Performance and Area. Future Challenges ahead us are:-

- High-speed & Low power design is a requirement for many applications
- A new way of THINKING to simultaneously achieve both!!!

- Low power impacts in the cost, size, weight, performance, and reliability.
- Variable Vdd and Vt is a trend
- CAD tools high level power estimation and management

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