AREA MINIMIZATION OF CARRY SELECT ADDER USING BOOLEAN ALGEBRA

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ABSTRACT
The modern electronic devices require a less expensive, compact and power saving technology. Computational units like multipliers and adders are some vital components of those systems working with this target. Among the adders available and used Carry select adders are the fastest adders as designed by O.J.Bedrij. In this adder Dual ripple carry adders - one for CIN = 0 and other for CIN = 1 are used. To reduce Propagation delay of generated carry, Carry look ahead adders are used instead of ripple carry adders. To enhance the performance the size of the adder is reduced using Binary to Excess 1 instead of RCA for CIN = 1. In this paper the size of the Adder is proposed to be further reduced by Boolean algebraic techniques.

KEYWORDS: *Ripple carry adder, Carry looks ahead adder, Binary to Excess 1, Boolean algebra.*

I. INTRODUCTION

The demands of faster devices has culminated in fine tuning the design in system level, architectural, register level and circuit level. Much of the design concentrates on architectural level manipulations of arithmetic algorithms [1], [4], [6], and [14].

Arithmetic units form vital components of systems like communication, signal analysis, image processing, numerical analysis, etc. [16]. Particularly adders play a major role in all sorts of applications such as ALU, multiplier and accumulator, memory applications and also in modern communication such as DWT, DCT, Transmitters and Receivers, etc.

Parallel adders are of different types- Ripple Carry Adder, Carry Look ahead Adder, Manchester Carry chain Adder, 3:2 Lossy Compressors, and Carry Select Adders with half adder, full adders and logic gates as basic units .Of these Carry Select Adders which are widely used.[2],[3]. In [12] instead of duplicating the ripple carry adder unit a binary excess -1 convertor circuit replaces the RCA with Cin=1.

I-Chyn Wey, Cheng-Chen Ho, Yi-Sheng Lin, and Chien-Chang Peng use sharing of Boolean logic term effectively to minimize the area of ripple carry adders [13]. In this paper it is proposed to minimize the area by exploiting the benefits of techniques proposed above [12] & [13].

In this paper existing adder circuits is dealt in section II, Proposed technique in Section III, and then results of experiments and conclusions at the last.

II. EXISTING ADDER CIRCUITS

Some of the widely used adders are Ripple carry adder, Carry skip adder, carry free adder, carry save adder, carry look ahead adders and carry select adders. In a carry-ripple adder the carry-out signal of every adder cell ripples from LSB adder to the MSB. In a carry-skip adder the carry signal skips a block if all the corresponding propagate signals of this block are equal to 1. In a carry look-ahead adder the carry-in signals are predicted with a fast carry look-ahead unit resulting in large area overhead. In a carry-free adder no carry-signal is propagated but a unique number representation is used. [7]

2.1 Carry select adders

Carry select adder is a fast adder which is used in digital communication and Memory Architectures. The Carry of one ripple carry adder will be '0' and another will be '1'.Here the output sum and carry is identified by the 2 to 1 multiplexers .The control signal of the multiplexer is carry $C_{IN.}$

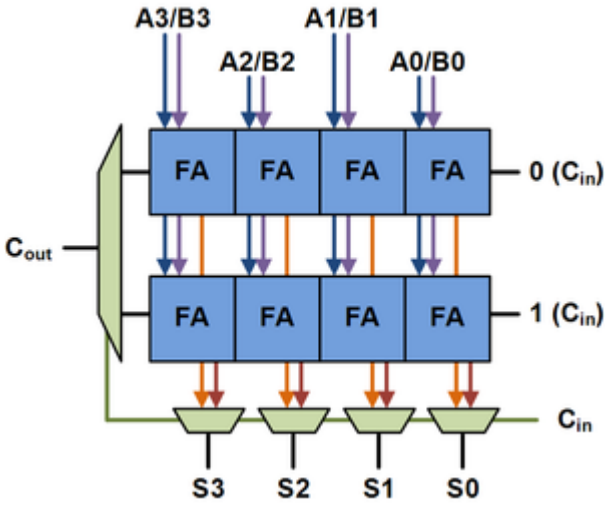

Fig 1: Basic Carry Select adder circuit

The carry select adders are divided into two types: Uniform Sized Adders and Variable Sized Adders. If the bit length is equally divided it is called Uniform Sized adders. It is also called Linear Carry select adder. In Variable Sized Adders the bit length are unequally divided as given in Fig.2. It is also called SQRT carry select adder (CSA).

Normally the CSLA is designed with the Dual Ripple Carry Adders with the carry being '1' and '0'.Here instead of having Dual ripple carry we are having only single Ripple carry Adder while the Binary to Excess one converter is connected instead of RCA with Carry '1'.[8]-[12].

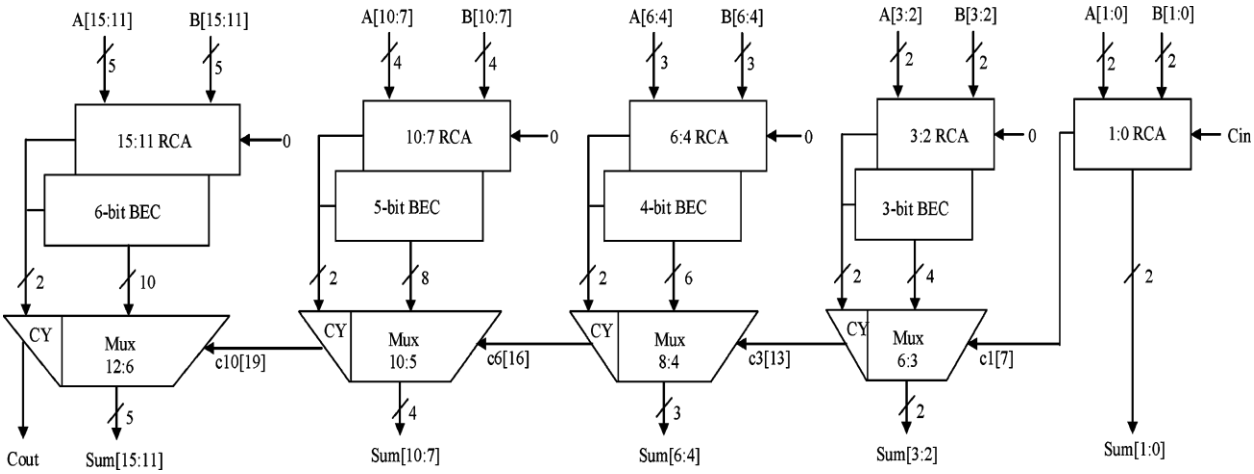

Figure 2. SQRT CSA Circuit.

2.2 Binary To Excess One Converter (BEC)

Binary to Excess one circuit is used for incrementing the input by one. So this circuit very well replaces the RCA with C_{in}=1.Here the gates are NOT, AND and XOR. Let us see the logic diagram and logic Equations of BEC converter.

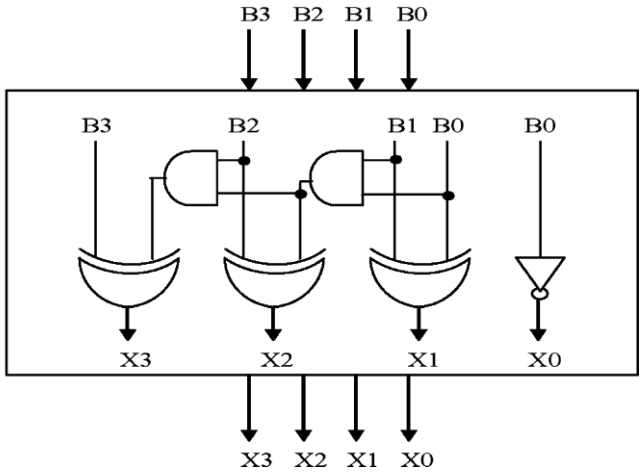

Figure 3. Binary To Excess One Converter

Logic equation of BEC is as below:

X_0= NOT(B_0) ;
X_1=B_0 XOR B_1 ;
X_2=B_2 XOR (B_0ANDB_1);
X_3=B_3 XOR (B_0 AND B_1 AND B_2);

III. PROPOSED SYSTEM

For Area Minimization the Number of Gates should be minimized. It can be achieved by altering the Full Adder. Let us see the Truth table of Full Adder and its logic diagram. The proposed System is designed with the help of NOT, OR, XOR and AND gates. Here the size of the adder is again reduced by Boolean algebra so that the gate counts are reduced. When the gate counts are reduced automatically the power and area are also reduced

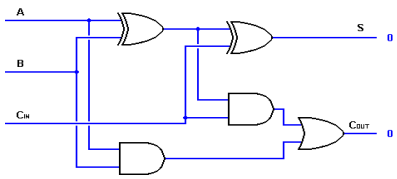

Figure 4. Logic Diagram Of Full Adder

Table.1 Truth Table

C_{IN}	A	B	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

Logical equations for full adder are as below:

Sum = A XOR B XOR C_{IN}

Carry = (A.B) + C_{IN} (A+B)

Minimized Logical equations for full adder:

For C_{IN} = 0

S_V = A XOR B

C_V =A.B

For C_{IN} = 1

S_K =NOT S_V

C_K =A+B

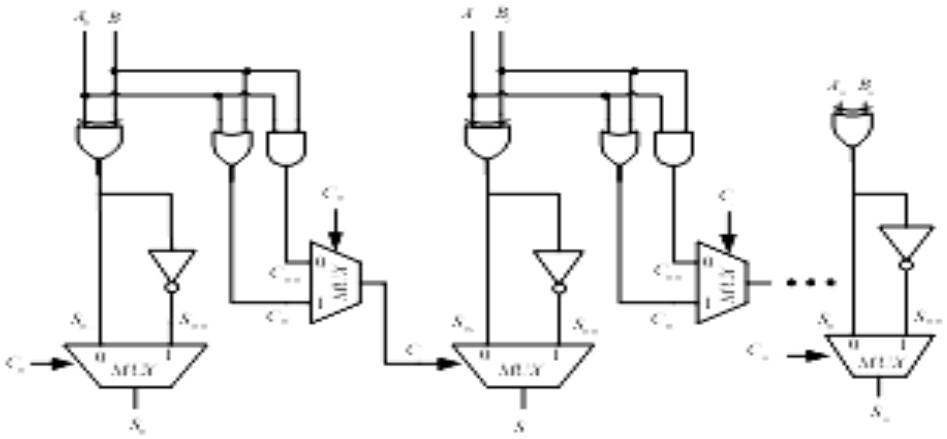

Figure 5. Proposed System

The logic for the required carry is chosen using 2:1 mux circuits. This results in reduced gate numbers than existing carry select adders. Hence it has the area minimized and operating computational speed is more.

IV. RESULTS AND CONCLUSION

The circuit was implemented using Xilinx Navigator 9.2 and simulations were carried out using ModelSim with VHDL. The area and static power consumed by the circuit depends only on gate counts. This is shown as the comparison of the gate counts versus bit length of the inputs in the graph. It is simulated for a basic ripple carry adder, a Carry select adder with binary to excess one convertor and with the proposed adder with Boolean logic minimization.

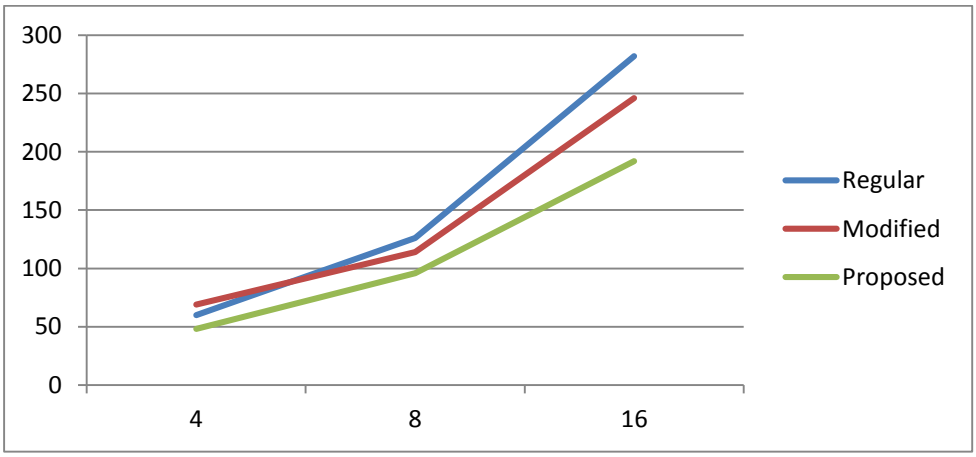

Figure 6 : Gate count Vs bit length

The table shows considerable reduction in gate counts with proposed system compared with basic adder. The area minimization is confirmed from the utilization summary of uniform CSA

Table.2 Utilization summary of CSA with BEC system

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	41	1,920	2%
Logic Distribution			
Number of occupied Slices	26	960	2%
Number of Slices containing only related logic	26	26	100%
Number of Slices containing unrelated logic	0	26	0%
Total Number of 4 input LUTs	41	1,920	2%
Number of bonded IOBs	50	108	46%
Total equivalent gate count for design	246		
Additional JTAG gate count for IOBs	2,400		

Table.3 Utilization summary of Proposed system

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	32	4,896	1%	
Logic Distribution				
Number of occupied Slices	24	2,448	1%	
Number of Slices containing only related logic	24	24	100%	
Number of Slices containing unrelated logic	0	24	0%	
Total Number of 4 input LUTs	32	4,896	1%	
Number of bonded IOBs	50	172	29%	
Total equivalent gate count for design	192			
Additional JTAG gate count for IOBs	2,400			

Table 4. Gate Counts For Various Adders

Type of adder	**Length of input words**		
	4 bit	**8 bit**	**16 bit**
Regular	60	126	282
Modified	69	114	246
Proposed	48	96	192

From these results it is concluded that the area is being minimized in Carry select adder successfully. Further computational speedup may be achieved by suitable algorithmic manipulations. Low power constraints may be realized using techniques like number representations of input, idle mode of inactive units etc.[5], [7].

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