MODELING AND DESIGN OF ENERGY EFFICIENT SRAM CELL FOR EMBEDDED MEMORY ARCHITECTURE

G. Saiprakash, S. Rajendar
Department of Electronics and Communication Engineering,
Vardhaman College of Engineering (Autonomous), Hyderabad, India

ABSTRACT
In this paper, a new adiabatic static random access memory (SRAM) is presented by using multi-threshold voltage (multi-V_t) technique. The multi-V_t transistors are used to reduce the power while maintaining speed. It has been shown that the energy consumption of the proposed adiabatic SRAM is lower than the conventional SRAM. All the circuits in this paper are designed and simulated using Cadence® Virtuoso® Design Environment. Generic Process Design Kit (GPDK) 180nm, 90nm and 45nm technology files are used to get the transistor models. The power reduction of the proposed adiabatic SRAM is 22% better than conventional SRAM in 45nm technology.

KEYWORDS: *SRAM, Adiabatic Logic, Average Power Dissipation, Body Bias, Multi-V_t.*

I. INTRODUCTION

The technology scaling to deep submicron feature size and the increasing density of the transistors in integrated circuits (ICs) has encouraged in the research in low power and robust memory cell designs. Portable devices with limited battery-life require low standby power processors and memory. Often, embedded static random access memory (SRAM) arrays can be the dominant part of the whole static power consumption and also occupy large chip area, thus minimization of memory power is a crucial area of concern for today's IC designers [1].

Energy loss is reduced by limiting voltage differences across conducting devices. This is accomplished through the use of time-varying voltage waveforms. This is also called adiabatic charging technique. The SRAM working purely on adiabatic charging principles needs multiple phase power clocks. The design of the SRAM circuit is complex and not same as the design of the conventional SRAM, but there is huge saving in energy during writing as well as reading in the design of the SRAM [2]. To overcome the design complexity and latency of complete adiabatic SRAMs, SRAMs that make use of the adiabatic charging technique partially have been designed.

Based on whether adiabatic charging is applied to only power supply line or ground line or bit lines and word lines or only bit lines, there are many types of adiabatic SRAMs. High resistivity switches are also used to vary the power supply voltage slowly [3]-[4].

Adiabatic (Energy recovery) logic is a new promising approach because they are able to break the lower limit of the energy dissipation in static CMOS which amounts to $\frac{1}{2}CV_{dd}^2$. Adiabatic circuits achieve low energy dissipation by recycling the energy stored on their capacitors instead of dissipated as heat [5].

In this paper, a novel low power adiabatic SRAM with multi-V_t is proposed. From the simulation results, it has been shown that the energy consumption of the proposed adiabatic SRAM is lower than conventional SRAM.

This paper is organized as follows. The adiabatic logic overview is presented in section 2. The operation of conventional 6T SRAM, 9T SRAM and adiabatic SRAM is presented in section 3. Adiabatic SRAM with body bias and proposed SRAM with multi-V_t is presented in section 4.

Average power dissipation, delay and power-delay-product (PDP) of various SRAM cells are compared in Section 5. Finally, some conclusions are formulated in section 6.

II. ADIABATIC LOGIC OVERVIEW

Adiabatic is basically defined in thermodynamic principle of the state change with no loss or gain of heat. This adiabatic principle is explained with the help of switching activity done in an electrical circuit [6].

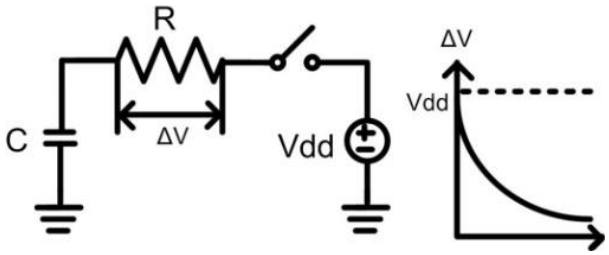


Figure 1. RC network with switch

Figure 1.shows the energy dissipation during a switching transition in the conventional CMOS circuit. The circuit shows the transition of the switch from LOW to HIGH which as a result the capacitor charges and discharges. When the switch is open the V_{dd} supply is not connected to the capacitor hence the capacitor is not charged. When the switch is closed, voltage V_{dd} is applied and current start flowing through R, this as a result charges the capacitor to voltage V_{dd}. The energy taken from the power supply is C.V_{dd}^2, but half of that $\frac{1}{2}$C.V_{dd}^2 is stored in C and the rest half is dissipated in R.

Now, consider the circuit and current waveform shown in Figure 2. Here notice that, instead of using a fixed power supply as in the previous case we use a time varying power supply. By this slow transition of the supply voltage the charging and discharging time of the capacitor is greatly increased [7].

As it is well known that the energy loss during charging and discharging is given by the following formula.

$$E = \frac{RC}{T} C.V_{dd}^2 \qquad (1)$$

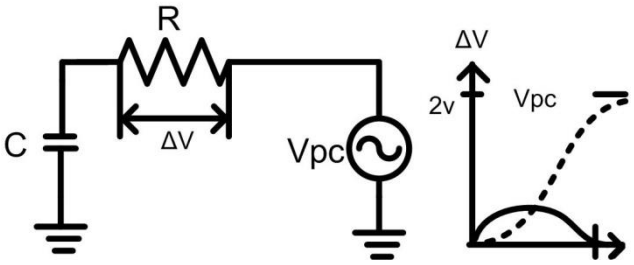


Figure 2. Adiabatic logic with sinusoidal power supply

Where, *R* = Resistance
C = Load capacitance
T = Charging and discharging time
V_{dd} = Supply voltage

From the equation (1) it is clear that, as the charging time of the capacitor is increased the energy loss in the circuit is reduced. This is the reason that here a time varying power supply is used instead of a fixed power supply [8].

III. CONVENTIONAL SRAM CELLS

SRAM is a volatile memory and can hold data as long as power is applied. There are three different modes they are reading mode, writing mode and hold mode [9].

A typical SRAM uses six MOSFETs to store each bit as shown in Figure 3. Each bit in an SRAM is stored on four transistors, P1-P2 and N1-N2 that form two cross coupled inverters. This storage cell has two stable states which are used to denote "0" and "1". The memory stores data in complimentary values, out1 and out2. Two additional transistors, called access transistors N3, N4 serve to control the access to the storage cell during read and write operations. In a 6T SRAM cell, in a single clock cycle either read or write operation is possible [10].

In this control signal is denoted by WL i.e. word line which control whether the bit line is to connect with the SRAM cell or not. The data for both read and write operation is transferred through the BL and BLB [11]. It is not necessary to have two bit lines, both the signal is complementary to each other and it improves noise margin. Hold mode is performed when the word line is low. Then the SRAM is in hold mode and it will hold the data into the latch.

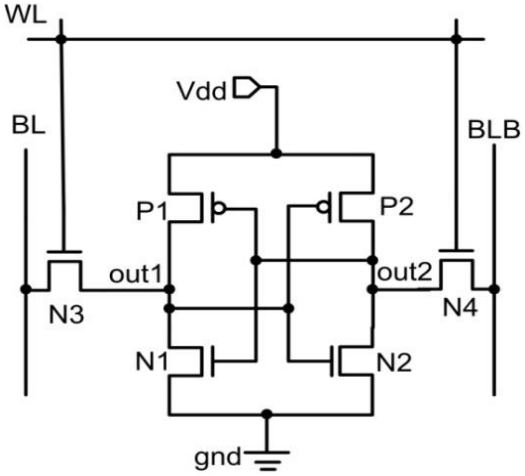


Figure 3. Conventional 6T SRAM Cell

The schematic of the 9T SRAM cell is shown in Figure 4. The upper sub-circuit of the new memory cell is essentially a 6T SRAM cell with minimum sized devices. The two write access transistors (N3 and N4) are controlled by a write signal (WR). The data is stored within this upper memory sub-circuit. The lower sub-circuit of the new cell is composed of the bit-line access transistors (N5 and N6) and the read access transistor (N7). The operations of N5 and N6 are controlled by the data stored in the cell. N7 is controlled by a separate read signal (RD) [12].

During a write operation, WR signal transitions high while RD is maintained low, as shown in Figure 4. N7 is cut off. The two write access transistors N3 and N4 are turned ON. In order to write a "0" to out1, BL and BLB are discharged and charged, respectively. A "0" is forced into the SRAM cell through N3. Alternatively, for writing a "0" to out2, BL and BLB are charged and discharged, respectively. A "0" is forced onto out2 through N4 [14].

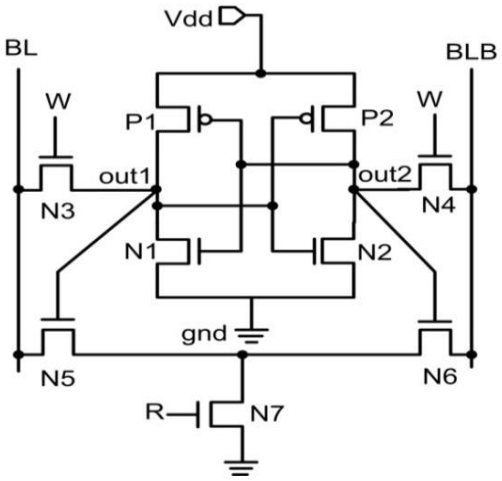


Figure 4. 9T SRAM Cell

During a read operation, RD signal transitions high while WR is maintained low, as illustrated in Figure 4. The read access transistor N7 is activated. Provided that out1 stores "1", BL is discharged through N5 and N7. Alternatively, provided that out2 stores "1", the complementary bitline (BLB) is discharged through N6 and N7. Since N3 and N4 are cut off, the storage nodes out1 and out2 are completely isolated from the bit lines during a read operation.

The adiabatic SRAM is shown in Figure 5. The adiabatic SRAM cell having five NMOS and four PMOS transistor. In which two NMOS transistor and two PMOS transistors are used as access circuit current and two NMOS transistor and two PMOS transistor are used in back to back connect inverters [15].

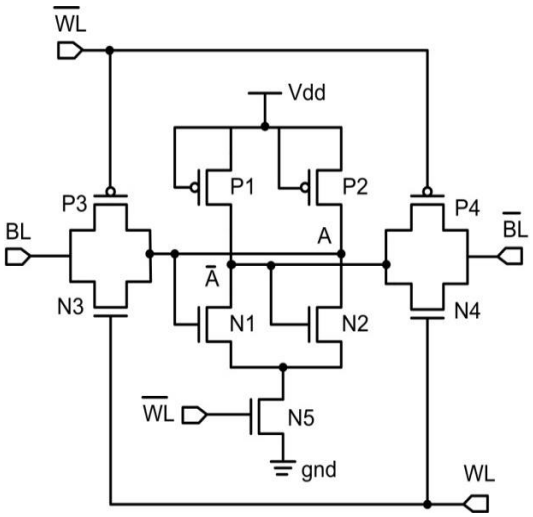


Figure 5. Adiabatic SRAM

The write mode of the adiabatic SRAM is as follows. At the first phase, when WL is high and $\overline{WL}$ is low level, MOS transistors: N3, N4, P3, and P4 are ON. Hence, the output node A and $\overline{A}$ is possible to change the write mode, and then N5 is OFF in order to reduce the energy dissipation in the elementary cell. In the second phase, adiabatic signal line BL and $\overline{BL}$ are on-state, and then the data write on A and $\overline{A}$. Finally, when WL and $\overline{WL}$ are low and high state respectively, MOS transistors N3, N4, P3 and P4 become all OFF, and then N5 transistor becomes ON. As a result, data is in the hold state in the elementary cell [16].

IV. PROPOSED ADIABATIC SRAM

The adiabatic SRAM with body bias is shown in Figure 6. In general, the bulk of the PMOS (P1 and P2) transistor and NMOS (N1 and N2) transistor are connected to the V_{dd} and ground potential respectively. Body bias involves connecting the transistor bodies to a bias network in the circuit layout rather than to power or ground. The sub-threshold leakage is the drain-source current of a transistor operating in the weak inversion region. Unlike the strong inversion region in which the drift current dominates, the sub-threshold conduction is due to the diffusion current of the minority carriers in the channel for a MOS device.

In order to reduce the average power consumption, bulk bias technique is used and optimum value of bulk bias is applied only to inverter transistors, the bulk of two NMOS and two PMOS transistor which are used as access transistors, connected to the ground potential and V_{dd} respectively.

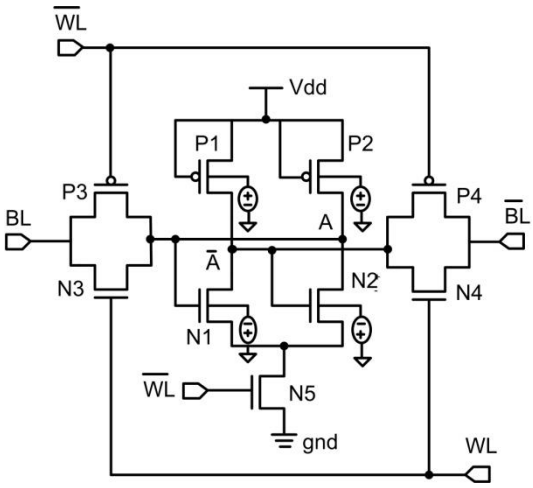


Figure 6. Adiabatic SRAM with body bias

The proposed adiabatic SRAM with multi-V_t is shown in Figure 7. Multiple threshold voltage MOS devices are used to reduce power while maintaining speed. High speed circuit paths are designed using low-V_t(N3 and N4) transistors, high-V_t(P1, P2, N1, N2 and N5) transistors and standard-V_t(P3 and P4) transistors are used.

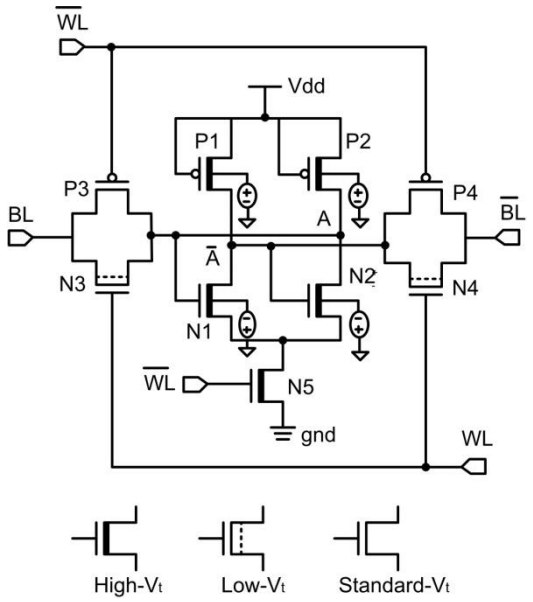


Figure 7. Proposed Adiabatic SRAM with multi-V_t

V. RESULTS AND DISCUSSION

The conventional SRAM cells, adiabatic SRAM, and the proposed SRAM are tested by Cadence spectre using an 180nm, 90nm and 45nm standard CMOS process technology. Table 1, 2 and 3 summarizes the power, delay and PDP values. From this table, it has been found that energy dissipation of proposed adiabatic SRAM is drastically reduced compared to those of the conventional 6T-SRAM and adiabatic SRAM. The operating condition for the simulation is 250MHz and supply voltages are 180nm technology is 1.8V, 90nm technology is 1.2V and 45nm technology is 1V.

Figure 8. shows the simulation wave form of the proposed adiabatic SRAM with multi-V_t technique. The four input pulse signals are WL, WLB, BL and BLB changes from 0 to 1V. The two complementary outputs are A and $\overline{A}$.

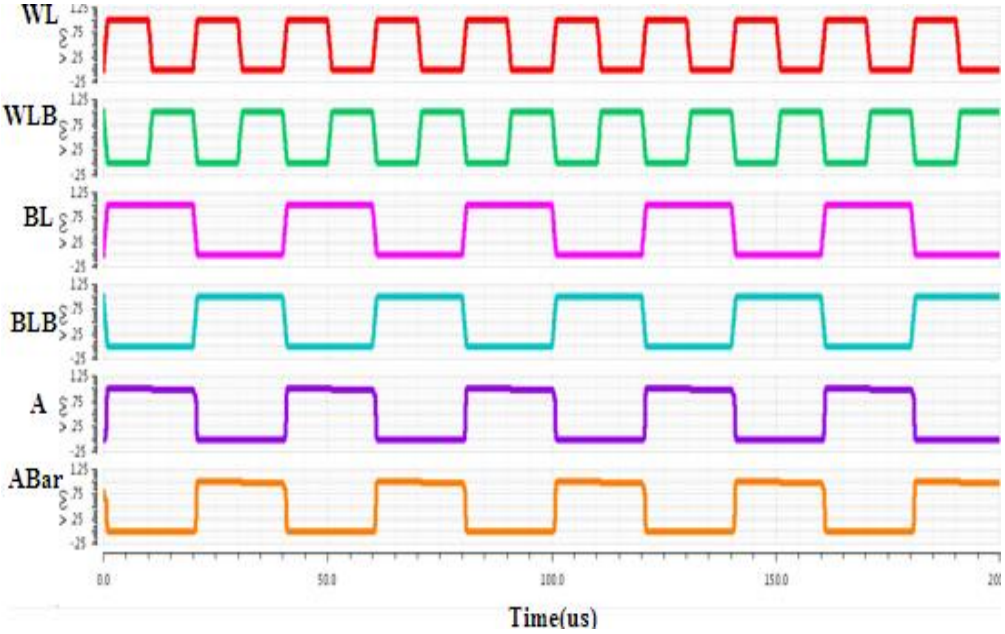


Figure 8. Simulation waveform of proposed Adiabatic SRAM in 45nm technology

Table 1. Power, delay and PDP comparisons of various SRAM cells in 180nm technology at voltage is 1.8V and temperature is 27ºC

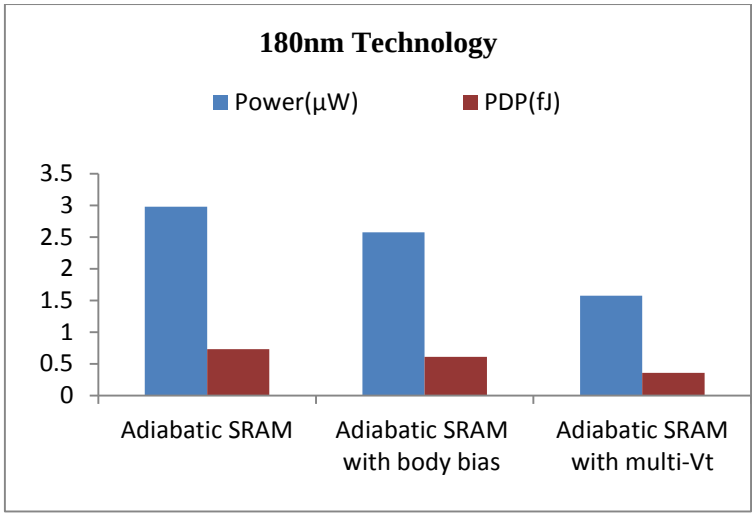
Cell	Power (µW)	Delay (ns)	PDP (fJ)
Adiabatic SRAM	2.978	0.245	0.729
Adiabatic SRAM with body bias	2.578	0.236	0.608
Proposed SRAM with multi-V_t	1.574	0.228	0.358

Table 2. Power, delay and PDP comparisons of various SRAM cells in 90nm technology at voltage is 1.2V and temperature is 27ºC

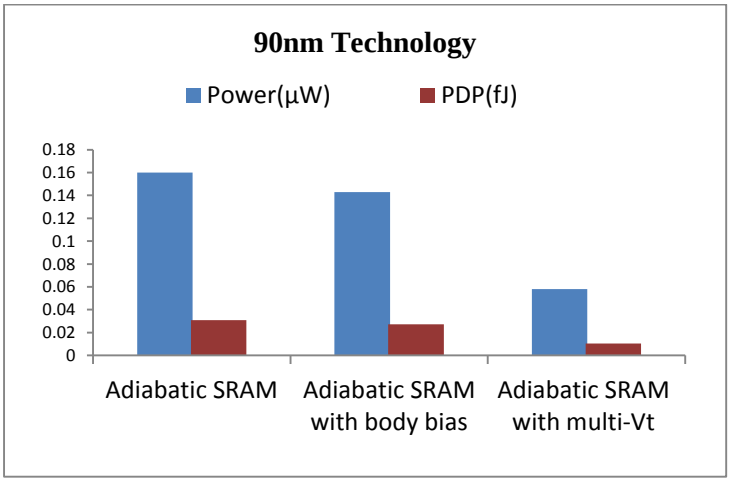
Cell	Power (µW)	Delay (ns)	PDP (fJ)
Adiabatic SRAM	0.160	0.193	0.030
Adiabatic SRAM with body bias	0.143	0.190	0.027
Proposed SRAM with multi-V_t	0.058	0.182	0.010

Table 3. Power, delay and PDP comparisons of various SRAM cells in 45nm technology at voltage is 1V and temperature is 27ºC

Cell	Power (µW)	Delay (ns)	PDP (fJ)
Adiabatic SRAM	0.010	0.173	0.001
Adiabatic SRAM with body bias	0.009	0.104	0.0009
Proposed SRAM with multi-V_t	0.007	0.102	0.0007



(a)



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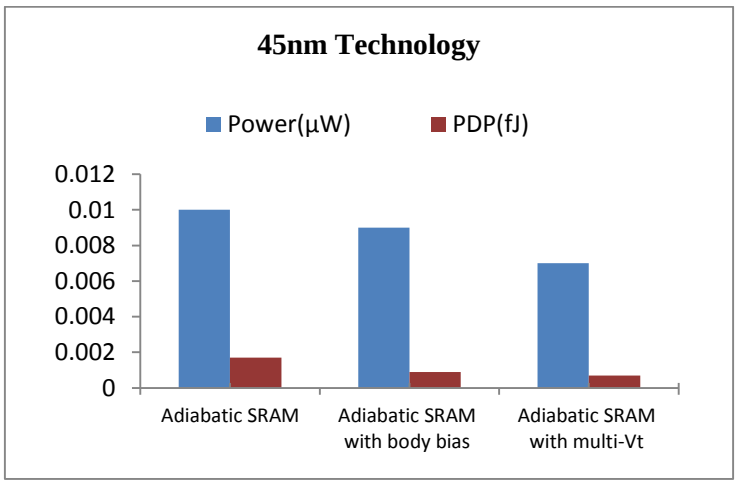

(c)

Figure 9. Power and PDP comparisons of adiabatic SRAM cells and proposed adiabatic SRAM in (a) 180nm (b) 90nm and (c) 45nm technologies.

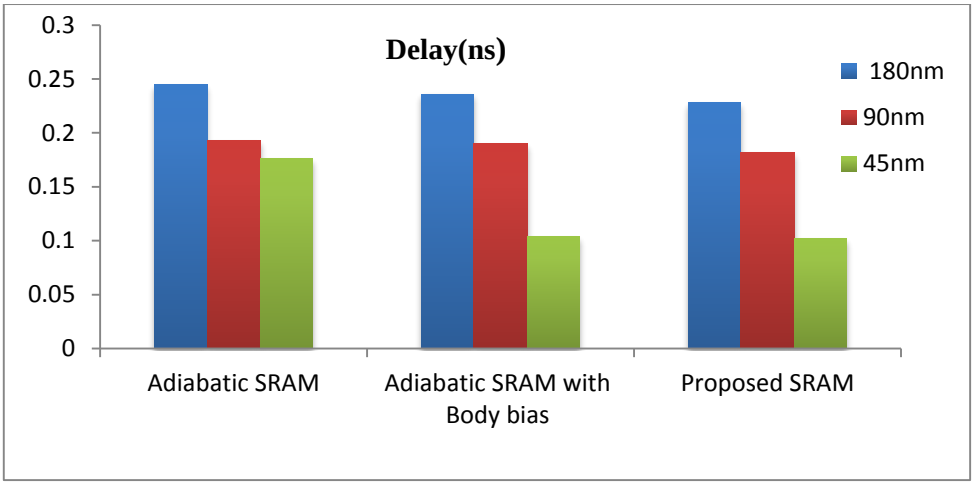

Figure 10. Delay comparisons of adiabatic SRAM cells and proposed adiabatic SRAM in 180nm, 90nm and 45nm technologies.

VI. CONCLUSIONS AND FUTURE SCOPE

In this paper, energy efficient SRAM cell is proposed. The conventional SRAM cells and proposed adiabatic SRAM cell are simulated using Cadence Spectre Simulator in 45nm, 90nm and 180nm technologies. It is found that the average power reduction for the proposed SRAM circuit in 180nm technology is 40%, 90nm technology is 58% and 45nm technology is 22% as compared to conventional SRAM circuits. In view of all these, the future course of action involves effective reduction of leakage power in an SRAM cell. It is proposed here that appropriate leakage reduction techniques would be developed with an emphasis on the reduction of gate leakage. Leakage reduction in SRAM is also possible using self controllable switch either at the upper end of the cell to reduce supply voltage or at the lower end of the cell to raise the potential of the ground node. This method would also be tested for its efficacy when this work is advanced.

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AUTHORS BIOGRAPHIES

G. Saiprakash received Bachelor's degree in Electronics and Communication Engineering from Arjun College of Technology and Science, Hayath Nagar, Hyderabad, affiliated to Jawaharlal Nehru Technological University, Hyderabad, in 2013 and presently pursuing Master's degree in Digital Electronics and Communication Systems from Vardhaman College of Engineering, (Autonomous), Hyderabad, India affiliated to JNTUH, Hyderabad. His research interests include Low-power VLSI design.

S. Rajendar received his Bachelor's Degree and Master's Degree from Jawaharlal Nehru Technological University, Hyderabad. He is currently pursuing his Ph.D from JNTU, Hyderabad. At present he is working as Associate Professor, ECE at Vardhaman College of Engineering (Autonomous), Hyderabad, India. He is a member of IEEE, IETE, ISTE, SAISE, IAENG, UACEE, and IACSIT. He has more than 20 research publications in national and international conferences and journals to his credit. His research interests include High-performance Low Power VLSI circuit design, Interconnect Modeling and Analysis.