HYBRID AND DIRECT LOGIC FULL ADDER BASED COMPARATOR USING MICROWIND

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ABSTRACT

One of the basic elements of ALU is Magnitude Comparator. Here in this paper, the design of Magnitude Comparator is described by using different styles of Full Adder design logic, where Full Adder is the basic building block of ALU which is used in Microprocessors and Digital Signal Processing. In VLSI systems, the main theme of present methodologies and techniques for design of any device is to reduce the power consumption and the area occupation. In this paper Comparator is developed by using various full adder logics with the help of DSCH2 and Microwind2. This will reduce the power consumption and area occupation.

KEYWORDS: *Arithmetic Logic Unit (ALU), Magnitude Comparator (MC), Full Adder (FA), Power, Area*.

I. INTRODUCTION

Comparator is one of the basic and useful arithmetic components of ALU. There are so many designs of comparator are present with different results of area occupied, power consumption, number transistors used [1]. In today's world of technology, all the users of smart systems are aimed to use best systems which can give the better results with low power consumption [2] and low area at high speed. The low power consumption is possible when the number of transistors is reduced on the chip of particular circuit, by this, we can import many number of devices on a single chip and area can be decreased [4].

The main conspire of VLSI systems for new approaches is power saving of a device or system. Low power consumption helps to reduce installation costs [4] [5]. By the reduction of power consumption, operating Speed of the device or system will increase. So that can achieve the better results [6]. One of the better ways to bring down the power of circuits is to find the new methodologies of circuits for preserving power [7]. In this paper, we propose different design techniques of comparator for better performance and power-efficient [8].

Comparison of any two binary numbers is one of the arithmetic operations of ALU [9]. This comparison determines if the number is greater than (>), less than (<) or equal to another number. This comparison is done by the Magnitude Comparator. Magnitude Comparator is a combinational circuit that compares the two binary numbers of any numbers of bit and gives the outcome as three variables [10]. The below fig shows the comparators block diagram.

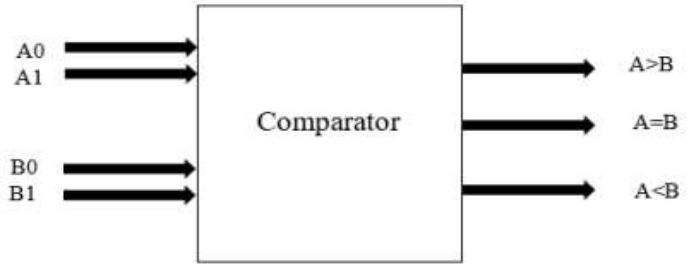

Figure 1 : Two-bit Magnitude Comparator

As figure shows above, Comparator can take the two binary numbers A and B irrespective of two bits and produce the outputs as A>B, A<B and A=B. We have n-bit Magnitude comparator that takes two binary numbers of n-bit and produce three outcomes as less than (<), greater than (>) and equal to (=). Here we said the Magnitude Comparator is designed by using Full Adder [11]. Full Adder which consists of three inputs and produces two outputs, those are Sum and Carry. Main function of Full Adder is addition of binary numbers [12]. The diagrammatic representation and truth table of basic Full Adder is shown in below.

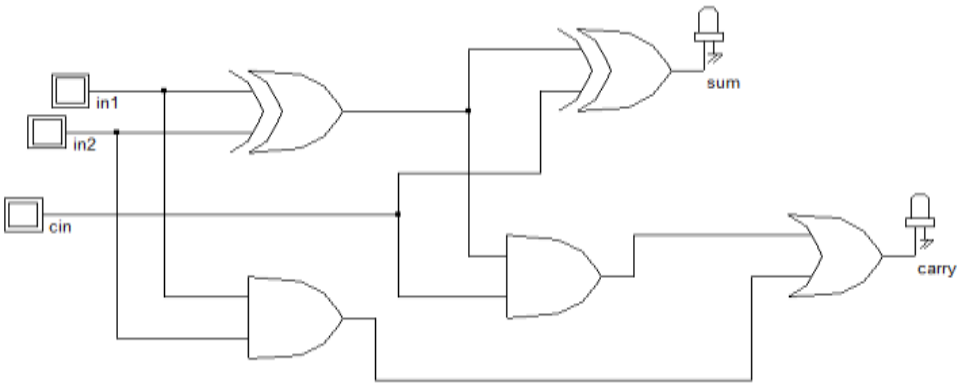

Figure 2 : Basic Full Adder

Table 1 : Truth table of Full Adder

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

II. EXISTENT METHODOLOGY

This paper imparts the design of comparator using Full Adder design logic. The subordinate figure illustrates the figure of Basic Full Adder based Comparator.

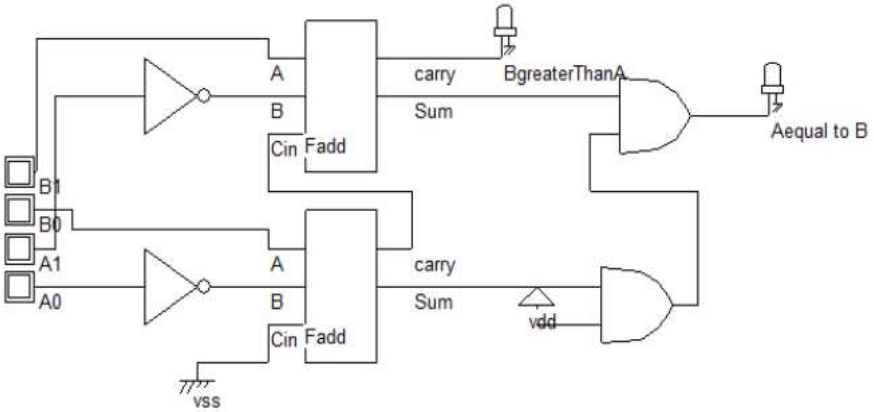

Figure 3: Block diagram of Basic Full Adder based comparator

Table 2 : Truth table of Full Adder based Comparator

A0	A1	Bo	B1	A>B	A<B	A=B
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	0	0	1
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	0	1
1	0	1	1	0	1	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0

Design:
The Diagrammatic design of Basic Full Adder based comparator is shown in below. It consists of logic gates AND, OR, NOT and XOR. This diagrammatic design is designed by using the tool Digital Schematic (DSCH2).

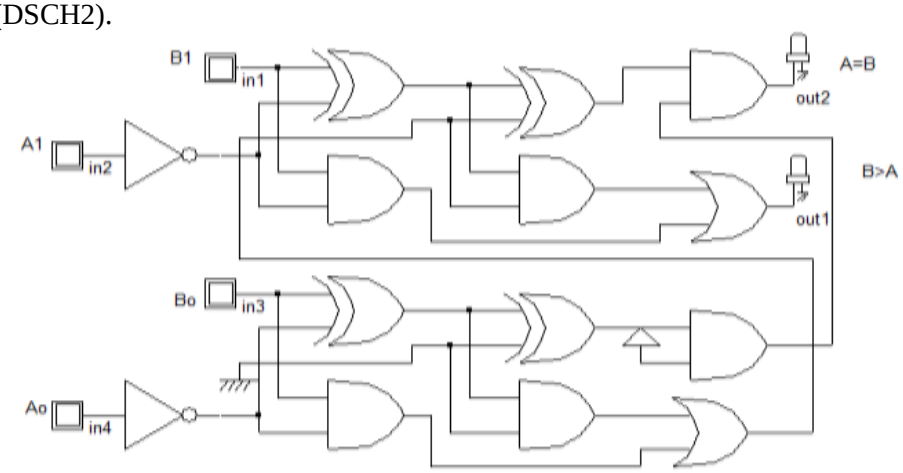

Figure 3 : Basic Full Adder Based Comparator

The layout and Analog simulation of the basic Full Adder based Comparator is shown below figure: 4(a) & figure: 4(b). The Layout of circuit can tell of the geometrical representation of circuit. This Layout design is obtained by using the tool Microwind2.

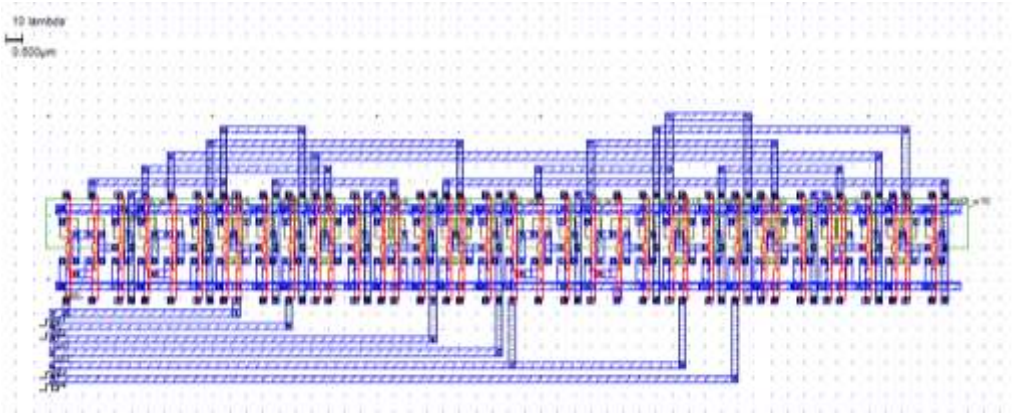

Figure :4(a) layout of the basic Full Adder based Comparator

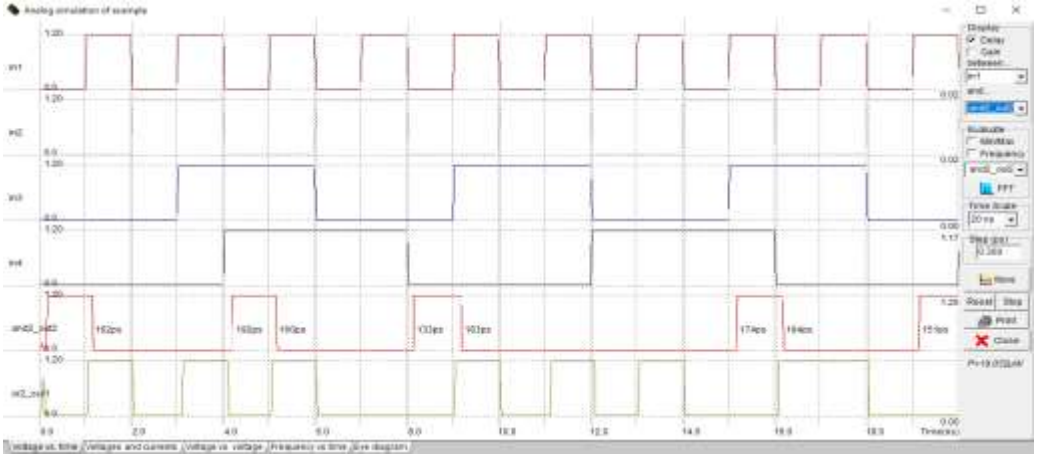

Figure :4(b) simulation of the basic Full Adder based Comparator

III. INTENDED METHODOLOGY

To increase the power efficient of comparator than the existent method, we propose another style of comparators using different Full Adder design logics. These may increase the power efficient of comparator. These methodologies are, one is Hybrid Full Adder based Comparator and another on is Direct Logic Full Adder based Comparator.

The below figure shows the Basic Hybrid Full adder and design of comparator by using basic hybrid full adder

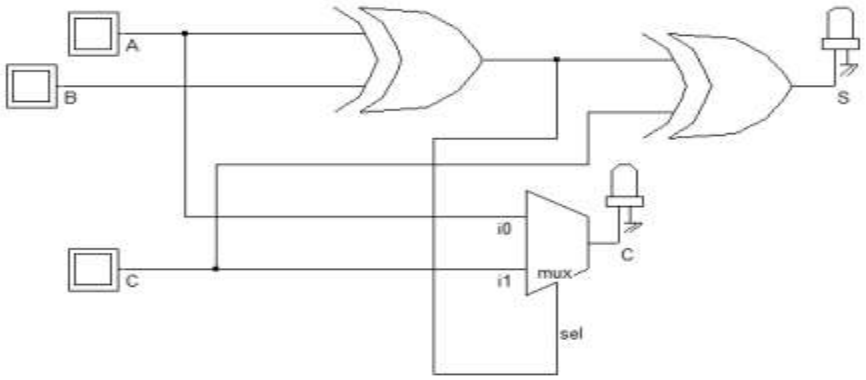

Figure 5 : Basic Hybrid Full Adder

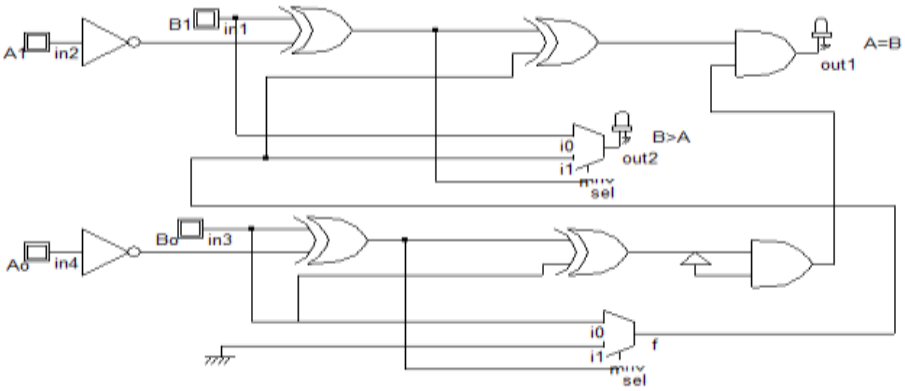

Figure 6 : Hybrid Full Adder based Comparator

The corresponding layout design and the analog simulations are shown in below figure:7(a) & figure:7(b). The Layout of circuit can tell of the geometrical representation of circuit. This Layout design is obtained by using the tool Microwind2.

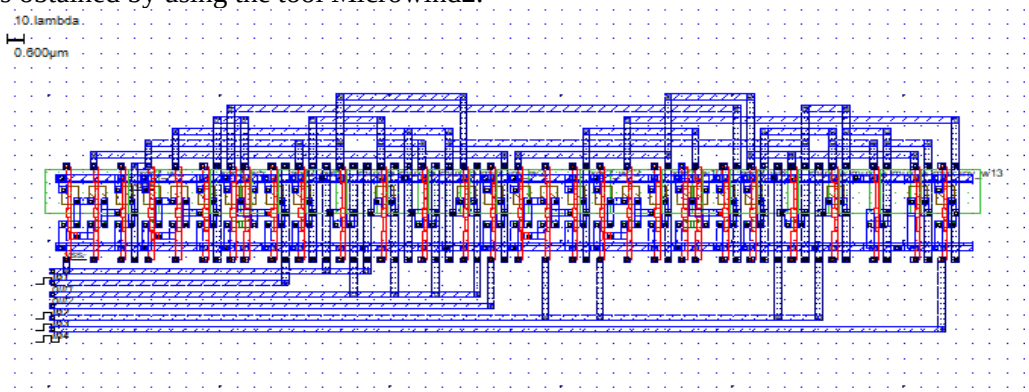

Figure : 7(a) layout design of Hybrid Full Adder based Comparator

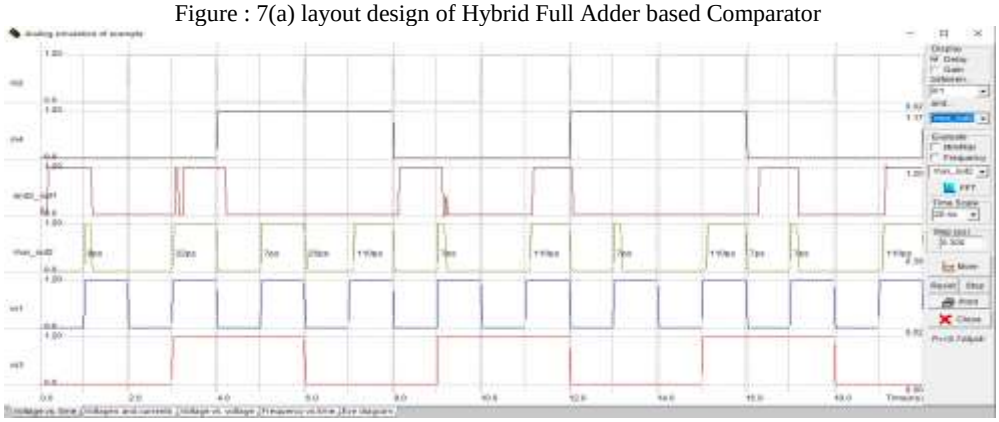

Figure : 7(b) simulation result of Hybrid Full Adder based Comparator

The other intended method is design of comparator by using Direct Logic. The below figures shows the Direct logic based Full adder and the Direct logic Full Adder based Comparator.

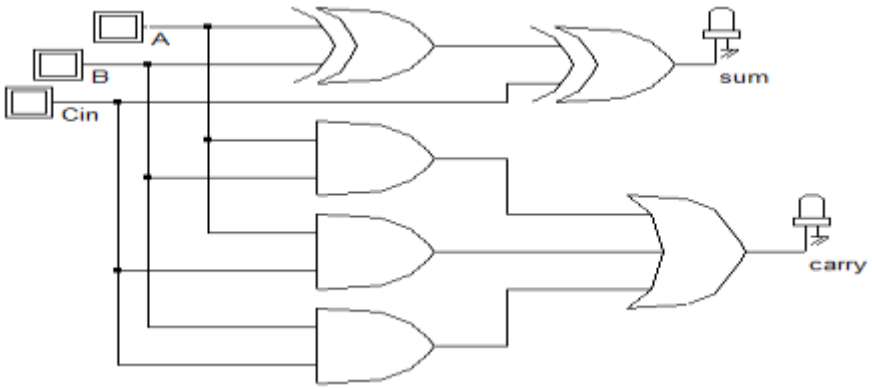

Figure 8: Direct Logic based Full Adder

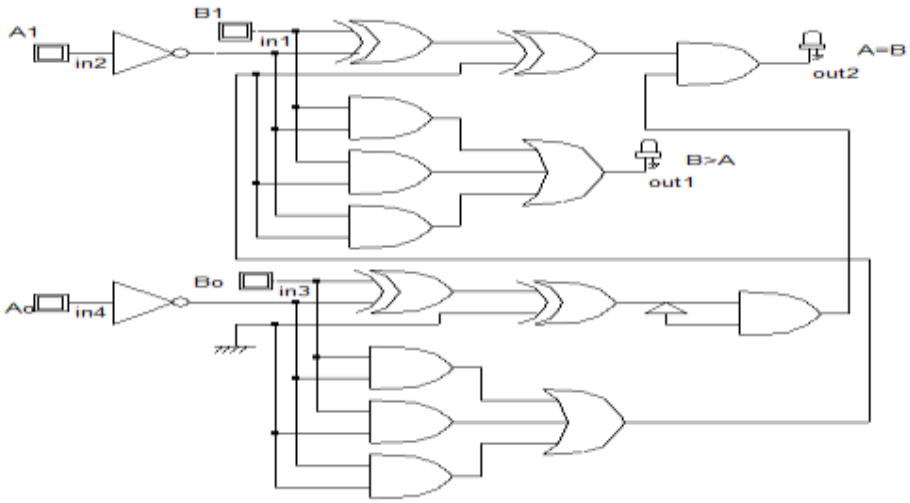

Figure 9 : Direct Logic Full Adder based Comparator

The layout and analog simulation of this method is shown in below figure:10(a) & figure:10(b).

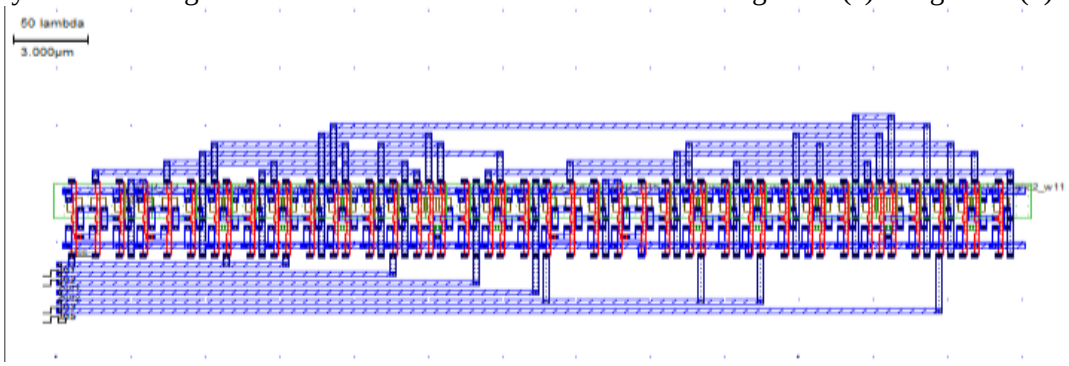

Figure :10(a) layout design of Direct Logic Full Adder based Comparator

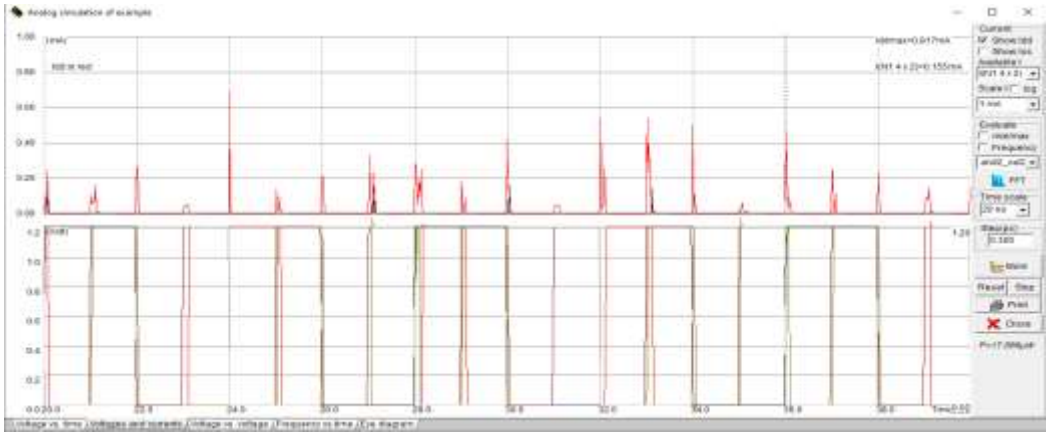

Figure :10(b) simulation result of Direct Logic Full Adder based Comparator

IV. ANALYSIS AND COMPARISON

Here the analysis of different logic styles of Comparator using Full Adder logic design was done with the help of software tools DSCH and Microwind. The comparison of those methodologies is shown in below table3.

Table 3 : Comparison of various Comparators

Full Adder Based Comparator Design	Area(μm²)	Power(μw)	Routed wires
Basic Full Adder	455	19.032	25
Hybrid	442	15.745	37
Direct Logic	560	17.886	30

V. CONCLUSION

This paper depicts different logic styles of full adder for designing a comparator for power proficient. Basic full adder based comparator Logic Style provides high power contrasted with Hybrid and Direct Logic Full Adder Based Comparator and area design as compared to other Logic Style. Hybrid logic Full Adder Based comparator logic style gives low power utilization & area. Direct Logic Full Adder based comparator consumes less power when contrasted with Basic Full Adder logic style and consumes high power as constrased with Hybrid logic Comparator. In any case, the area utilization is more noteworthy , contrasted with another two full adder based comparators. So different approches have different benefits and impediments specifically field. In view of client necessity architect can pick the better exhibition strategy to satisfy the client objective.

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