NOISE ANALYSIS OF A PHASE SHIFT OSCILLATOR BASED ON CNTFET

Roberto Marani* and Anna Gina Perri**[a]

* National Research Council of Italy, Institute of Intelligent Industrial Technologies and Systems for Advanced Manufacturing (STIIMA), Bari, Italy
** Electronic Devices Laboratory, Department of Electrical and Information Engineering, Polytechnic University of Bari, via E. Orabona 4, Bari, Italy
annagina.perri@poliba.it

ABSTRACT

We present a method to match the output and transconductance characteristics between two CNTFET models proposed in literature. Then we briefly describe a compact noise model, used to simulate the noise performance of a phase shift oscillator, in order to analyse how the noise sources, constitute a significant limitation for circuits based on CNTFET. All simulations have been obtained in Verilog-A, and for this we indicated the code lines to add to the software to be able to do the proposed noise analysis.

KEYWORDS: *CNTFET, Modelling, Noise sources, Phase shift oscillator, Verilog-A.*

I. INTRODUCTION

A CNTFET is a Field Effect Transistor that has the typical structure of the MOSFET, but uses a single or multiple Carbon NanoTubes (CNTs) instead of silicon as a channel material [1-16].
In the first part of this paper, we present a method to match the output characteristics and transconductance characteristics between two CNTFET models: the first, proposed by us [5-6] and the second the Stanford one [17-18].
Then we briefly describe a CNTFET compact noise model, proposed by us in [19] and used in this paper to simulate, in Verilog-A [20], the noise performance of a phase shift oscillator.
The presentation is organized as follows. A brief review of the examined models with the method to match the models is presented in Section 2, while a quick description of the main noise sources in CNTFETs are given in Section 3. Section 4 is devoted to the simulation of a CNTFET phase shift oscillator, while conclusions are described in Section 5.

II. MATCHING BETWEEN THE TWO CONSIDERED MODELS

In this paper we consider a DC model of CNTFET [5-6] and named in sequel LabDispositivi *model*. Therefore, we suggest the reader to consult these References.
The Stanford-Source Virtual Carbon Nanotube Field-Effect Transistor model (VS-CNFET) [17-18], named also *Wong's model*, is a model that describes the I-V characteristics in a short-channel CNTFET. Also in this case we suggest the reader to consult References [17-18],
Now we want to propose a method to match the output and transconductance characteristics between these two models.
The main obstacle to match characteristics of the two models is in different nature of these.
Stanford model has quantum resistances and inductances included internally while our model needs the definition and connection of certain external resistances and inductance. Moreover, Stanford model

[a] Corresponding author.
ORCID iD https://orcid.org/0000-0003-4949-987X Scopus ID: 7004631160
e-mail roberto.marani@stiima.cnr.it **ORCID iD http://orcid.org/0000-0002-5599-903X**

includes an internal parameter to set the flat band voltage while this operation must be done externally for our model. Anyway, the starting point is to set the same technological parameters (such as CNT diameter, channel length, etc.) to both models and then bias them with the same voltages.
Only after this, we can think about sizing of the external components.
In Fig. 1 we show the circuit used to match the two models.

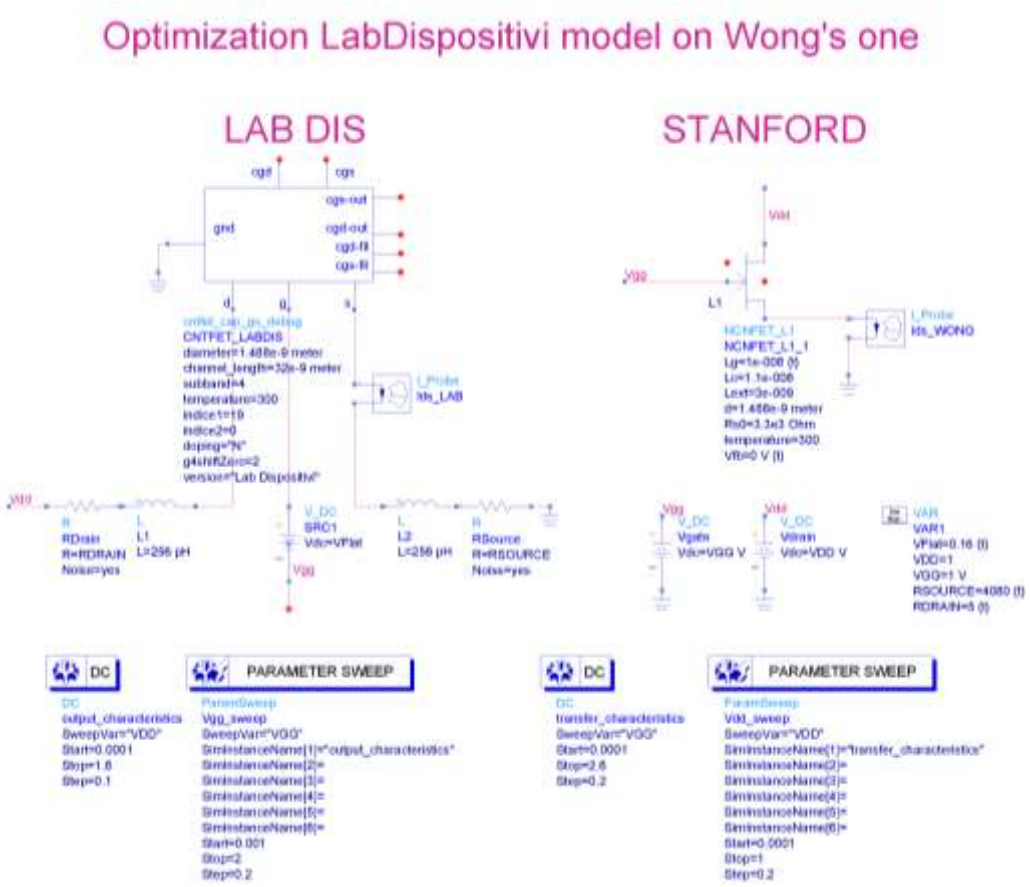

Figure 1. Circuit used for matching the two considered models.

For the design of the inductances, there is a quantum and a classical contribution. The quantum inductance, usually referred to as kinetic inductance L_g, is the resistance to the change of the kinetic energy of the electrons of the CNT and is dominant [21].
We have splitted L_g into two inductances of 8 nH/μm to connect them to the drain and source of the CNTFET.
About the design of the resistances, our objective is to obtain the resistances values with an empirical simulation: we put two parametric resistances on drain and source of our CNTFET. Then we plot the output characteristics of the two models on the same graph and we start using the *Tuning* function of the software Verilog-A [20]. This allow us to vary the resistances values and to see in real-time the effects on the output characteristic.
During this process, with the same method, we compared the variations in transconductance characteristic. It was also necessary to set few millivolts of an external flat band voltage generator located on gate, to obtain the best matching possible.
As expected, at high values of R_{SOURCE} and R_{DRAIN} there is a reduction in output gain while at increasing values of flat band voltage, there is a more pronounced slope of the characteristics, visible especially at higher voltages.
The best results are obtained with R_{SOURCE} = 5 Ω, R_{DRAIN} = 4.08 Ω and $V_{FLAT\ BAND}$ = 0.16 V.
Figs. 2 and 3 show the output and trans-characteristics of LabDis model and Stanford one respectively.

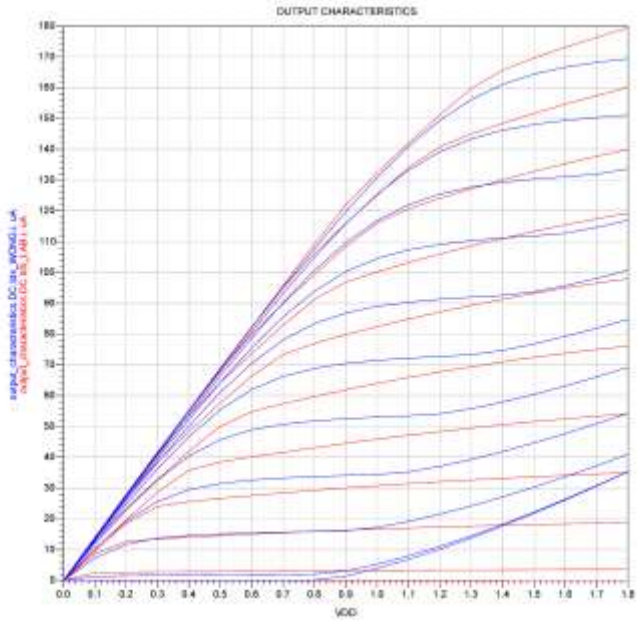

Figure 2. Output characteristics of LabDispositivi model (red) and Stanford one (blue).

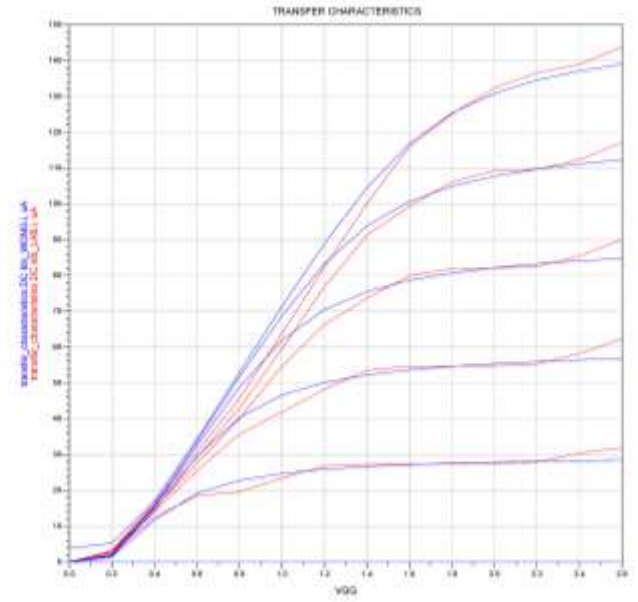

Figure 3. Trans-characteristics of LabDispositivi model (red) and Stanford one (blue).

The trans-characteristics are now strongly correlated but in the output characteristics there are some mismatches. At higher voltages, Stanford curves show a more pronounced tunneling effect compared to our model. This problem has been solved varying an internal parameter of our model that controls the beginning of tunnel effect, obtaining results quite satisfactory.

III. IMPLEMENTATION IN VERILOG-A OF NOISE SOURCES

Regards to noise model, in [22] we have proposed a compact noise model of CNTFET, and therefore, also in this case, we suggest the reader to consult this paper.
In this Section, we just show the main equations which describe the main noise sources in CNTFETs. In particular in this paper we implemented in Verilog-A [20] the following noise sources:

1) Thermal noise of R_G, R_S and R_D, whose power spectral density (PSD) is:

$$S_{Th,R} = 4kT/R \tag{1}$$

where is R is R_G or R_S or R_D. For the implementation of this noise, we used the built-in ADS feature [20] that evaluates thermal noise of resistors present in circuits.

2) Channel thermal noise and shot noise

PSD of channel thermal noise is [23]:

$$S_{Th,Ch} = 4kT\gamma g_{d0} \tag{2}$$

being g_{d0} the channel conductance at $V_{DS} = 0$ V and γ the *white noise gamma factor* [24], while PSD of channel shot noise is:

$$S_{Shot,Ch} = 2qI_{DS} \cdot F(I_{DS}) \tag{3}$$

where $F(I_{DS})$ is the *Fano factor*, whose value is between 0 and 1. We considered the worst case condition, i.e. F = 1 [22].
The code line that we add in the main Verilog file to implement this kind noise is:

```
I(d,s) <+ white_noise(2*elettroneCarica*ids, "shot noise")
```

3) Flicker noise

The PSD of flicker noise is [25]:

$$S_{1/f,Ch} = A_H \left(\frac{I_{DS}^2}{f} \right) = \left(\frac{\alpha_H}{n} \right) \left(\frac{I_{DS}^2}{f} \right) \tag{4}$$

A_H is the ratio of the Hooge constant a_H and the number of carriers n in the channel, choosing the standard value of a_H equal to 10^{-4} and n = 100.
To implement this noise, we used a Verilog-A function called `flicker_noise(pwr,exp)` which generates a noise with a power of pwr at 1 Hz which varies in proportion to $1/f^{exp}$. So, we introduced this new code line in the main Verilog file of model:

```
I(d,s) <+ flicker_noise(ids*ids*(alfah/ncarriers), 1, "flicker noise")
```

IV. NOISE ANALYSIS OF A SHIFT PHASE OSCILLATOR

Fig. 4 shows a three-stage phase-shift oscillator constituted by three identical RC networks.

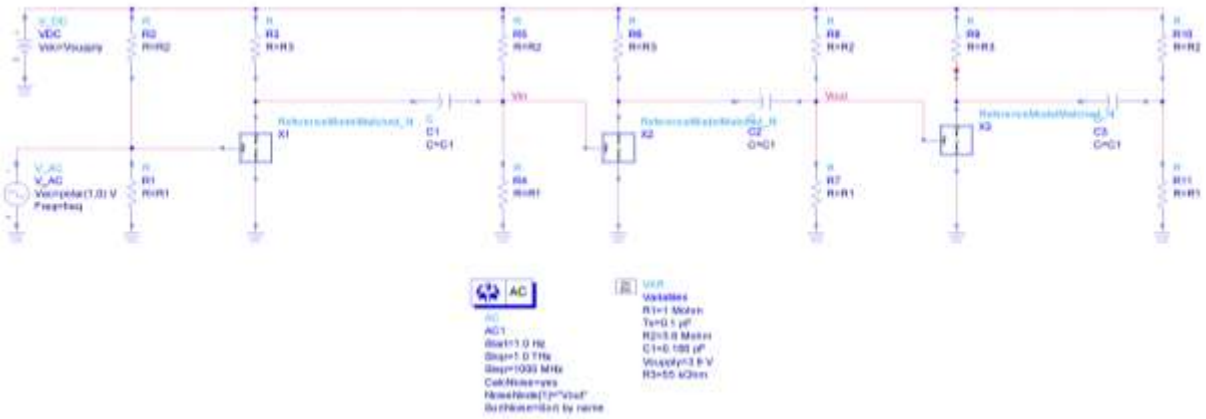

Figure 4. Phase-shift oscillator circuit.

To avoid the difficulties of noise analysis in closed-loop, we perform our study in open-loop.
In particular only the central stage was under test because in this way the noise analysis is more accurate.
In the next figures, from Fig. 5 to Fig. 8 we show the single and total contributions of noise evaluated on the output node of the second circuit stage.

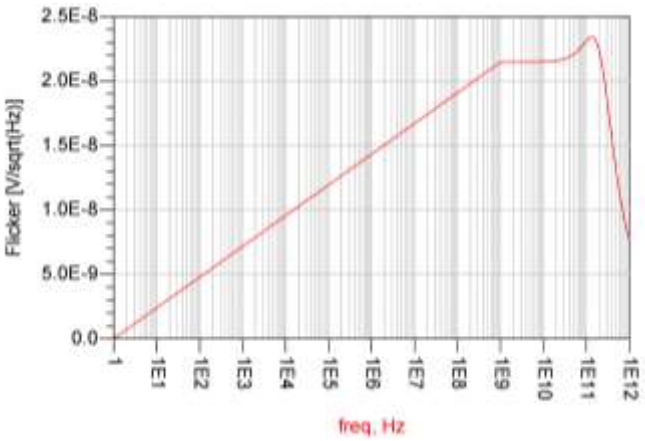

Figure 5. Flicker noise.

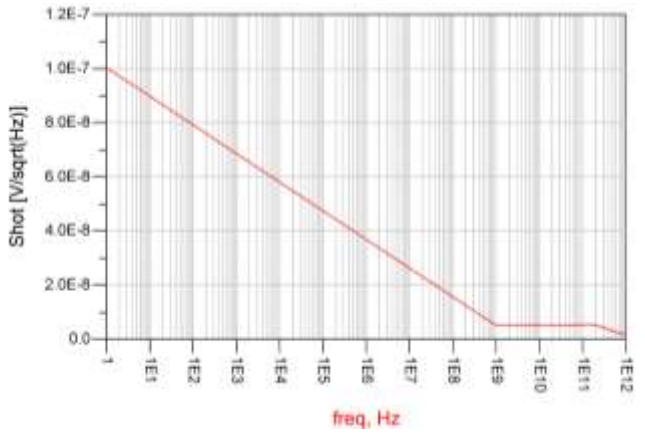

Figure 6. Shot noise.

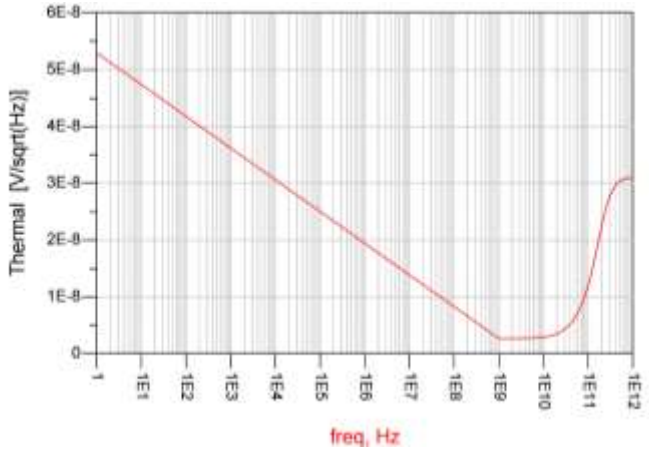

Figure 7. Thermal noise.

Figure 8. Total noise.

For frequencies below 10 GHz the main contribution is the flicker noise for its 1/f dependence. For frequency over 10 GHz the main contributor are the shot noise and the thermal noise.
Since the thermal noise is proportional to the resistances, we can say that its reduction requests a better control of the various parasitic resistances, always considering that the limit for channel resistance is the quantum limit.
At last we have repeated this procedure using MOSFET, obtaining, as in [26], that the output noise current is always higher for the CNTFET than for the MOS device.

V. CONCLUSIONS

In the first part of this paper, we presented a method to match the output and transconductance characteristics between two models: LabDispositivi model and the Stanford one.
Then we briefly described a CNTFET compact noise model, used to simulate the noise performance of a phase shift oscillator, in order to analyse how the noise sources constitute a significant limitation in the design of circuits based on CNTFET. All simulations have been obtained in Verilog-A, and for this we indicated the code lines to add to the software to be able to do the proposed noise analysis.

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AUTHORS

Roberto Marani received the Master of Science degree *cum laude* in Electronic Engineering from Polytechnic University of Bari, where he received his Ph.D. degree in Electronic Engineering.
He worked in the Electronic Device Laboratory of Bari Polytechnic for the design, realization and testing of nanoelectronic systems. Moreover he worked in the field of design, modelling and experimental characterization of devices and systems for biomedical applications.
Currently Dr. Marani is a Reseacher of the National Research Council of Italy (CNR), at the Institute of Intelligent Industrial Technologies and Systems for Advanced Manufacturing (STIIMA), Bari, Italy, where he cooperates with the Intelligent Sensing and Perception Group.
He has published over 180 book chapters, journal articles and conference papers and serves as referee for many international journals.

Anna Gina Perri received the Laurea degree *cum laude* in Electrical Engineering from the University of Bari in 1977. In the same year she joined the Electrical and Electronic Department, Polytechnic University of Bari, Italy, where she is Full Professor of Electronics from 2002.
In 2004 she was awarded the "Attestato di Merito" by ASSIPE (ASSociazione Italiana per la Progettazione Elettronica), Milano, BIAS'04, for her studies on electronic systems for domiciliary teleassistance.
Her research activities have been in the area of numerical modelling and performance simulation techniques of electronic devices for the design of GaAs Integrated Circuits, in the characterization and design of optoelectronic devices on PBG (Phothonic BandGap) and in the field of experimental characterization of electronic systems for biomedical applications.
Currently she works in the design, realization and testing of nanometrical electronic systems, quantum devices and FET on carbon nanotube.
Prof. Perri is the Head of the Electron Devices Laboratory of the Polytechnic University of Bari and is author of over 300 journal articles, conference presentations, twelve books and currently serves as a Referee and Editorial Board Member of a number of international journals.
Prof. Perri is the holder of two italian patents and the Editor of three international books.