ESD SHIELD FOR ICS: A REVIEW

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ABSTRACT

Modern Integrated circuits are severely affected by ESD (electro static discharge) which may severely affect the performance of ICs or may even lead to complete failure of the chip. electro static charge represents a very high voltage which gives rise to very high peak current causing problem of burn out in ICS. A per the Moore's law number of components on an Integrated circuit will double in every 18 to 24 months this results in miniaturization resulting in individual components becoming smaller each day. This makes integrated components more and more sensitive to the effects of damage occurring due to ESD. Even a small discharge through a very small component may cause result in cumulative overheating, or complete breakdown of the component. Various techniques are employed to overcome from ESD. Some of the techniques are use of products like static dissipative workbench, anti-static or static dissipative containers, or some designers even use especially custom designed ESD Protection devices in their circuits. Common ESD protection devices employs snap-back principle for protecting ICs from damage. snap-back characteristic is similar to a common silicon control-rectifier.

KEYWORDS: *electro static discharge, Protection, Grounding*

I. INTRODUCTION

ESD is discharge of the large amounts of electrical static charge between two bodies at different potentials and at very fast rate on to the chip causing damage. Whenever IC damages the designers have the first in mind that it would be an ESD.ESD damages are mostly high current related. Voltage related damage modes such as Gate-oxide breakdown are less often encountered. As gate-oxide gets thinner, however, gate-oxide degradation and breakdown becomes increasingly important. To guard against such failure, ESD design must limit the voltage experienced by the affected circuits during an ESD event.

1.1. What is ESD.

Static charge is an unbalanced electrical charge at rest. Typically, it is created by insulator surface rubbing together or pulling apart. One surface gains electrons, while other surface losses electrons. This result in an unbalanced electrical condition known to as static charge. When a static charge moves from one surface to another, it becomes ESD.

Standard CMOS chips can be damaged by static voltages of as little as 250V. These include the 74HC and 74HCT logic families are widely used in many designs using "glue logic" because of their lower current consumption.

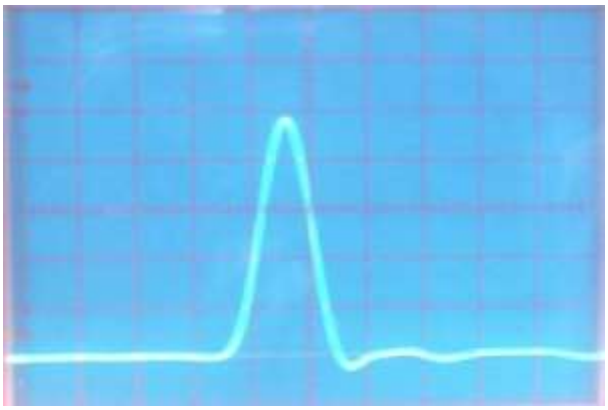


Fig. 1. Oscilloscope trace of the 50ps (full width at half maximum) stress pulse.

Whenever ESD event occur in design, there is a voltage/current spikes as shown in Fig. 1, which may damage the junction, if occur in ESD discharge path (Fig 2.a), damages the routing metals (Fig 2.b) or on high CDM stress may lead to oxide rupture (Fig 2.c). Shown in Fig. 2.

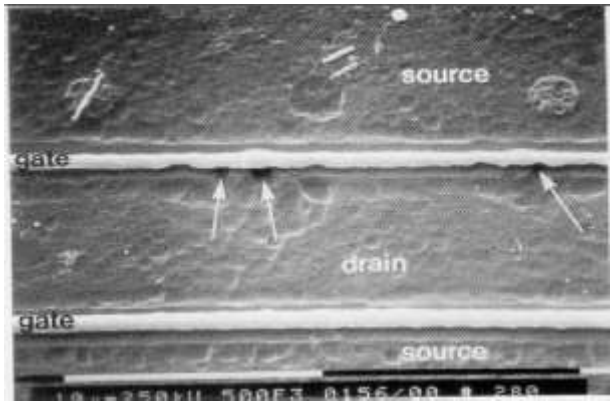


Fig. 2.a Drain Junction Damage after ESD Stress

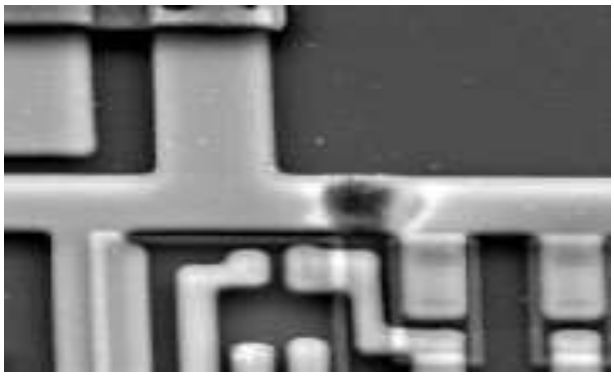


Fig. 2.b Metal damages after an ESD Stress.

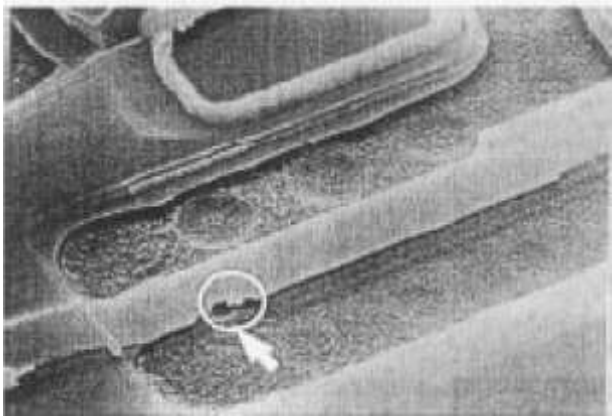


Fig. 2.c Gate Oxide rupture to an input buffer after CDM stress.

II. HOW TO PROTECT THE CIRCUIT FROM ESD

Now all the IO designers think about ESD during their circuit design. The main task they have to think about is how to bypass the high stress to ground without effecting circuit functionality, for this they have to use ESD Protection Devices, like SCR, Bipolar NPN, and GGNMOS.
The main task of these devices is they have to pass the charges to ground from any PAD of the circuit during an ESD event. These devices are switched ON on an ESD occurrence in the circuit, so as to flow the charges to ground not in the circuit.

2.1 ESD Concepts.

Fig 3. Explains that stress can travel any path of the design and may damage the junction, metal contact etc. To avoid an ESD stress pulse not to flow in circuit, designers uses ESD protection devices at each PAD the circuit where the possibility of ESD occurrence. For example, suppose an ESD occur at I/O PAD of Fig 3, and then they have to provide positive and negative clamps at this node to bypass the positive and negative charges to ground.

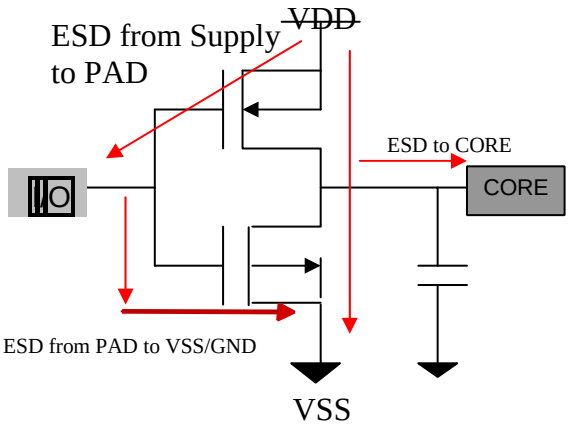
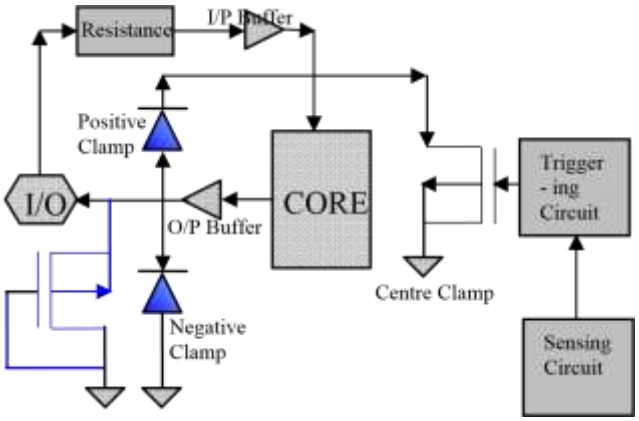


Fig 3. ESD Stress/Charge flow in the circuit.

Clamp used in the circuit generally are the diode but they can bypass the charges which is developed by the HBM (Human Body Model) or MM (Machine Model). If stress is occurring due to CDM (Charge Device Model) then designers must be used ESD Protection devices which are capable to clamp the high voltage to low voltage, or bypass the ESD stress/charge at very fast rate. These Protection devices operate in “snap back” region where the voltage becomes lowers and current suddenly increases i.e. grounding the charges at very fast rate.

2.2 ESD Protection

Depend upon the ESD stress whether they are because of HDM, MM or CDM, Clamps are used to bypass the charges to ground.



GGNMOS

Fig 4. Clamps in the circuit where they bypass the charge upon on ESD event. GGNMOS is used for fast discharge.

Whenever ESD event (HBM or MM) occurring at I/O PAD then depend upon charge polarity it will bypass to ground, i.e. When positive charge encounter at PAD then it will forward bias the Positive Clamp diode and bypass the charges to ground through centre clamp, and Negative Clamp become forward bias when negative charges occur at PAD, becomes grounded.

III. GGNMOS ESD PROTECTION DEVICE

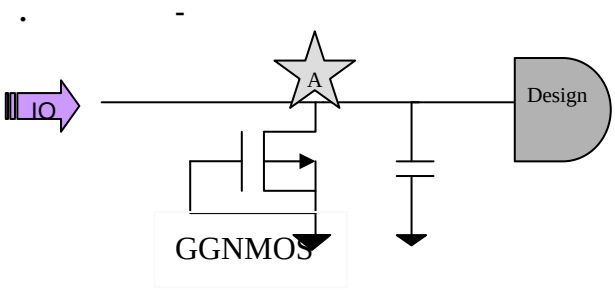


Fig. 5: GGNMOS Device

Gate Grounded NMOS shown in figure 5 is a ESD protection device whose function is to bypass the charges very fast, GGNMOS characteristics is same as SCR but it will not require any kind of triggering pulse.

GGNMOS is a NMOS whose Gate and Source are shorted, such that NMOS will never on, reader might be think that when NMOS is never on then how it would bypass the charges to ground, this is because of Two parasitic diode form in NMOS substrate region as shown in Fig 6. Two diode back to back form an NPN parasitic bipolar and because of this NPN device GGNMOS goes in snap-back region causing discharges.

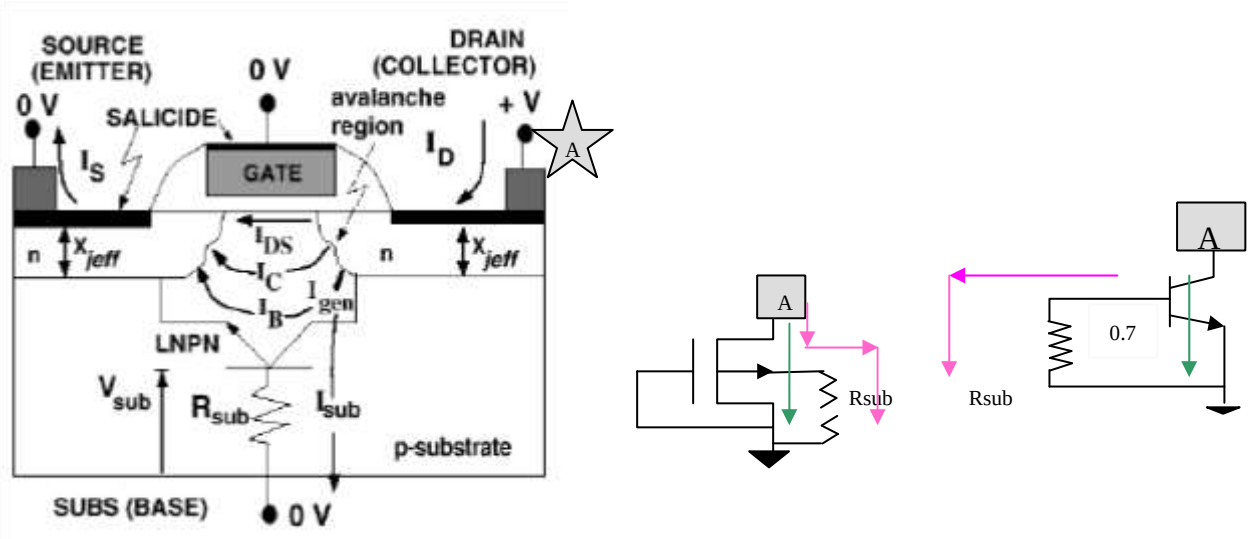


Fig 6. Parasitic NPN in GGNMOS whose Gate, Source and Substrate are at same potential.

3.1 GGNMOS Device Physics

On an ESD event occurring high amount of voltage at drain terminal would be developed and because of this Collector-Base (Drain to Substrate) junction of the Parasitic NPN is goes in Avalanche break down and leads to bypass the stress to ground through substrate initially, as substrate voltage reaches to Knee Voltage of the NPN, the Base-Emitter (Substrate-Source) junction is Forward bias and now stress bypass to ground through Source, this leads to increase in Drain current by reducing the collector-emitter voltage.

When the Parasitic bipolar NPN is ON then collector to emitter voltage reduces and collector (Drain) current increases as it goes to active region, and this reduce in voltage increase in current is so called Snap-back effect.

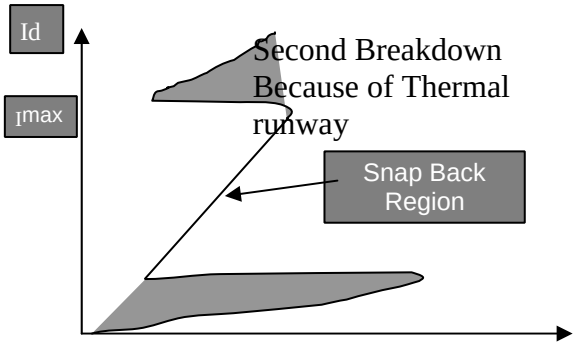


Fig 6. Snap-Back Effect of Parasitic Bipolar NPN in GGNMOS ESD Protection device.

During Normal operation, Gate voltage should be below threshold, thus NMOS acts as an open circuit.

IV. ESD MODELS

Models are needed to simulate ESD phenomena. As we know that static charges may comes from any of the medium such as by touching Human Body, any charged Instrument or from Device it self, based on this, Three types of models have been suggested are as: Human Body Model(HBM), Machine Model(MM), Charge Device Model(CDM). Through these models robustness of devices to ESD can be determined and compared.

V. CONCLUSIONS

It is found that recently for an any IC Designers ESD issues are at prime concern like, “Increased IO & power pins per chip, component reliability as good as its weakest PAD, scaling reduces Gate thickness area, Increased sensitivity towards the fabrication process, Increased peripheral issues like Power Sequencing”. To overcome from ESD Stress Designers have to use ESD Protection devices like GGNMOS. NMOS operates as clamps when in Snap-Back region, as ESD event triggers Gate voltage lowering snap-back voltage.

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