DESIGN CRITERIA OF CNTFET-BASED A/D CIRCUITS: A REVIEW

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ABSTRACT

In this paper we review design criteria to evaluate the performance of typical analog and digital (A/D) circuits based on CNTFET, both in SPICE, using ABM library, and in Verilog-A, using a semi-empirical compact model for CNTFETs already proposed by us. The obtained results, with reference to a design of a phase shift oscillator, as example of analog circuit, are the same in static simulations and comparable in dynamic simulations. However using Verilog-A the simulation run time is much shorter and the software is much more concise and clear than schemes using ABM blocks in SPICE.
Then we review a procedure in order to carry out static and dynamic analysis of basic digital circuits. In particular, to carry out the dynamic analysis, we consider both the quantum capacitance effects and the sub-threshold current. At last we analyze the timing performances of a NOT gate in order to define the optimal working conditions, emphasizing that the proposed method can be used to analyze the timing performance of any CNTFET-based logic gate.

KEYWORDS: *Nanotechnologies, CNTFET, Analog Circuits, Digital Circuits, CAD, SPICE, Verilog-A.*

I. INTRODUCTION

Technology can be defined as the set of processes or steps of processing required to manufacture devices and systems of any complexity.
The advance of technology is accompanied by the advance of progress where for **progress** we intend all technological products which allow to do: devices for transportation, home automation, medical applications, computing, graphics, telecommunications, creating new tools to acquire knowledge (research), to educate, and so on.
The advancement of technology is measured by the minimum size that a device can reach because the reduction in the size is associated to an increase of the potential or performance (for example the speed) and applications. As technology advances, the minimum size is reduced up to dimensions of several nanometers.
However, the transition from micro-technologies to the nano scale (or **nanotechnologies**) is not trivial but rich in implications.
Nanotechnologies, in fact, do not mark an evolution but a technological revolution and represent the possible solution to not hinder progress [1].

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It is clear, therefore, that they have a key role in the future of humanity and are therefore the subject of considerable research efforts around the world.

Due to their low dimensionality, Carbon NanoTubes, also known with the acronym **CNTs** (**C**arbon **N**ano**T**ubes), have unique electronic and mechanical properties that make them promising candidates for future nanotechnology applications [2-3].

However, to truly harness their potential, it is essential to develop a fundamental understanding of the basic physics that governs their behaviour in devices. The current research has shown that the concepts learned from bulk device physics do not simply carry over to nanotube devices, leading to unusual device operation. For example, the properties of bulk metal/semiconductor contacts are usually dominated by Fermi level pinning; in contrast, the quasi-one-dimensional structure of nanotubes leads to a much weaker effect of Fermi level pinning, allowing for tailoring of contacts by metal selection. Similarly, while strain effects in conventional silicon devices have been associated with mobility enhancements, strain in CNTs takes an entirely new perspective, with strain-induced bandgap and conductivity changes.

Moreover CNTs present a unique opportunity as one of the few systems where atomistic based modelling may reach the experimental device size, thus in principle allowing the experimental testing of computational approaches and computational device design. While similar approaches are under development for nanoscale silicon devices, the much different properties of CNTs require an entirely separate field of research.

In particular CNTs present extraordinary electronic properties, related to the ability to have a metallic or semiconducting behavior in relation to their geometry [3].

The scaling of electronic devices, particularly of silicon-based transistors, has always had a key role in electronic evolution: from tubes to transistors, to integrated circuits (IC), from small scale of integration to ultra very large scale of integration. At each generation the miniaturization allows to obtain higher speed, lower power dissipation, lower costs and higher number of gates on chip. Lithography, the key of miniaturization, has evolved steadily with continuous little jump together with a growing understanding of physical and industrial involved processes.

The smaller and smaller scaling approaches the time when the diffusion regions of transistors will be so close that the channel will be few atoms thick and gate oxide so thin that the charge will tunnel through it: this will be the ultimate size and performance of silicon-based devices.

Since we already move from microelectronic to nanoelectronic realm, the semiconductor industry and the whole scientific community are exploring a number of alternative device technologies. Some approaches involve moving away from traditional electron transport-based electronics: for example, the development of spin-based devices. Another approach, on which we focus here, maintains the operating principles of the currently used devices, primarily that of the field-effect transistor, but replaces the conducting channel with carbon nanomaterials such as one-dimensional (1-D) Carbon NanoTubes or two-dimensional (2-D) graphene layers [3].

These new devices, able to work better at nanometer scale, have molecular building block not coming from lithography and therefore, in order to describe electrons, holes, atoms, molecules and photons, for these devices it is necessary to use quantum electronics and not the well known differential equation for charge diffusion.

CNTFETs (Carbon Nanotube Field Effect Transistors) are novel devices that are expected to sustain the transistor scalability while increasing its performance. One of the major differences between CNTFETs and MOSFETs is that the channel of the devices is formed by Carbon NanoTubes (CNTs) instead of silicon, which enables a higher drive current density, due to the larger current carrier mobility in CNTs compared to bulk silicon. In particular, with CNTs we obtain good operation even at very high frequencies [1-11].

Among carbon nanotube FETs, conventional CNTFET is utilized for high-performance and low-power memory designs, also because this device has a significantly smaller off current which greatly reduces the power consumed at off state of CNTFET [4-11].

For this device we have already proposed a compact, semi-empirical model [5], in which we introduced some improvements to allow an easy implementation both in SPICE and in Verilog-A. Then our model has been implemented to carry out static and dynamic analysis of A/D circuits [12-15].

In this paper we review design criteria to evaluate the performance of typical A/D circuits based on CNTFET, both in SPICE, using ABM library, and in Verilog-A, using a semi-empirical compact model for CNTFETs already proposed by us [5]. The obtained results, with reference to a design of a phase shift oscillator, are the same in static simulations and comparable in dynamic simulations. However using Verilog-A the simulation run time is much shorter and the software is much more concise and clear than schemes using ABM blocks in SPICE.
Then we review a procedure in order to carry out static and dynamic analysis of basic digital circuits. In particular, to carry out the dynamic analysis, we consider both the quantum capacitance effects and the sub-threshold current. At last we analyze the timing performances of a NOT gate in order to define the optimal working conditions, emphasizing that the proposed method can be used to analyze the timing performance of any CNTFET-based logic gate.
The presentation of the paper is organized as follows. At first we present a brief review of our CNTFET model used in the proposed designs. Then we show and discuss the simulation results together with conclusions and future developments.

II. A BRIEF REVIEW OF OUR CNTFET MODEL

An exhaustive description of our I-V CNTFET model is in [5-6]. Therefore we suggest the reader to consult these References.
It is a compact, semi-empirical model directly and easily implementable in simulation software to design analog and digital circuits: in fact the most complex part of the model is contained in Verilog A [16].
With the hypothesis that each sub-band decreases by the same quantity along the whole channel length, the total drain current can be expressed as [5]:

$$I_{DS}=\frac{4qkT}{h}\sum_{p}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \tag{1}$$

where k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while ξ_{Sp} and ξ_{Dp}, depending on temperature through the sub-bands energy gap, and V_{CNT}, have the expressions reported in [5].
Regards to C-V model, an exhaustive description of our C-V model is widely described in [10] and therefore the reader is requested to consult it, in which the following expressions of quantum capacitances C_{GD} and C_{GS} are explained:

$$\begin{cases} C_{GD}=q\sum_{p}\frac{\partial n_{Dp}}{\partial V_{GS}}=q\sum_{p}\frac{\partial n_{Dp}}{\partial \xi_{Dp}}\frac{\partial \xi_{Dp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \\ C_{GS}=q\sum_{p}\frac{\partial n_{Sp}}{\partial V_{GS}}=q\sum_{p}\frac{\partial n_{Sp}}{\partial \xi_{Sp}}\frac{\partial \xi_{Sp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \end{cases} \tag{2}$$

In order to simulate correctly the CNTFET behaviour, we needed to estimate parasitic capacitances and inductances as well as the drain and source contact resistances.
In this paper we have achieved this goal using an empirical method [5] more suitable for simulations in CAD (Computer Aided Design) environment. This method requires the extraction of the previous parasitic elements comparing the device characteristics with the measured ones. In this way all elements of the equivalent circuit can be determined [5].
In this way all elements of the equivalent circuit of Fig. 1 can be determined.

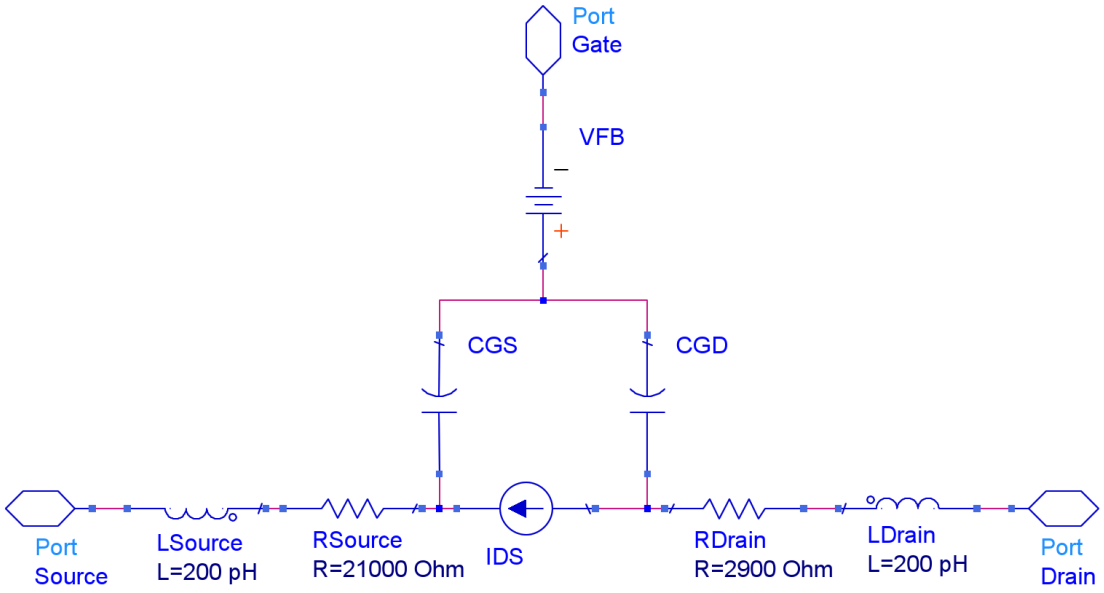

Figure 1. Equivalent circuit of n-type CNTFET.

It is similar to a common MOSFET one [17] and is characterized by the flat band generator V_{FB}, the quantum capacitances C_{GS} and C_{GD} , the inductances of the CNT L_D and L_S and the resistors R_D and R_S, in which the parasitic effect due to the electrodes are also included.

III. MODEL IMPLEMENTATION BOTH IN SPICE AND IN VERILOG-A

Prediction through modelling is the basis of engineering design. The computational power at the fingertips of the professional engineer is increasing enormously and techniques for computer simulation are changing rapidly. Engineers need models which relate to their design area and are adaptable to new design concepts. They also need efficient and friendly ways of presenting, viewing and transmitting data associated with their models.

A device model is considered a *compact* model because of the methods used to develop the equations and coefficients used for the electrical representation of the physical behaviour of a device. The word *compact* is used because these equations are simplified based upon several assumptions made when developing the model equations. On the other hand the availability of accurate, robust, and efficient compact models is critical to the successful utilization of any circuit simulation tool.

The most common simulation tool for a designer is SPICE (Simulation Program with Integrated Circuit Emphasis), originally introduced in early 1970s by the University of California, Berkeley.

In the reviewed procedure we have used SPICE as implemented in ORCAD, working in graphic mode. However, since the expressions describing our device are not compatible with those of devices available in the SPICE models, the model of Fig. 1 could not be described by an equivalent circuit including simple devices as resistances, inductances, capacitances, diodes and transistors. Therefore we have used the ABM library, one of ORCAD libraries, which implements many non linear expressions: in this way we are able to characterize our model with the correct drain current equations and the correct capacitance effects depend on bias voltages. Using ABM library, all expressions can be written as electrical circuits and therefore, during SPICE simulation, all intermediate results are expressed in voltages or currents.

In the SPICE simulations, however, we have found several problems:

1) any voltage over 10^9 V triggers an overflow error by SPICE and therefore all model expressions must be scaled to avoid overcoming this limit in any connection;
2) the gate-drain and gate-source capacitances, depend on bias voltages, can be obtained either as integral of current or as derivative of voltage. In the first case we introduce integration errors because of very small values of currents and time steps, while, in the second case, we introduce noise coming from derivative calculation;
3) the schematic used to simulate the CNTFET model was so large that we have decided to use

the capacitances dependent only on the first band, which is the dominant component of capacitances at low voltages;

4) Debugging of formulae, expressed with schematics, has been very difficult.

The previous problems have led us to utilize Verilog-A language [16], which is a part of Verilog-AMS, a high level description language for Analogue and Mixed Signal circuits.

For model developers accustomed to working in a standard programming language such as C, the switch to Verilog-A syntax should be straightforward and painless. The language is relatively succinct and compact, and is well-suited to analog model development. Nowadays several academic and industrial model development groups use Verilog-A as a key part of their development methodology.

Verilog-A language has a syntax that recalls in many aspects that of C and, for the numerical expressions, it has a mathematical library very similar to that of C. However one of the main difference from C syntax is the "*contribution operator*" (<+), which is used to accumulate currents or voltages. Moreover, in our case, an important element of Verilog-A syntax has been the presence of "*parameter*" which could be set at run time: in this way we set nanotube diameter, length, number of electronic bands (to be accounted for current) and the kind of doping.

For example, for doping, the instruction line is:

```
parameter real doping = +1      from [-1,+1] ;  // +1 p-type, -1 n-type
```

This last parameter was used avoiding, in this way, to duplicate code for n-type and p-type CNTFET.

In proposed procedure we use Verilog-A to describe the CNTFET in the ADS environment, while the rest of circuit was drawn with standard ADS libraries. After compiling the Verilog-A source, during the simulation, ADS calls the Verilog-A program to obtain values for the circuital equations.

This organization of the work has presented the following advantages:

1) the model source code is independent of the simulator and it can be used on any simulator which has a Verilog-A compiler and interface;
2) the values of the device voltages or currents are computed by expression which are calculated using the mathematical library with high precision and in a very short time;
3) since we have no more the model expressions split in a graph of several elemental analogue blocks as with ABM in SPICE, the number of equations to be solved at each simulation step is widely reduced with important gain in speed and precision of the simulation;
4) the mathematical computation works in standard double precision, overflow errors are those standard to double precision, and there is no need to rescale variables;
5) during the simulation it is possible to trace the behaviour of intermediate expression in the Verilog-A program as it was possible with SPICE, but in Verilog-A it is also possible to obtain code controlled messages and to dedicate more space to the debugging code;
6) the complexity of the code is tiny compared to the complexity of the schemes used to reproduce expression with ABM blocks in SPICE and this allows us to implement the complete model in all details. The code results more clear and well organized and the programming errors are widely reduced;
7) since the code is simple and fast, there is space to implement also some mathematical optimizations to enhance the numerical precision. In the model we have implemented several times expressions of the form ln[1+exp(x)] which suffers of a progressive lost of precision for x < -13, so we implemented the following code based on the Taylor approximation:

```
if (x < -13)
    begin
         ex = exp(x) ;
         f = ex*(1-ex/2) ;
    end
 else
    f = ln(1+exp(x)) ;
```

8) the gate-drain and gate-source capacitances, controlled in voltage, are implemented only in a couple of lines of code:

```
icgs = ddt(cgs*vgs) ;
icgd = ddt(cgd*vgd) ;
```

9) we obtain a speed gain up to 100 compared to our model on ABM SPICE library, since any simulation requests few seconds unlike the SPICE version, in which several minutes are necessary for simulation.

Fig. 2a compares the I_{DS} – V_{DS} characteristics (denoted by continuous lines) of numerical simulations with Verilog-A language and the experimental ones [18] (denoted by ●), in which we have assumed the same values for V_{FB}, CNT diameter, R_D and R_S reported in [18], while Fig. 2b compares the same with SPICE.

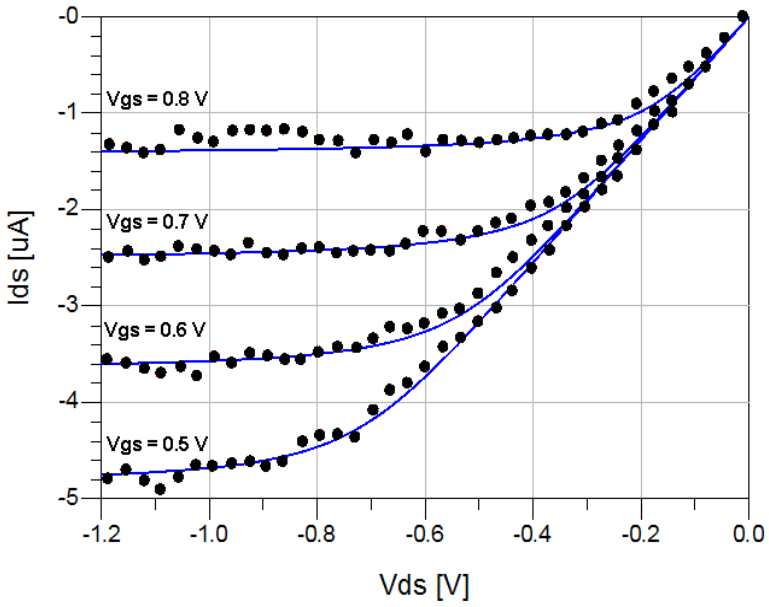

Figure 2a. Simulated I_{DS} – V_{DS} characteristics (denoted by continuous lines) with Verilog-A and experimental I_{DS} – V_{DS} characteristics [18] (denoted by ●).

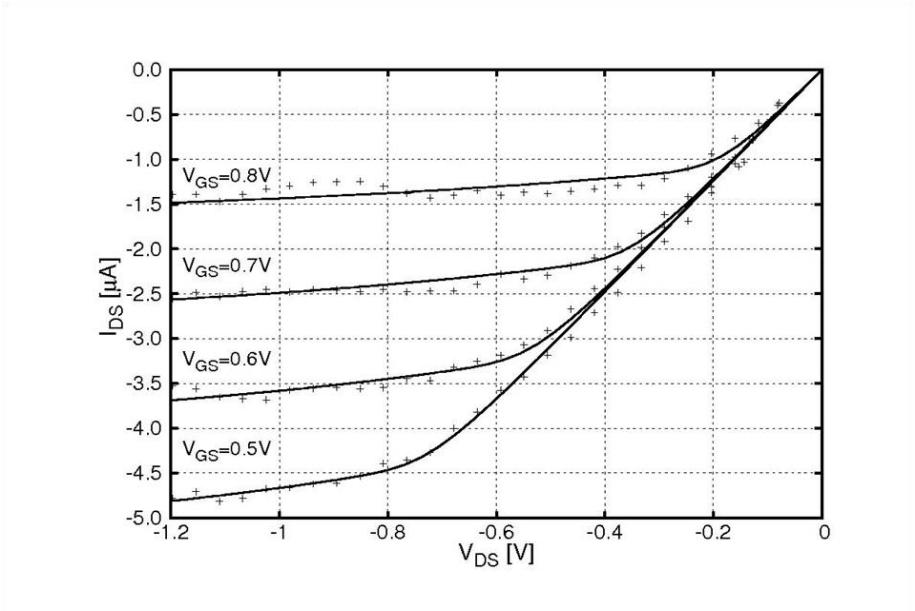

Figure 2b. Simulated I_{DS} – V_{DS} characteristics (denoted by continuous lines) with SPICE and experimental I_{DS} – V_{DS} characteristics [18] (denoted by +).

It is easy to see that the obtained results are practically the same in static simulations. In particular the small difference around the knees of the I-V characteristics is due to the implementation issues, because in SPICE we have implemented a simplified formula using SOFTLIM block from the ABM library, unlike Verilog-A.

However the implementation of the gate-drain and gate-source capacitances has been different in SPICE and in Verilog-A, because in SPICE only one band in the capacitance model has been considered.

Figures 3a and 3b show the implementation of the gate-drain and gate-source capacitances respectively using our C-V model in Verilog-A language, in which we have assumed V_{FB} = 0 V, CNT diameter d = 1.4 nm, $R_D = R_S = 0\ \Omega$ and $C_{ox} = 3.8$ pF/cm .

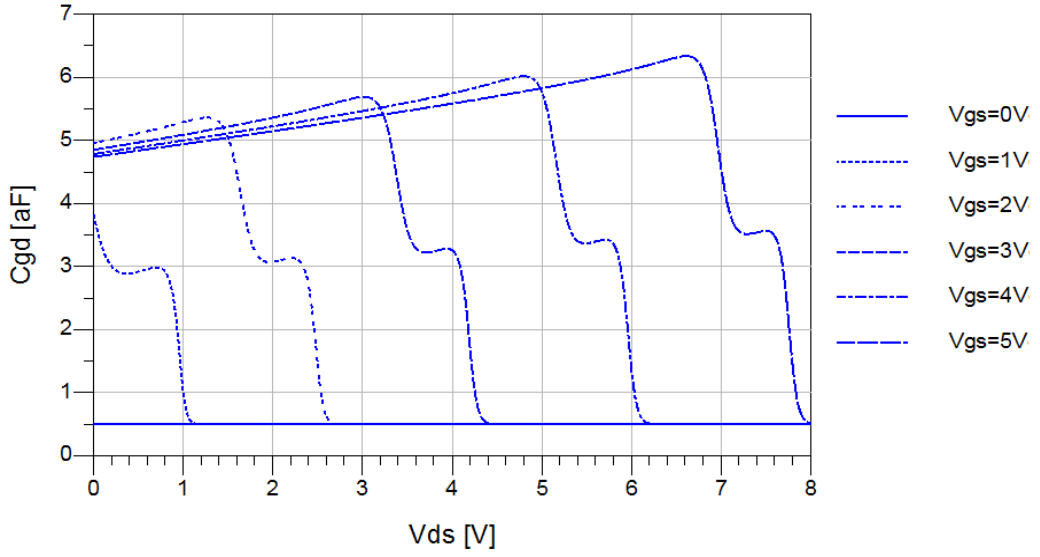

Figure 3a. Simulations of C_{GD} vs V_{DS} for different values of V_{GS} in Verilog-A.

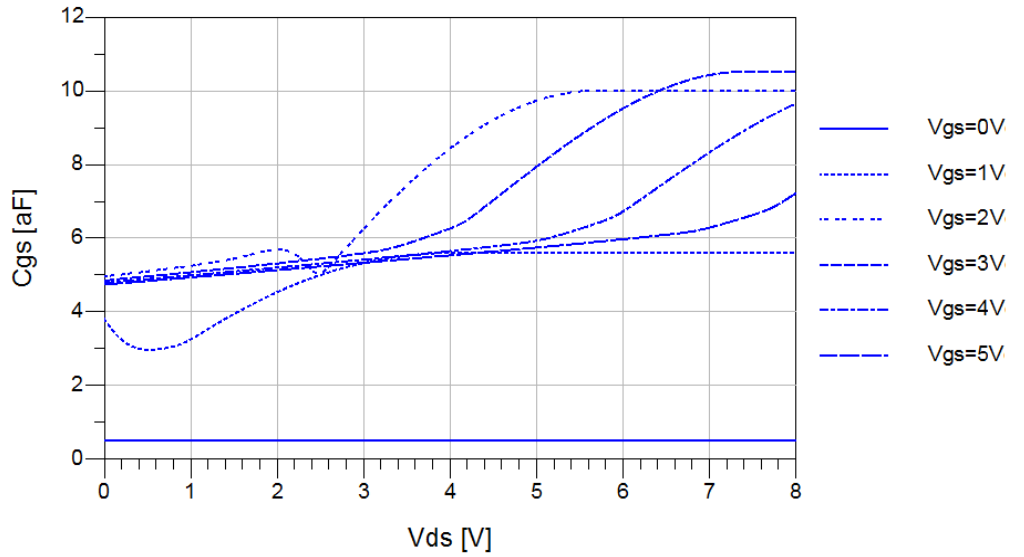

Figure 3b. Simulations of C_{GS} vs V_{DS} for different values of V_{GS} in Verilog-A.

The implementation of the same capacitances in SPICE has been reported in [19], where we have obtained different values of gate-drain and gate-source capacitances, because in SPICE only one band in the capacitance model has been considered.

In particular, the difference between the capacitance models comes from some simplifications we have adopted in our SPICE model [19], in order to do not weigh down the software further, unlike Verilog-A implementation.

However these differences have no influence on I-V characteristics, which are practically the same, as illustrated previously.

IV. EXAMPLE OF ANALOG CIRCUIT: PHASE-SHIFT OSCILLATOR

In all following simulations we have considered CNTFETs having a diameter of 1.42 nm, length of 100 nm and quantum capacitances depending on polarization voltages.
Fig. 4 shows a phase-shift oscillator, which includes three identical RC networks.

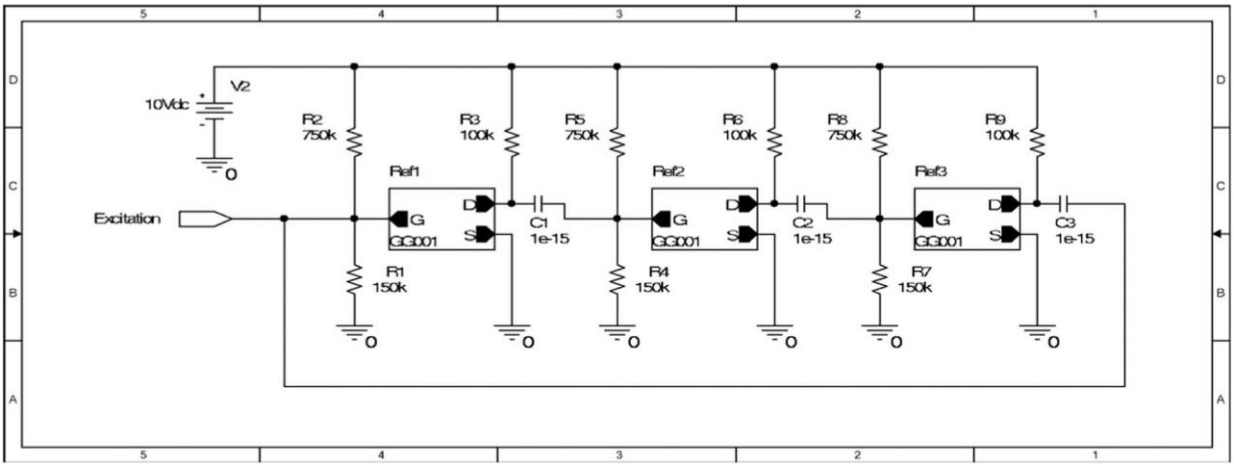

Figure 4. Phase-shift oscillator employed three CNTFETs.

In Fig. 5 we have reported the output voltage of Verilog-A simulation, while in Fig. 6 the same obtained with SPICE.

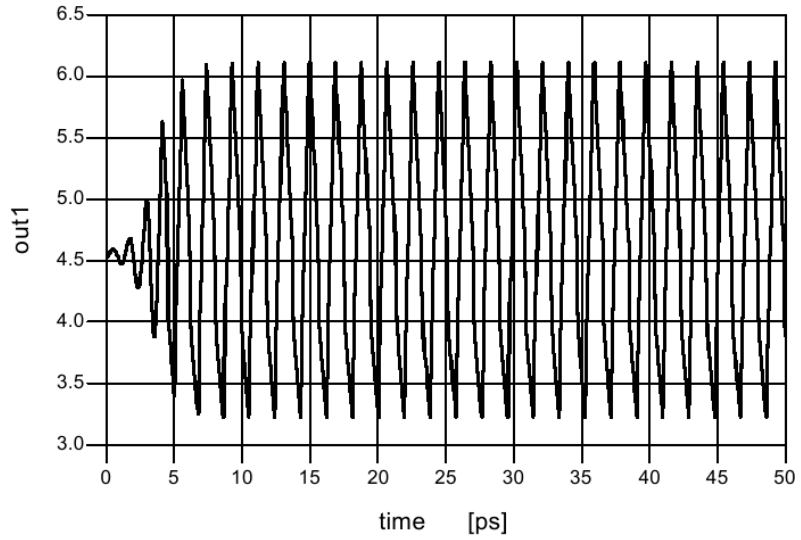

Figure 5. Output voltage of Verilog-A simulation for the phase-shift oscillator.

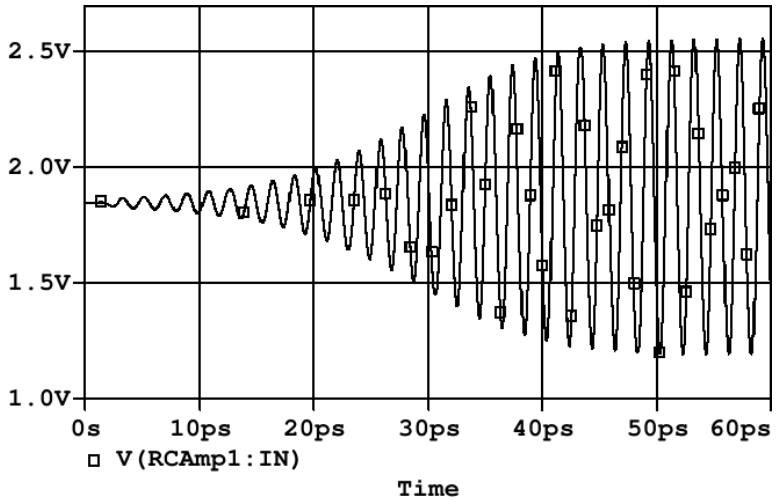

Figure 6. Output voltage of SPICE simulation for the phase-shift oscillator.

This simulation shows a small differences for the oscillation frequency (0.5 THz for SPICE [9-10], 0.53 THz for Verilog-A) and a larger difference in amplitude (1.3 V for SPICE, 2.9 V for Verilog-A). We think that these differences are mainly due to the fact that in the SPICE implementation it has been considered only one sub-band for the capacitance model, while in our Verilog-A implementation the number of sub-bands p can be defined as a parameter settable by the user. In particular we have set p equal to 3.

Moreover in Verilog-A it has been necessary to reduce the supply voltage, and therefore to modify the circuit, in order to reduce the parasitic gate source capacitances, while, since under SPICE the oscillator was pushed to the highest frequency, the circuit became very sensible to the model parameter variations.

However, using Verilog-A implementation the development time in writing the model is shorter, the simulation run time is much shorter and the software is much more concise and clear than schemes using ABM blocks in SPICE.

Although SPICE has still an huge importance in the electronic design. since a great number of commercial devices are described by SPICE models and major chip producer distribute their simulation libraries for SPICE, we think that Verilog-A is an useful tool to help circuit designers to devise these very new nascent architectures, although its diffusion is still very limited and nowadays most of its libraries are dedicated to RF [20].

V. EXAMPLE OF DIGITAL CIRCUIT: NOT GATE

Static Analysis

Referring to an inverter, for a static analysis we can determine the voltage transfer characteristic, VTC (Fig. 7), and then the noise margins, which provide a measure of the maximum external voltage noise that can be overlapped to the input signals, without causing unwanted output variation.

The noise margins, whose values are necessary in the design of digital circuits, are determined from the -1 slope points on the VTC, indicated by the letters A and B in Fig. 7, which delimit the amplification range of the device. V_{OH} and V_{IL} (point A) represent respectively the valid minimum output voltage at high level and the valid maximum input voltage at low level. Similarly V_{OL} and V_{IH} (point B) the valid maximum output voltage at low level and the valid minimum input voltage at high level.

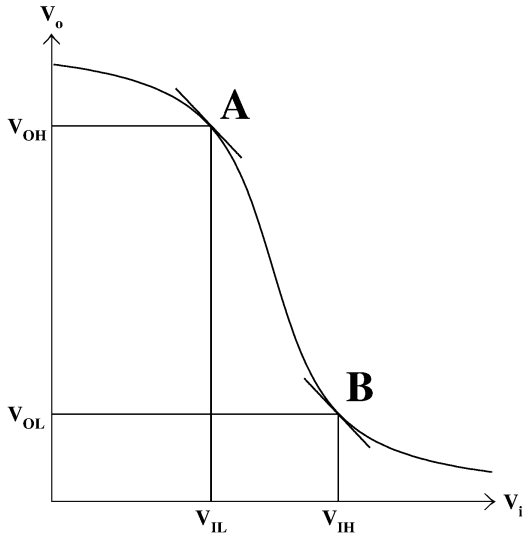

Figure 7. Voltage transfer characteristic for an inverter.

The noise margins are defined as follows:
$NM_H = V_{OH} - V_{IH}$ for high voltage
and
$NM_L = V_{IL} - V_{OL}$ for low voltage.
When the input voltage V_I is between V_{IL} and V_{IH}, the logic gate is in an undefined state, which is an operative condition that we must avoid to make sure the logic levels are within well defined regions.
The schematic of NOT gate implemented by Verilog-A language is shown in Fig. 8.

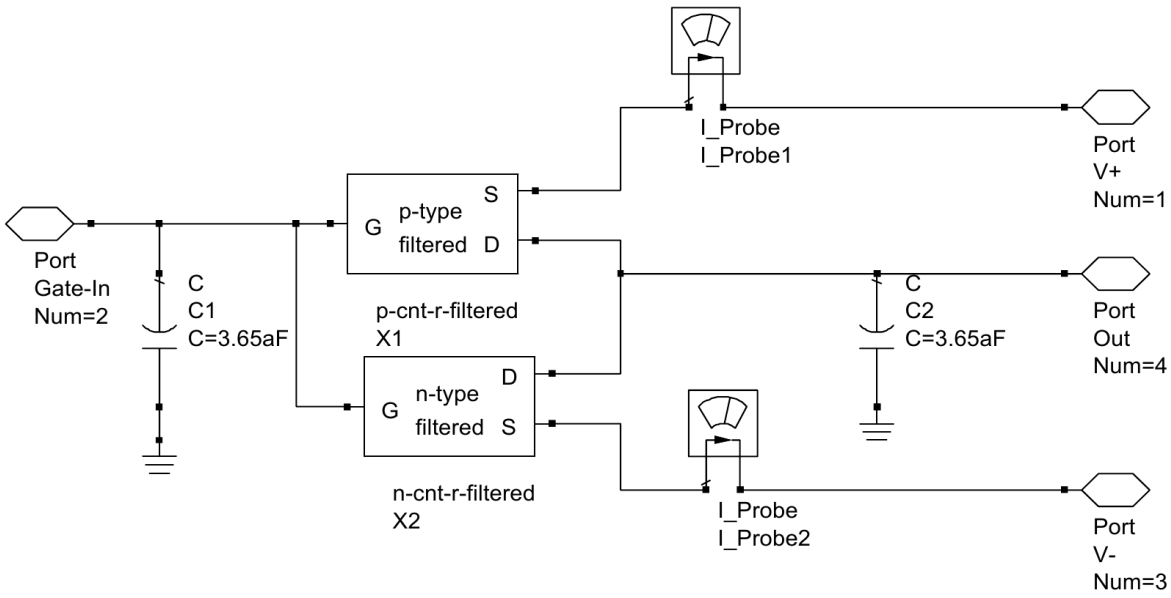

Figure 8. Schematic of a NOT gate.

The gate consists of two MOS-like CNTFETs with n and p channel respectively.
In Fig. 8 Gate-in and Out indicate the input and the output of the gate, while V+ and V- indicate the positive and negative power supply terminals. Two current probes have been introduced to evaluate static currents flowing through the two CNTFETs.

Finally, two capacitors have been introduced to model the capacitance of the metallic interconnections with respect to ground, which have no influence in static performance, but in dynamic analysis are important for new measurement technology.
In order to perform a static analysis, we have used the circuit reported in Fig. 9, which shows a cascade of five NOT gates, which are internally composed as in Fig. 8.

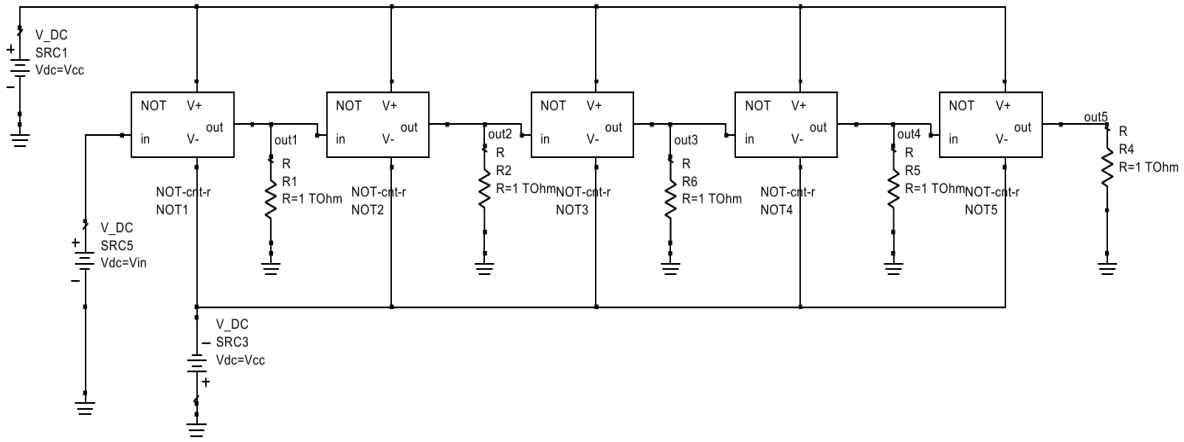

Figure 9. Schematic of a cascade of five NOT gates.

A dual power supply is used and a constant voltage source V_{in} is connected to the input of the first gate and varies from $-V_{CC}$ to $+V_{CC}$ (V_{CC} varies from 0.1V to 1V with step 0.1V).
In Fig. 10 we have reported the simulated static currents of the first gate of the cascade. These currents give an indication of the static power dissipation in the circuit, which is a very important factor for high integration density circuits.

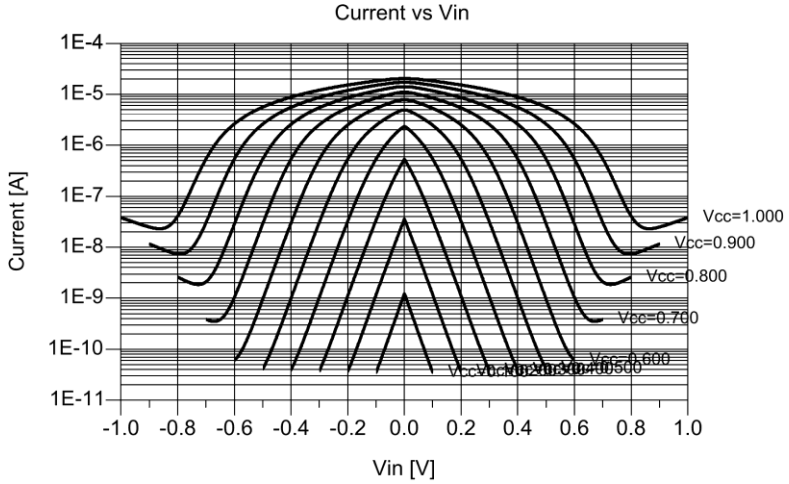

Figure 10. Static currents of the first NOT gate vs V_{in}, with V_{CC} varying from 0.1 V to 1.0 V.

Current peacks in the high gain region (near V_{in} = 0 V) are to be observed, because in this region the two CNTFETs of the NOT gate are both in the on state and they are saturated. A conducting path between the positive and negative power supply is determined and relatively high currents can flow. We can see that the current decreases in the regions where the gate state is well defined, i.e. the states where the input signal is recognized as low or high level. In these regions, where one transistor is turned on and the other one is turned off, the static current that flows between the positive and negative supply is due to the tunnel effect in the interdicted transistor.
As we said previously, noise margins are determined from the -1 slope points on the VTC. This slope is the gate gain and can be determined using the circuit of Fig. 11.

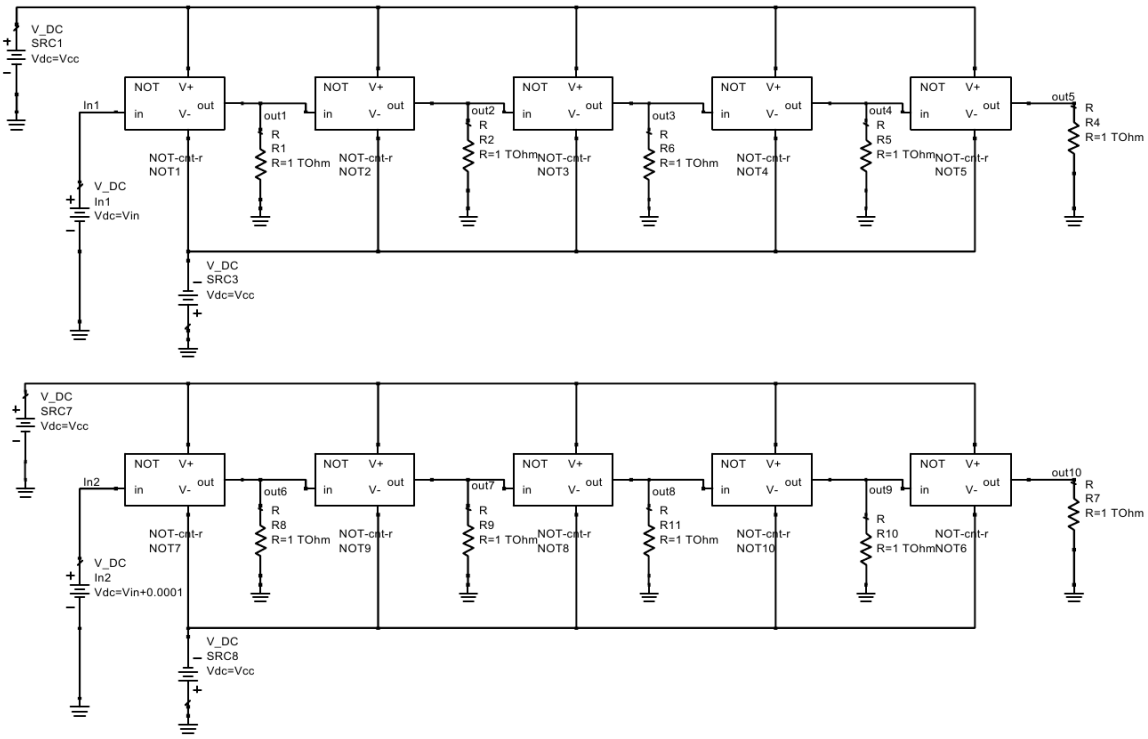

Figure 11. Circuit used to calculate NOT gain.

In particular Fig. 11 shows two identical circuits in which the lower one presents an input voltage increased by ΔV_{in} = 0.1mV with respect to the upper circuit. Referring to the first gate of the cascade, considering the difference between the outputs of the lower and upper circuit and dividing that by ΔV_{in} we obtain the gate gain.
Fig. 12 shows the gain diagrams of NOT1 gate as function of input voltage.

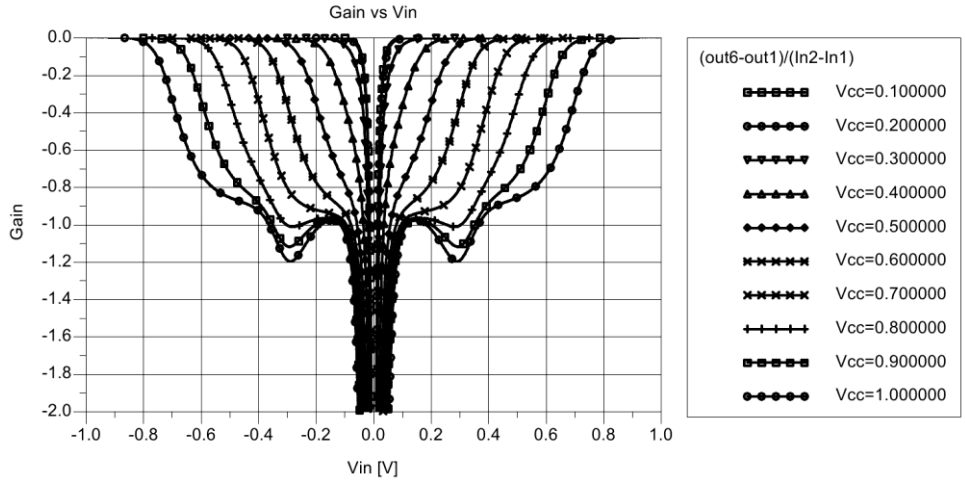

Figure 12. Gain of the first NOT of the cascade vs V_{in} with V_{CC} varying from 0.1 V to 1.0 V.

Similarly, plotting the gain as function of the output voltage of the first gate, we obtain V_{OH} and V_{OL}, which are the output voltage values when the gain is -1.
The results are shown in Fig. 13.

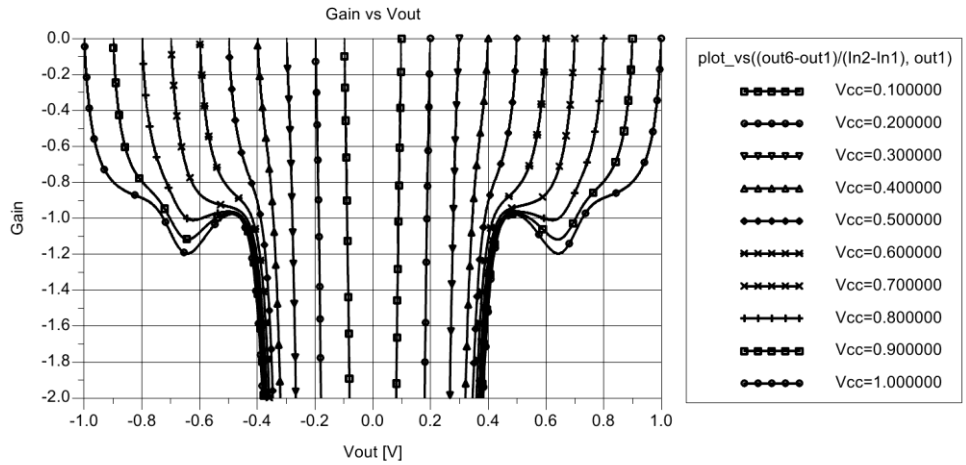

Figure 13. Gain of the first NOT of the cascade vs V_{out} with V_{CC} varying from 0.1 V to 1.0 V, step 0.1.

Table 1 summarizes the simulation results, where we have reported the V_{IH}, V_{OL}, V_{IL}, V_{OH} values and the noise margins NM_H and NM_L for different values of V_{CC}.

TABLE 1. Noise margins and -1 slope points (our model).

V_{CC} [V]	V_{IH}[V]	V_{OL}[V]	V_{IL}[V]	V_{OH}[V]	NM_H	NM_L
0,1	0,014	-0,089	-0,014	0,089	0,075	0,075
0,2	0,014	-0,188	-0,014	0,188	0,174	0,174
0,3	0,019	-0,278	-0,019	0,278	0,259	0,259
0,4	0,0357	-0,345	-0,0357	0,345	0,3093	0,3093
0,5	0,0578	-0,388	-0,0578	0,388	0,3302	0,3302
0,6	0,076	-0,419	-0,076	0,419	0,343	0,343
0,7	0,095	-0,439	-0,095	0,439	0,344	0,344

Dynamic Analysis

To analyse the dynamic behaviour of a logic gate, for example an inverter, the parameters of interest are the propagation delay and the rise and fall times (see Fig.14).

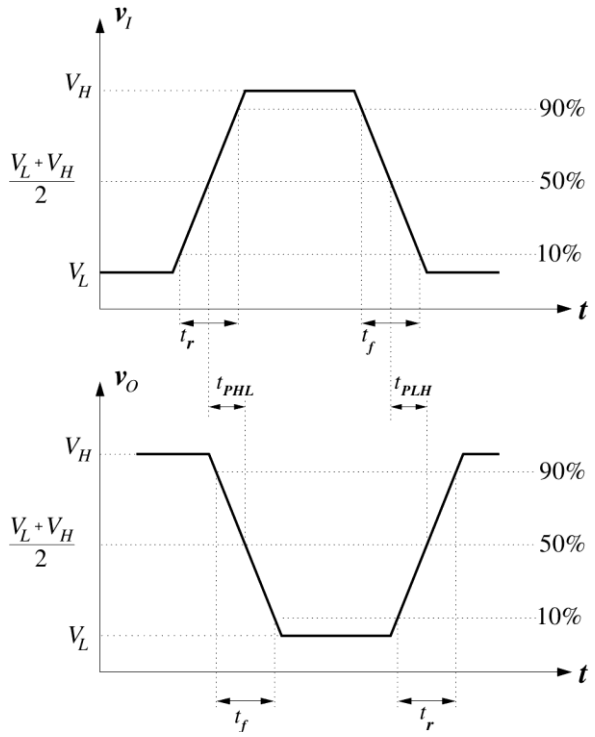

Figure 14. Time and voltage definitions for input and output waveforms [19].

The rise time t_r for a given signal is defined as the time required for the signal to make the transition from the 10% point to the 90% point on the waveform, during the V_L-V_H transition.
Similarly, the fall time t_f is defined as the time required for the signal to make the transition between the 90% point and the 10% point on the waveform, during the V_H-V_L transition.
The 10% and 90% points are defined as follows:
$V_{10\%} = V_L + 0.1\Delta V$
$V_{90\%} = V_L + 0.9\Delta V$
where $\Delta V = V_H - V_L$ is the logic swing, V_H and V_L are the high and low logic levels respectively.
The **propagation delay τ_P** is defined as the difference in time between the input and output signals reaching the 50% points in their respective transitions. The 50% point is the voltage level corresponding to one-half the total transition between V_H and V_L: $V_{50\%} = (V_H + V_L)/2$
We indicate propagation delay on the high-to-low output transition with τ_{PHL} and that of the low-to-high transition with τ_{PLH}.
The schematic of NOT gate implemented by Verilog-A language has been already shown in Fig. 8.
In order to perform a dynamic analysis, we have used the circuit reported in Fig. 9, already illustrated.
Parasitic capacitors have been introduced on the outputs of the gates to model the capacitance to ground of the metallic interconnections between gates. The input of the first gate is connected to an impulsive voltage generator that provides a binary signal with high level equal to $+V_{CC}$ and low level equal to $-V_{CC}$, rise and fall times equal to 1.78 ps (**slow transitions**), high level duration of 16 ps and period equal to 38 ps. The rise and fall times have been chosen to give in input a typical signal of the logic, with features similar to the output signal of the cascade. For the following simulations we use a voltage supply V_{CC} = 0.4V, which determines the values of the high and low logic levels. In particular we chose a simulation time equal to 80 ps that allows to view the complete waveforms at the outputs of the gates.
Fig. 15 shows the result of simulation for slow transitions.

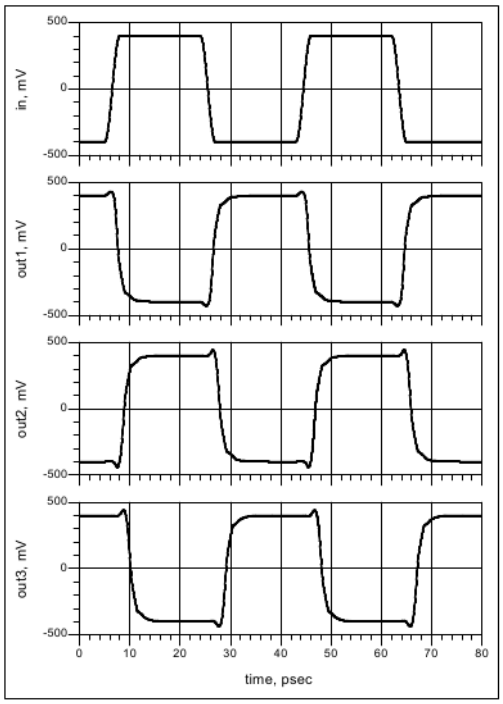

Figure 15. Output of the first four NOT gates and input signal vs time for slow transitions.

Figs. 16 and 17 allow to determine the propagation delays for the high-to-low and low-to-high transitions respectively.

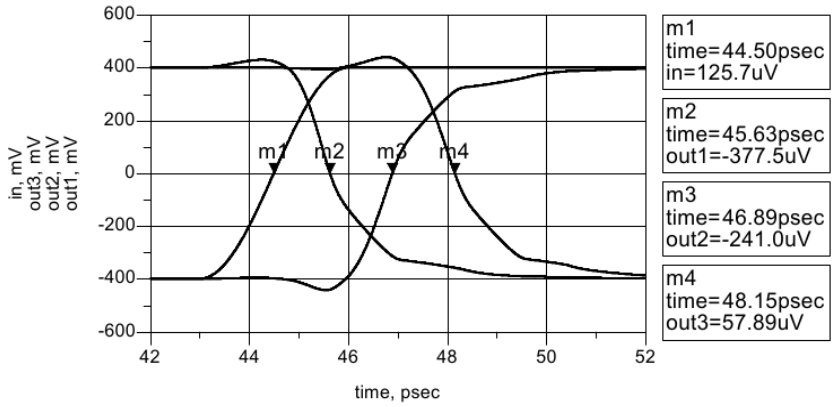

Figure 16. Input and output of transients of the NOT gates for high-to-low transitions.

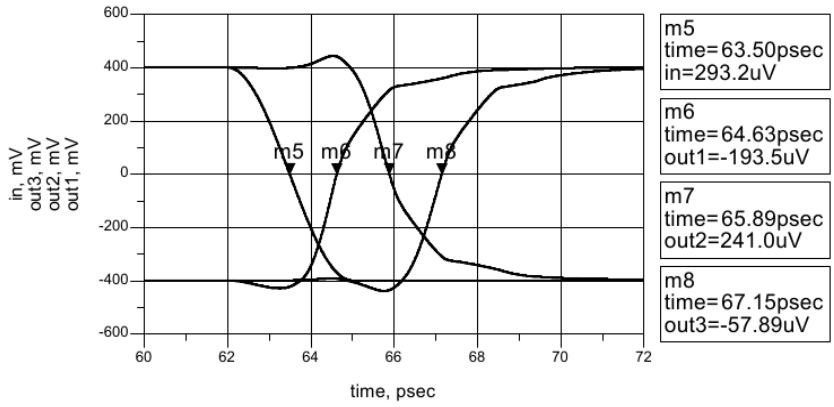

Figure 17. Input and output of transients of the NOT gates for low-to-high transitions.

On these diagrams we have superposed some markers in order to determine the times corresponding to the 50% points of the transitions. The 50% points are equal to 0 V. In this way we can easily determine the propagation delays τ_{PHL} and τ_{PLH}, applying the definitions mentioned before. For example, for the first NOT gate we obtain:

$\tau_{PHL1} = t_{m2} - t_{m1} = 45.63$ ps $- 44.50$ ps $= 1.13$ ps

$\tau_{PLH1} = t_{m6} - t_{m5} = 64.63$ ps $- 63.50$ ps $= 1.13$ ps

Moreover Figs. 18 and 19 allow to evaluate the rise and fall times of the input and output signals at the first NOT of the cascade respectively.

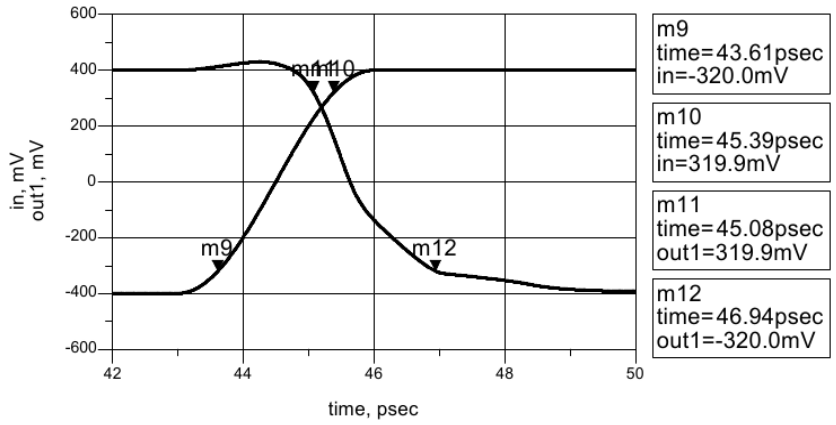

Figure 18. Input and output of transients of the first NOT gate for high-to-low transitions.

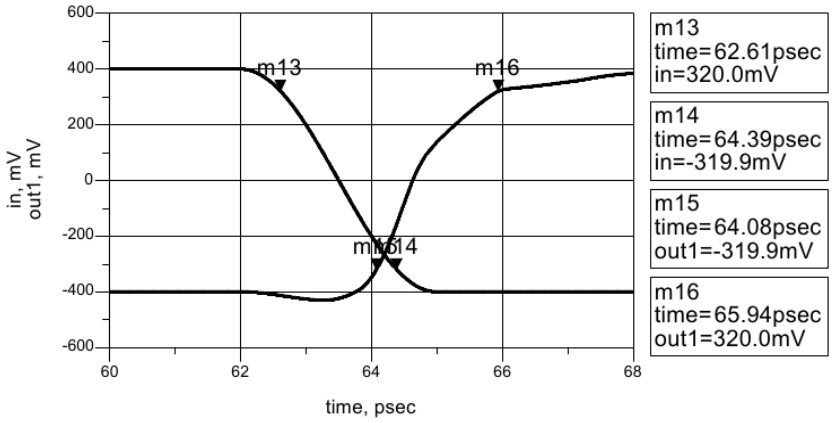

Figure 19. Input and output of transients of the first NOT gate for low-to-high transitions.

The markers on the diagrams have been positioned at the 10% and 90% points of the level transition: in this way it is possible to determine easily the rise times t_r and the fall times t_f in the following way:

$V_{10\%} = V_L + 0.1\Delta V = -400$ mV $+ 0.1 \cdot 800$ mV $= -320$ mV

$V_{90\%} = V_L + 0.9\Delta V = -400$ mV $+ 0.9 \cdot 800$ mV $= 320$ mV

where $\Delta V = V_H - V_L = 400$ mV $- (-400$ mV$) = 800$ mV

Corresponding to the markers, it is possible to read the times referring to these points and, therefore we can determine the rise times t_r and the fall times t_f. which refer to the input and output signals.

For example, for the first gate:

$t_{r1} = t_{m12} - t_{m11} = 47.43$ ps $- 45.15$ ps $= 2.28$ ps

$t_{f1} = t_{m16} - t_{m15} = 66.43$ ps $- 64.15$ ps $= 2.28$ ps

In order to evaluate the dynamic currents due to not instantaneous transition of the input signal of the gate, it is necessary observe that, during the level transition of the input signal, for a short time, both the CNTFETs are saturated. This happens when the signal leads the gate to the transition region. Therefore, a conducting path between the positive and negative supply exists and a certain current can flow through that path.

Performing the simulation for the first NOT of the cascade we obtain the diagram shown in Fig. 20

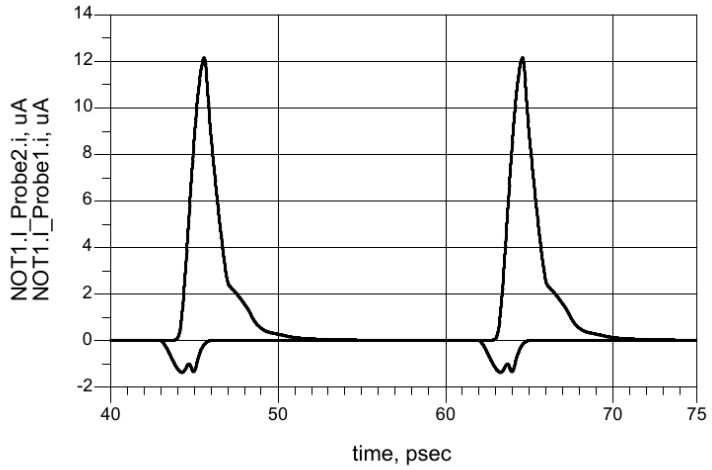

Figure 20. Dynamic currents flowing through the first NOT gate.

The n-channel CNTFET current corresponds to the first positive peak, while the p-channel CNTFET current corresponds to the first negative peak. The situation is inverted for the current peaks at 65 ps.
When the input signal at the first gate passes from the low level to the high level, the p-CNTFET turns off, whereas the n-CNTFET turns on. The load capacitance on the output of the gate, initially at high voltage level, discharges through the n-CNTFET, turned on, determining a current peak through this device which lasts for the time necessary to discharge the capacitance.
Similarly, when the input signal at the first gate passes from the high level to the low level, the n-CNTFET turns off, whereas the p-CNTFET turns on. The load capacitance starts to charge through the p-CNTFET, therefore the output passes from the initially low level to the high level, at the end of the transient. The current peak, in this case, flows through the p-CNTFET and lasts for the time necessary to charge the load capacitance.
We have repeated the proposed procedure to analyze the dynamic behaviour of NOR gate, but, in order not to weigh the treatment, we limit ourselves to report the obtained results, i.e. $\tau_{PHL1} = 2.14$ ps, τ_{PLH1} 3.72 ps, t_{r1} 8.91 and $t_{f1} = 4.58$ ps.
All simulations were carried out in ADS on an Asus X5DIJ computer which uses an Intel Pentium dual core T4200 processor running at 2 GHz, with 1 MB cache and 4 GB of RAM memory. Moreover we have obtained a compilation time of 2.69 s and a run time of 58.84.

Analysis of timing performance of NOT gate

At last in Fig. 21 we show the circuit used to analyze switching time and power dissipation of CNTFET-based NOT gate, in order to define the optimal working conditions.

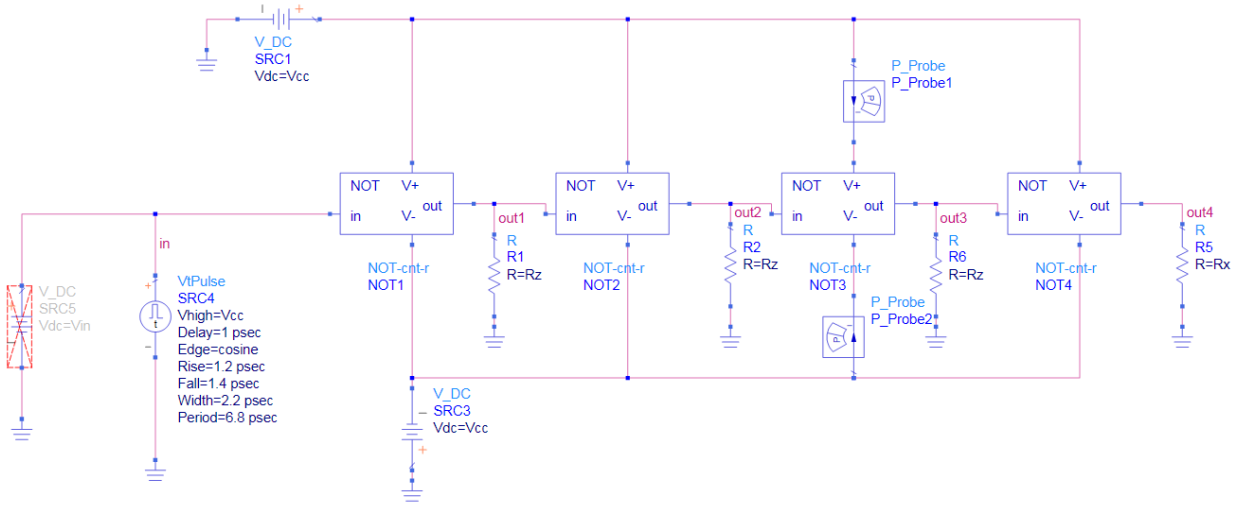

Figure 21. Circuit used to analyze switching time and power dissipation of CNTFET-based NOT gate.

The gate under test is the third and the output considered is the out3 node. The previous gates are necessary to generate a typical input signal and the following to simulate an appropriate load. The first NOT gate is stimulated by a pulse generator whose parameters are adjusted to produce a square wave with 50% duty cycle. The rise/fall time of the pulse generator was chosen with this procedure: first, a very small rise time was set (0.3 ps); then, the rise time at out1 node was measured and finally this rise time was set for the pulse generator.

This way we provide an input signal which is as similar as possible to the output signal of a NOT gate.

Quantities measured at the out3 node are rise time (t_R), gate delay (t_{HL}) in relation to out2 and energy per switching. This last quantity was obtained by integrating over time power dissipated by gate under test and measuring the energy used in one period, which is the sum of energy dissipated for H→L and L→H transitions.

The obtained results are shown in Figs. 22, 23 and 24.

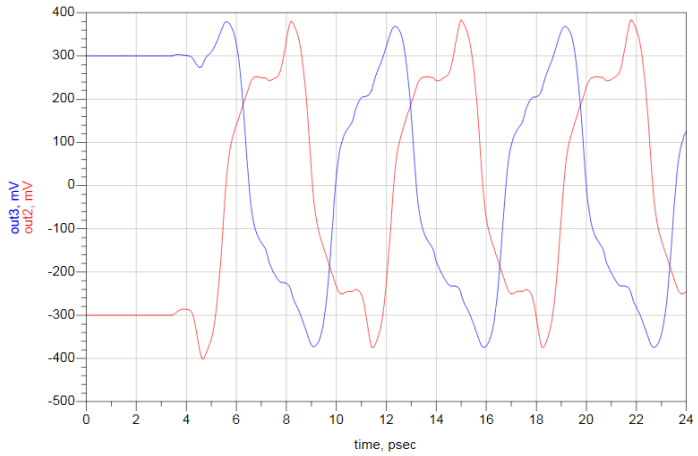

Figure 22. Out3 and out2 versus time.

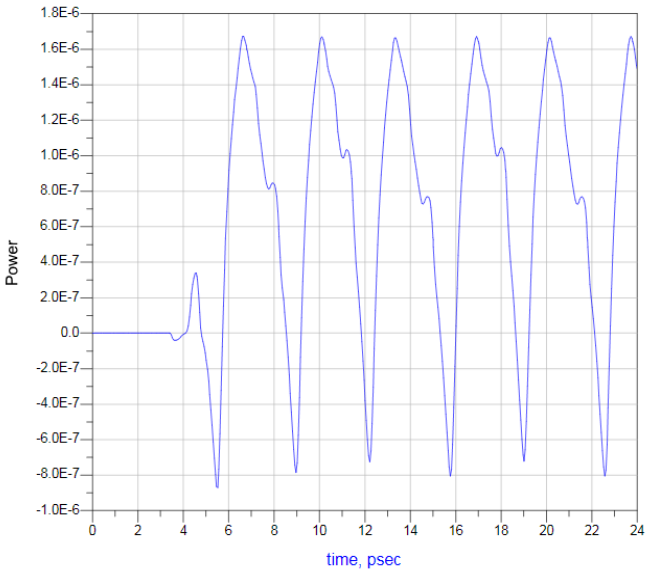

Figure 23. Power absorbed by gate versus time.

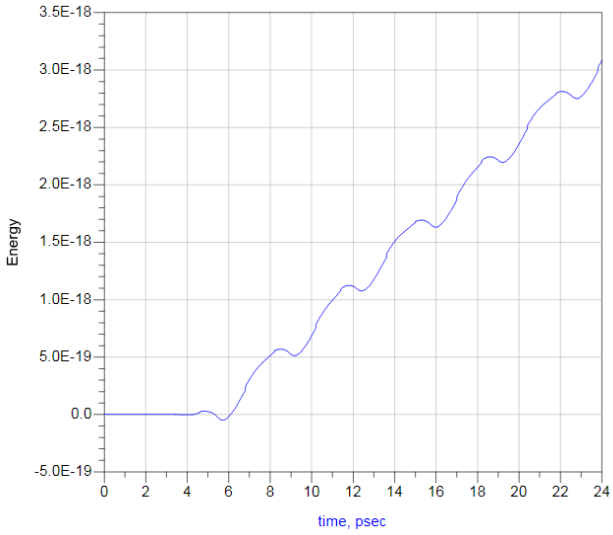

Figure 24. Energy absorbed by gate versus time.

The analysed procedure, examined for NOT gate, can be used to analyze the timing performance of any CNTFET-based logic gate.

VI. CONCLUSION AND FUTURE DEVELOPMENTS

In this review we have illustrated design criteria to evaluate the performance of typical analog and digital (A/D) circuits based on CNTFET, both in SPICE, using ABM library, and in Verilog-A, using a semi-empirical compact model for CNTFETs already proposed by us. The obtained results, with reference to a design of a phase shift oscillator, as example of analog circuit, have been the same in static simulations and comparable in dynamic simulations. However using Verilog-A the simulation run time is much shorter and the software is much more concise and clear than schemes using ABM blocks in SPICE.

Then we reviewed a procedure in order to carry out static and dynamic analysis of basic digital circuits. In particular, to carry out the dynamic analysis, we considered both the quantum capacitance effects and the sub-threshold current. At last we analysed the timing performances of a NOT gate in order to define the optimal working conditions.

Actually we are working to study the effect of noise [21] and of temperature [22-25] in the CNTFET-based design of A/D circuits, considering also other models of CNTFET proposed in literature [26-27].

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