A COMPARATIVE STUDY OF CNTFET AND MOSFET DEVICES THROUGH THE DESIGN OF CURRENT MIRRORS

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ABSTRACT

In this review we present a comparative study of CNTFETs and MOSFET devices, through the design of self-biased cascode current mirror.
In particular, the CNTFET used is a C-CNTFET and the MOSFET is in 32 nm technology to have comparable results. All simulations are performed in Advanced Design System, which is compatible the Verilog-A programming language. The obtained results show the overall improvement of the performance of the current mirror based on CNTFET with a higher output resistance without being disadvantaged in terms of current gain.

KEYWORDS: *CNTFET, MOSFET, Modelling, Current Mirror, Advanced Design System (ADS).*

I. INTRODUCTION

Carbon NanoTube Field Effect Transistors (CNTFETs) use a carbon nanotube as channel and work better at nanometer scale, ultimate limit in miniaturization [1-7].
In particular conventional CNTFETs (C-CNTFETs) are utilized for high-performance and low-power memory designs, also because this device has a significantly smaller off current which greatly reduces the power consumed at off state of CNTFET [8-9].
For this device we have already proposed a compact, semi-empirical model [2-8], in which we introduced some improvements to allow an easy implementation both in SPICE and in Verilog-A, in order to carry out static and dynamic analysis of A/D circuits [10-18].
In this review we present a comparative analysis of CNTFETs and MOSFET devices through the design of current mirrors. In order to have comparable results, we refer to C-CNTFET and a MOSFET in 32 nm technology.
The software used is Advanced Design System (ADS) which is compatible with the Verilog A programming language. The simulations allow to show the differences between CNTFET and MOS technology.
The presentation of the paper is organized as follows. At first we present a brief review of the CNTFET and MOSFET models. Then we show and discuss the simulation results together with conclusions and future developments.

II. A BRIEF REVIEW OF CNTFET AND MOSFET MODEL USED

An exhaustive description of our CNTFET model is in [14-18]. Therefore, we suggest the reader to consult these References.

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It is a compact, semi-empirical model directly and easily implementable in simulation software to design A/D circuits: in fact, the most complex part of the model is contained in Verilog A [19].
We have considered a single wall n-CNTFET in the ballistic transport hypothesis. This assumption allowed to define an analytical formula for CNT current.
When a positive voltage V_{GS} is applied between gate-source, the conduction band at the channel beginning decreases by qV_{CNT}, where q is the electron charge and V_{CNT} is the surface potential, whose expression is reported in our References [13-16].
With the hypothesis that each sub-band decreases by the same quantity along the whole channel length, the total drain current can be expressed as [3]:

$$I_{DS}=\frac{4qkT}{h}\sum_{p}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \quad (1)$$

where k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while ξ_{Sp} and ξ_{Dp}, depending on temperature through the sub-bands energy gap, and V_{CNT}, have the expressions reported in [3].
In order to simulate correctly the CNTFET behaviour, we needed to estimate parasitic capacitances and inductances as well as the drain and source contact resistances.
We have achieved this goal using an empirical method [2-3], suitable for simulations in CAD environment. This method requires the extraction of the previous parasitic elements comparing the device characteristics with the measured ones. In this way all elements of the equivalent circuit can be determined [2-3],
Fig. 1 shows our model, in which we have reported the values of circuital elements, used in the following simulations.

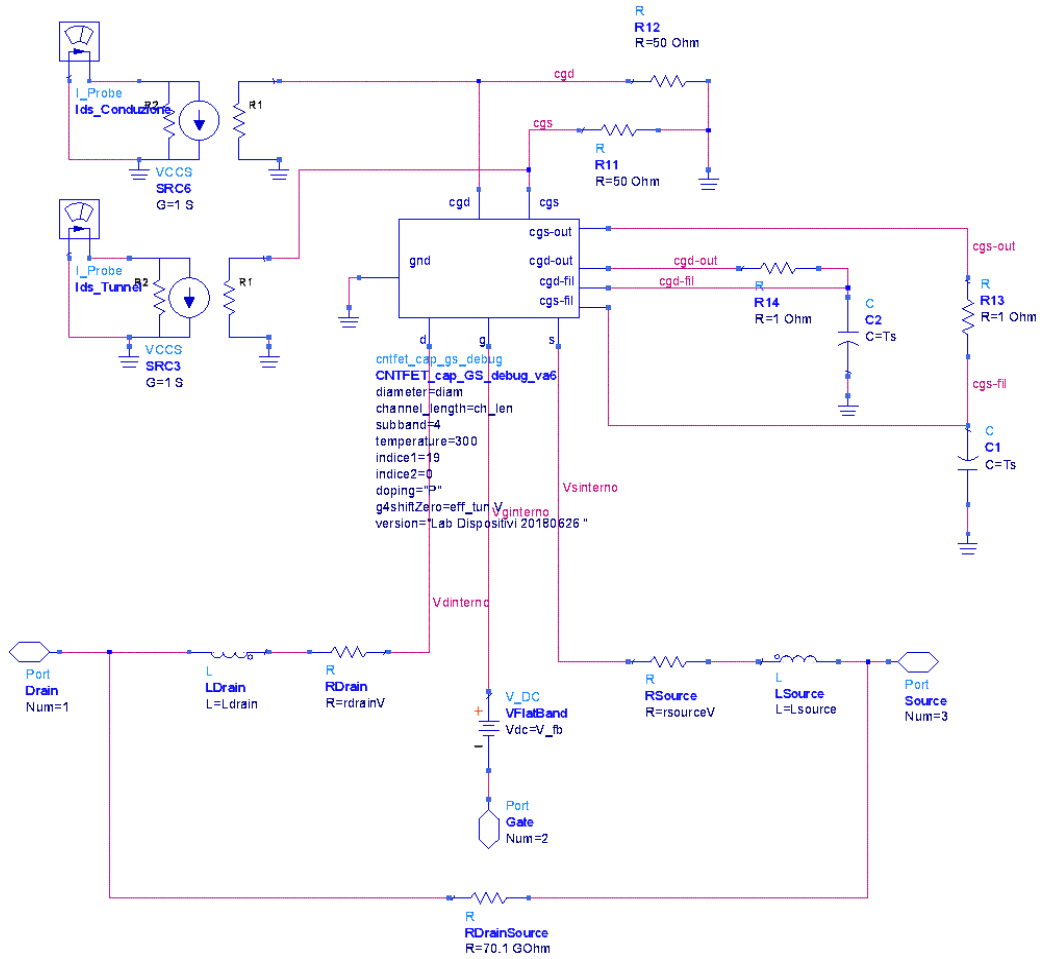


Figure 1. Our CNTFET model.

For the MOSFET model we use the **BSIM4 model** of ADS library.
BSIM (Berkeley Short-channel IGFET Model) [20] refers to a family of MOSFETs for integrated circuit design. In this work BSIM4 has been used for the 32 nm technology nodes.
Moreover the MOSFET parameters, obtained using an evolution of previous Berkeley Predictive Technology Model (BPTM), are improved by us through parametric simulations to obtain performance of the MOSFET model comparable to the CNTFET one.

III. DESIGN OF CURRENT MIRRORS

Current mirrors are circuits with two terminals whose currents are independent of the voltage applied at any time. Their use in integrated circuits, therefore, is extremely effective in simulating the behaviour of an ideal current generator.
In this section we only examine the design of a self-biased cascode mirror, emphasizing that the proposed procedure can be applied to any current mirror.

3a) Self-biased cascode mirror

We present this configuration because is the most complete and efficient in terms of the features considered respect to a simple current mirror or a cascade current mirror.
A resistor is introduced that exclude the possibility of using this type of current mirror in integrated circuits, because of the excessive use of space by the resistor.
The circuital configuration with CNTFET is shown in Fig. 2, and it is the same with 32 nm MOSFET.

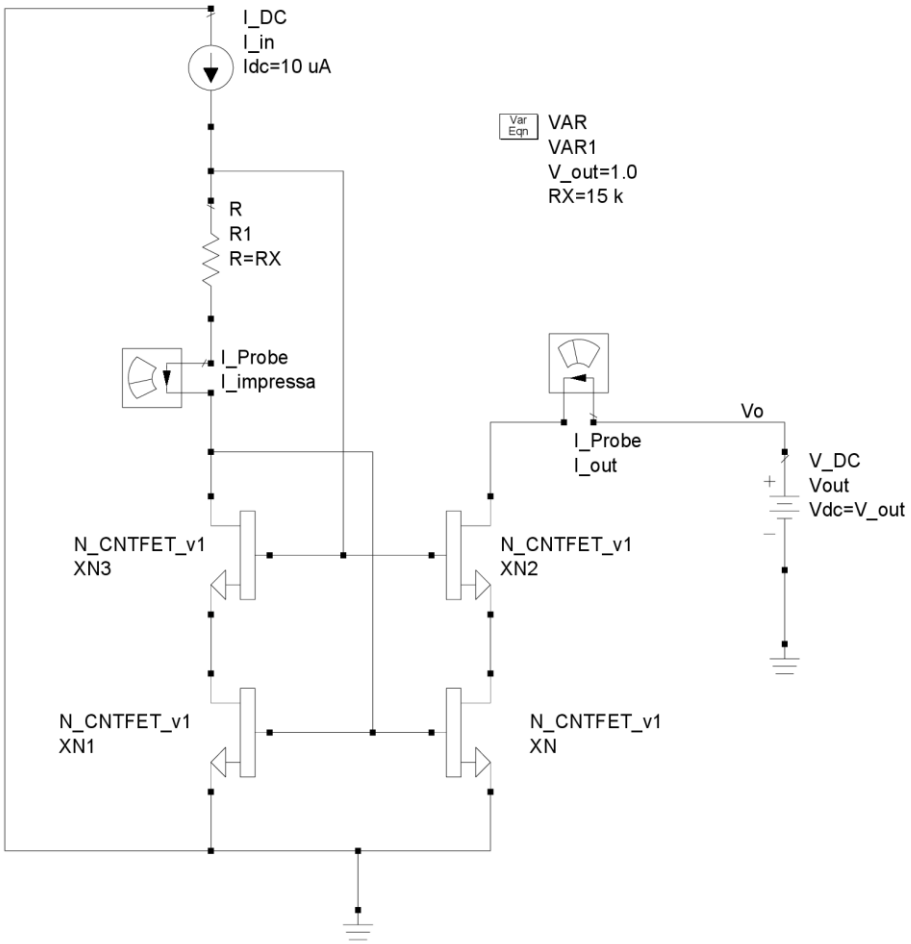
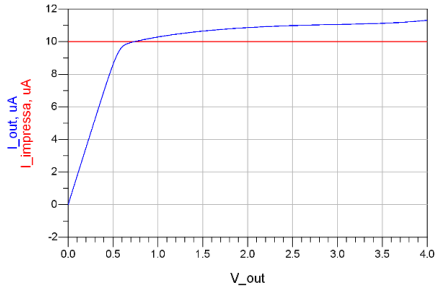


Figure 2. Self-Biased cascode mirror configuration with CNTFET.

The simulation results are shown in Fig. 3, for CNTFET, and in Fig. 4, for MOSFET.



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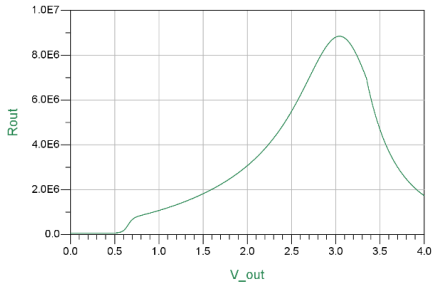

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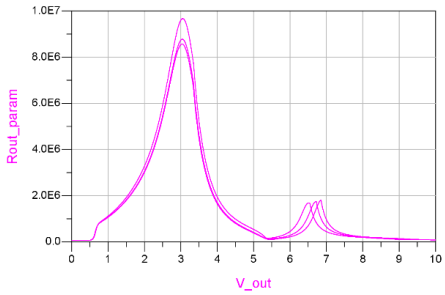
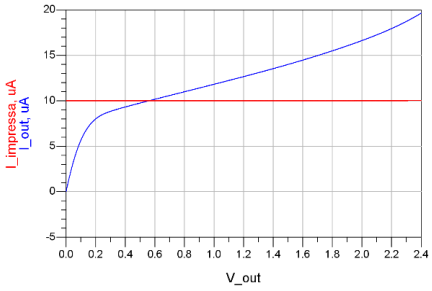
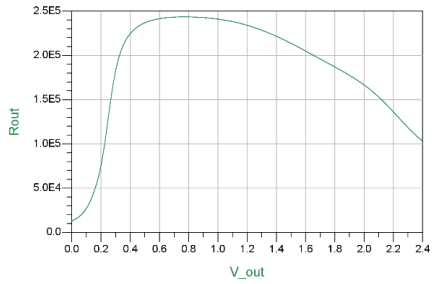


(c)

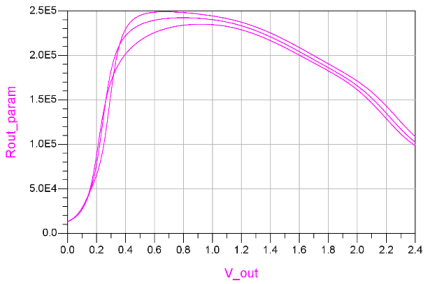
Figure 3. Simulation results for the self-biased cascode mirror configuration with CNTFET: (a) output current vs input current; (b) output resistance; (c) parametric sweep for optimal resistance.



(a)



(b)



(c)

Figure 4. Simulation results for the Self-Biased cascode mirror configuration with 32nm MOSFET: (a) output current vs input current; (b) output resistance; (c) parametric sweep for optimal resistance.

The numerical results are reported in Table I.

TABLE I. Simulation results for the self-biased cascade mirror.

	V_D	$I_{IMPRESSA}$	I_{OUT}	R_{OUT}	$R_{OUT,MAX}$	A_I
MOSFET 32nm	1 V	10 µA	11.82 µA	240.9 kΩ	243.5 kΩ ($V_D = 0.77\ V$)	0.84
CNTFET	1 V	10 µA	10.28 µA	1.07 MΩ	8.84 MΩ ($V_D = 3.04\ V$)	0.97

Data shows the overall improvement of the performance of the current mirror based on CNTFET. In fact it presents much higher output resistance than MOSFET without being disadvantaged in terms of current gain.

IV. CONCLUSIONS AND FUTURE DEVELOPMENTS

In this paper we shown, through a comparative study of current mirror based on CNTFET and 32-nm MOSFET, how it is possible to improve the performance of considered circuits.
In particular, in the design of a self-biased cascode mirror, we have at first emphasized that the proposed procedure can be applied to any current mirror. We chose this configuration because is the most complete and efficient in terms of the features considered respect to a simple current mirror or a cascode current mirror.
The obtained results have shown the overall improvement of the performance of the current mirror based on CNTFET with a higher output resistance without being disadvantaged in terms of current gain.
Moreover, the obtained results allowed to show the differences between CNTFET and MOS technology and the advantages of the first for analogue VLSI circuits.
In order to make further comparisons, we are considering other circuits, both analog and digital, using also other CNTFET models [21-22].
Currently we are working to study the effect of temperature [23-26].and of noise [27] in the CNTFET-based design of A/D circuits.

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