ANALYSIS AND SIMULATION OF MAIN SECOND ORDER EFFECTS IN CNTFETS

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ABSTRACT

In this paper we present at first an exhaustive description of the basic types of CNTFETs, with particular reference to the principle of operation. Then we analyze the main second order effects, discussing the simulation results in order to design CNTFETs having optimal technological characteristics.

KEYWORDS

Nanoelectronic Device, Nanotechnology, Carbon Nanotube Field Effect Transistors, Modeling, Second Order Effects, CAD Simulation.

I. INTRODUCTION

Carbon Nanotube Field Effect Transistors (CNTFETs) are novel devices that are expected to sustain the transistor scalability while increasing its performance. One of the major differences between CNTFETs and MOSFETs is that the channel of the devices is formed by Carbon NanoTubes (CNTs) instead of silicon, which enables a higher drive current density, due to the larger current carrier mobility in CNTs compared to bulk silicon [1]. In particular, with CNTs we obtain good operation even at very high frequencies [2-8].
A number of different geometries and solutions for CNTFETs, as well as their DC and low frequency behaviour [9-11], have been evaluated and reported in many papers.
In this paper we present an exhaustive description of the basic types of CNTFETs, with particular reference to the analysis and simulation of the main second order effects.
The presentation of the paper is organized as follows. In Section 2 we briefly examine the basic types of CNTFETs, analyzing, for each one, the principle of operation. In Section 3 we present a review of main second effects in CNTFETs, together with the discussion of relative simulation results. The conclusions are described in Section 4.

II. CLASSIFICATION OF CNTFETS

Carbon NanoTube Field Effect Transistors are a new kind of molecular device. They are field effect transistors using a carbon nanotube as channel, and are regarded as an important contending device to replace conventional silicon transistors [1].
There are basically three types of CNTFETs [1]:

1. Schottky Barrier (SB) CNTFET
2. Partially-Gated (PG) CNTFET
3. MOS-like CNTFET (also known as C-CNTFET).

Early SB-CNTFETs have been typically p-type devices: the current carriers are holes and the devices are considered ON for negative gate bias. N-type CNTFETs can be obtained by direct doping of the tube with an electropositive element or by a simple annealing process of p-type CNTFETs.
To understand the operation of a SB-CNTFET, it is necessary to examine the energy band diagram for the structure. At the intersection between the metal contacts and the semiconducting carbon nanotube, Schottky barriers are created [1].
The current in CNTFETs is from the tunneling of carriers through the Schottky barriers. The type of metal for the contacts is chosen so that its work function forces the metal Fermi Level to lie between the valance and conduction band of the CNT [1].
For short channels, the CNT channel can become ballistic and therefore the metal contact resistance and the Schottky barriers at the source and drain ends limit the current drive through the nanotube. Thus a low contact resistance, such as that of Titanium, is desirable. Presently the control of the metal contacts to carbon nanotubes is not consistent and the tunneling current levels between transistors can vary greatly.
When a negative voltage is applied between the drain and source, the band structure of the CNT is modulated to account for the drain to source voltage (V_{ds}).
When a small negative gate to source voltage is applied, CNTFET is in the subthreshold condition.
With a negative gate voltage applied, the Schottky barrier width at the source is modulated, allowing for holes or electrons to tunnel through the valence band and pass to the drain. The thickness of the source Schottky barrier at the metal Fermi level decreases exponentially with an increasing gate to source voltage. Thus the tunnel current through the Schottky barrier increases exponentially, inversely to the barrier thickness.
Moreover I_d-V_{gs} characteristic does not differ greatly changing V_{ds} because the drain voltage does not significantly control the source Schottky barrier.
The transistor threshold voltage, where the device acts similarly to an 'on' MOSFET, is reached when the metal source Fermi level is approximately even with the valence or conduction band of the CNT, in a p-channel or n-channel respectively. If the gate voltage continues to increase above this threshold, the Schottky barrier thickness at the source will remain constant and the current will not continue to increase exponentially. Above the threshold voltage, the current will only increase linearly with V_{ds}.
Above the CNTFET threshold voltage, the I-V characteristics are very similar to a MOSFET I-V characteristics: the current increases linearly with V_{ds}; and, when the barrier at the drain is completely eliminated, the FET current saturates.
The I_d-V_{ds} characteristics for a saturated SB-CNTFETs have a very little slope, unlike short channel MOSFETs.
PG-CNTFETs are uniformly doped (or uniformly intrinsic) with ohmic contacts at their ends. PG-CNTFETs can be of n-type or p-type when respectively n-doped or p-doped.
These devices work in a depletion mode (uniformly n/p doped): the gate locally depletes the carriers in the nanotube and turns OFF the p-type device with an efficiently positive threshold voltage (efficiently negative for n-type) that approaches the theoretical limit for room-temperature operation. The ON current of such devices is limited by a "source exhaustion" phenomenon [1].
When the CNT is intrinsic, CNTFETs operate in enhancement mode and exhibit n- or p-type unipolar behaviour.
In case of **MOS-like CNTFETs** the source and drain are basically semiconductors p-type or n-type which are heavily doped [2-3]. These devices, also denoted as **conventional CNTFETs** or **C-CNTFETs**, show the best performances in terms of "on-off" ratio currents and subthreshold swing. Fig. 1 shows a 3D representation of a C-CNTFET, whose conduction behaviour is similar to a common MOSFET.

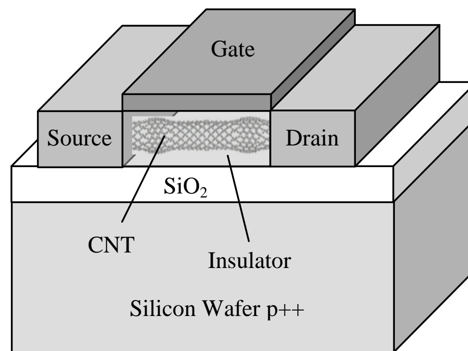

Figure 1. 3D representation of a C-CNTFET.

When a positive voltage is applied between drain and source (V_{DS}> 0 V), the hypothesis of ballistic transport allows to assert that the current is constant along the CNT and therefore can be calculated at the beginning of the channel, near the source, at the maximum of conduction band, where electrons from the source take up energy levels related to states with positive wave number, while the electrons from the drain take up energy levels related to states with negative wave number.
C-CNTFETs, with reference to SB-CNTFETs, show the following advantages:

1. unipolar characteristics and, therefore, faster;
2. reduction of the leakage current in the *off* state, due to absence of the Schottky barrier;
3. greater scalability;
4. a switch-*on* current of the source-channel junction significantly higher.

However, the control of the doping with ion implantation techniques are very difficult because the ions can replace the carbon atoms and destroy the desired properties of nanotubes.
In Figs. 2 and 3 we have reported the results of our simulations, which are not functional to the study of second order effects in CNTFET but are interesting in order to observe the geometrical form of two CNTs having chirality vectors (m=6, n=2) and (m=17, n=3) respectively.

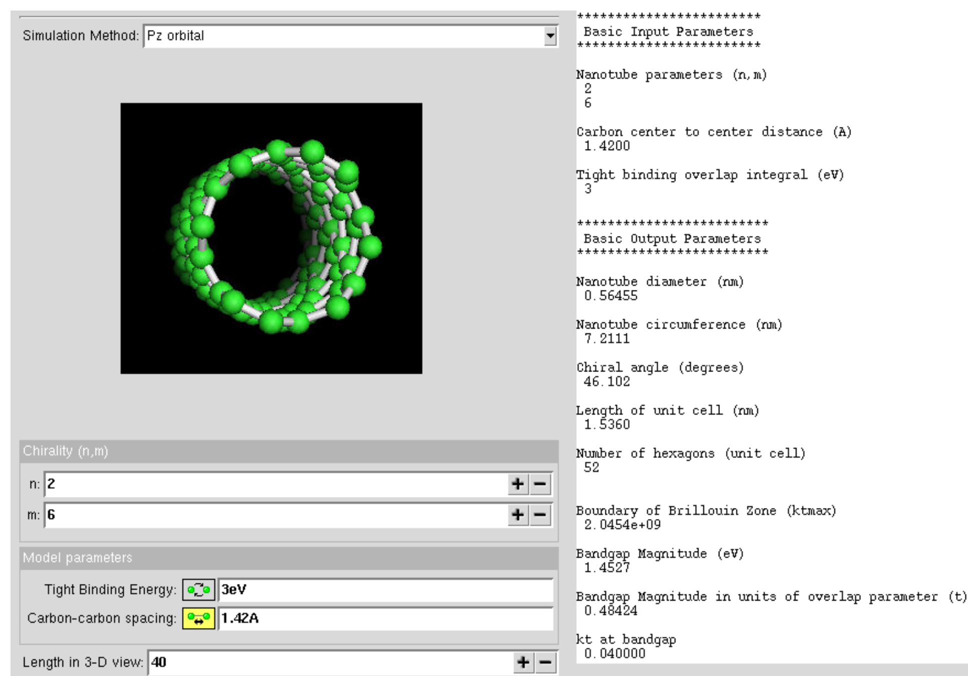

Figure 2. CNT with chirality vector m=6 n=2.

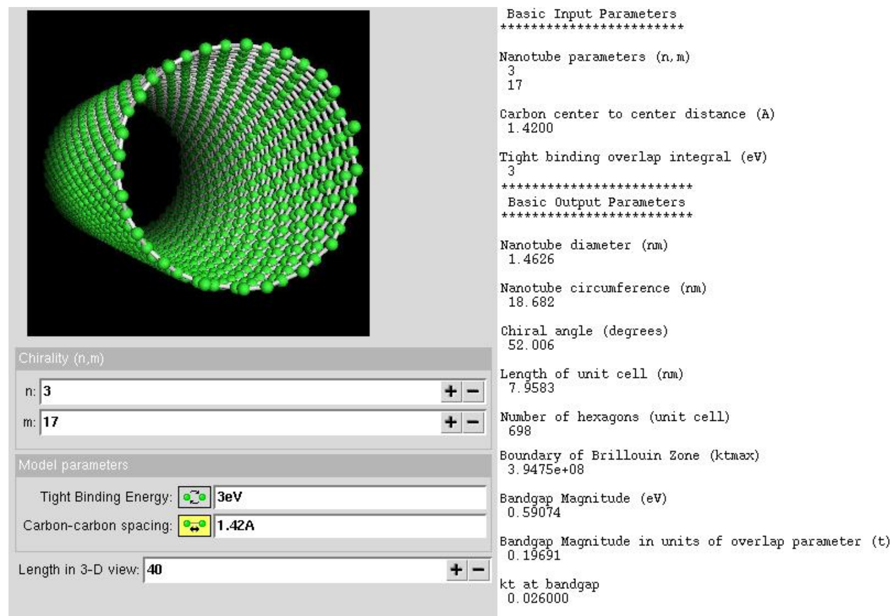

Figure 3. CNT with chirality vector m=17 n=17.

III. MAIN SECOND ORDER EFFECTS IN CNTFETS

IIIa) Channel Length modulation

There are many researches that assume a uniform voltage, resistance, and Fermi energy along the length of the CNT. For ballistic transport, this hypothesis are not valid because gate, source, and drain capacitances switch spatially, and this requires a spatial solution of Poisson's equation to have the voltage and carrier number density distribution. In devices with quasi-ballistic and diffusive transport, this approximation affect modeling of pinch-off and channel length modulation, effects that have many influences on electrical transport in FET devices.

The gate efficiency of the segment with the most efficient gate capacitance is defined as:

$$\alpha = \frac{C_G}{C_G + 4\frac{C_{sd}}{x_d}} \tag{1}$$

where C_G is the capacitance from the section of the CNT to the gate, C_{sd} is a characteristic capacitance per unit-length for the source-channel and x_d is the CNT channel length.

Fig. 4 shows current saturation curves for CNTFET (device p-type, with high on-current at negative gate voltages, an ON–OFF ratio of approximately 10^6 and a subthreshold slope of approximately 100 mV/decade) with different values of gate efficiency α.

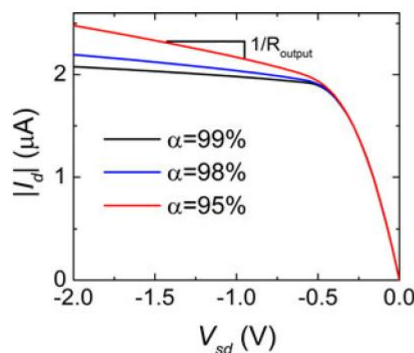

Figure 4. Drain current versus source-drain voltage for a CNTFET [12].

In particular Fig. 4 shows channel length modulation in a CNTFET: drain current versus source-drain voltage at gate efficiencies α of 99%, 98%, and 95%, showing decreased output resistance for lower gate coupling efficiencies caused by channel length modulation.
For high gate efficiency (low channel-source and channel-drain capacitances), the output resistance is high with a finite output resistance in the current saturation region due to channel length modulation, caused by channel-drain capacitive coupling. For low gate efficiencies, however, the output resistance is low [12].

IIIb) Hot carriers

Hot carrier injection (HCI) is a phenomenon in solid-state electronic devices where an electron or a hole gains sufficient kinetic energy to overcome a potential barrier necessary to break an interface state. The term "hot" refers to the effective temperature used to model carrier density, not to the overall temperature of the device. Since the charge carriers can become trapped in the gate dielectric of a FET transistor, the switching characteristics of the transistor can be permanently changed. Hot-carrier injection is one of the mechanisms that adversely affects the reliability of semiconductors of solid-state devices.
The high stability of metallic CNTs is maintained as long as the electron (hole) energy is not high enough to excite optical phonons. When these vibrational modes become excited the resulting energy dissipation eventually leads to the breakdown of the CNT structure. Since in defect-free CNTs transport is ballistic, high-energy carriers can be formed by hot carrier injection at the contacts. Thus, the stability of a CNT depends on the nature of the contacts. Another factor that influences the stability of a CNT is the gaseous environment it is in. Experiments have shown that the threshold voltage that is needed to induce breakdown in a CNT is drastically lower in air than it is in vacuum.

IIIc) Subthreshold currents

The portable electronics industry, expanded intensely in the recent years, requires voltage supply scaling, so that the supply voltage is lower than the threshold voltage of a transistor (0.4–0.6 V). For these low power applications, such as hearing aids, trade performance for power savings, the transistor must operate in subthreshold regime.
An important metric in subthreshold design is the ratio of on-to off-current (*Ion/Ioff*). This ratio characterizes the difference in current between a closed and open switch.
The on-current in MOSFETs decreases exponentially as the supply voltage is lowered. The same happens in carbon nanotube transistors. However, compared to MOSFETs, the off-current in CNTFETs continues to decrease as the voltage across the FET from drain to source decreases [13].
Carbon nanotubes have a varying *Ion/Ioff* ratio, depending on the nanotube structure and properties. These very high current values in CNTs are due to their ballistic transport and their limited electron and hole scattering. Therefore, CNTs have the ability to increase performance while adhering to lower power requirements in subthreshold circuits.
The total current in a CNTFET, as described previously, depends on the tunnelling current both of the holes and of the electrons through the source and drain Schottky barriers: the current in a SB-CNTFET exponentially increases, reducing the thickness of the Schottky barrier at source, with also an increase of the subthreshold current.
In comparison with MOSFETs, in CNTFETs we have not the minimum current for Vgs = 0 V, but to Vgs = Vds/2. This is true for all SB-CNTFETs having the same metal used for the gate, drain and source [13]. In [13].we have implemented a Matlab code, characterized by a minimum current at Vds/2, threshold voltage and exponential subthreshold current.
The obtained Id-Vgs characteristics, for a n-channel and a p-channel CNTFETs, are shown in Figs. 5 and 6 respectively.

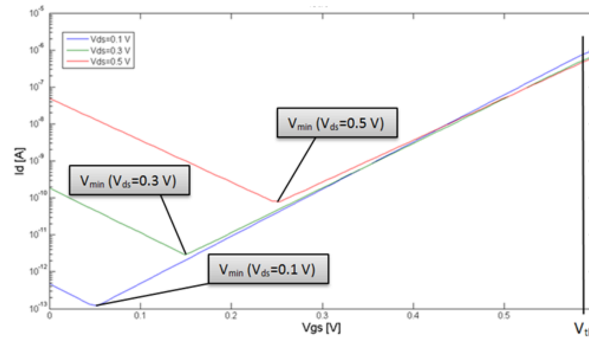

Figure 5. Simulated Id-Vgs characteristics of a n-channel SB-CNTFET.

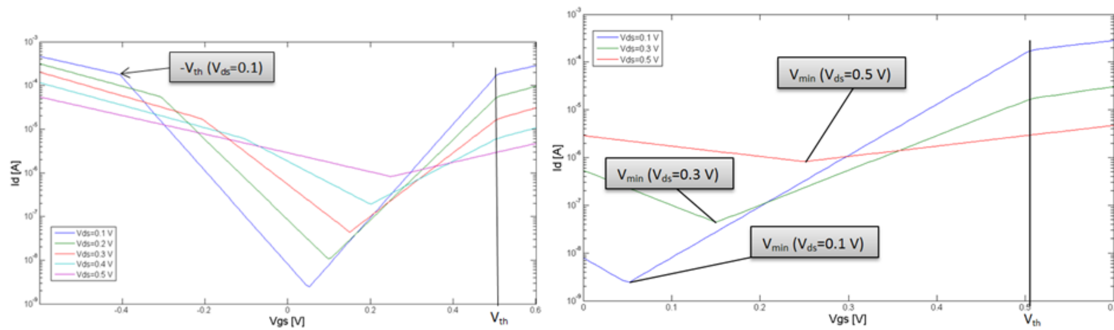

Figure 6. Simulated Id-Vgs characteristics of a p-channel SB-CNTFET.

From these figures we can evaluate the numerical values of V_{min}, I_{Dmin} and V_{th}. In fact the CNTFET subthreshold regime is verified between the two threshold voltage (V_{th}) points. These points have the same distance from the minimum voltage.

The distance from the minimum to the threshold is ΔV_{SUB} (Vds) = V_{th} - V_{min}.

IIId) Effect of Oxide Thickness on Threshold voltage

The oxide thickness is a parameter of CNTFET devices that influences the quantum capacitance and therefore the threshold voltage [1]. In order to determine the quantum capacitance, we omitt all the mathematical passages, because they are exhaustively described in [2-3]. In this paper we report our simulations carried out using nanoHUB tool, named "FETToy" [14]. In particular Fig. 7 shows the quantum capacitance vs gate voltage for four CNTFETs that have same threshold voltage, equal to 0.32 V, at room temperature (300 K).

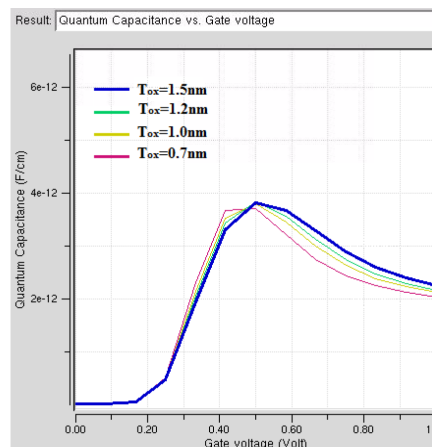

Figure 7. C_Q vs gate voltage for four CNTFETs

CNTFETs used for simulation have oxide thickness of *1.5 nm*, *1.2 nm*, *1.0 nm* and *0.7 nm* respectively. This simulation shows that increasing oxide thickness also the quantum capacitance increases. In particular the four CNTFETs show a different peak valure: device with widest oxide thickness presents an higher peak value of quantum capacitance at higher gate voltage. For all devices the quantum capacitance tends to a saturation value, equal to 2. 10^{-12} F/cm. This makes CNTFET excellent semiconductor devices in deep nanometer regime.

IIIe) Effect of temperature on threshold voltage

Simulation analysis of the CNTFET characteristic at different temperatures is shown in Fig. 8**.**

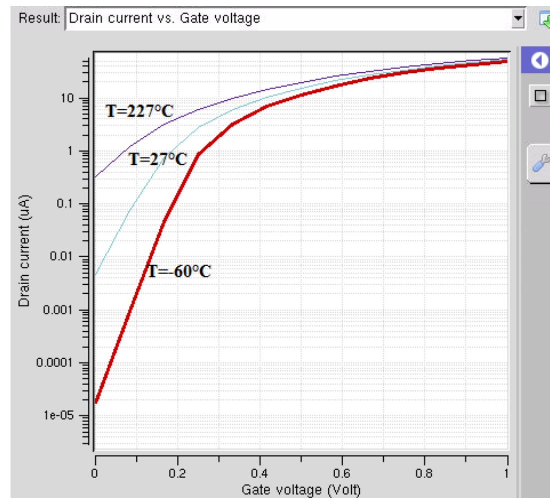

Figure 8. Drain current vs Gate voltage for three CNTFETs

It has analyzed the drain current versus the gate voltage at different drain voltages of the CNTFET device and observed that the threshold voltage is almost the same in all temperatures considered and there is small variation in threshold voltage while increasing and decreasing the temperature, which is negligibly small.

Devices used for simulation have different value of V_{TH} and different temperature, i.e.:

$V_{TH} = 0.164\ V\ (T= 227°C)$, $V_{TH} = 0.210\ V\ (T = 27°C)$ and $V_{TH} = 0.256\ V\ (T =- 60°C)$.

As it can see from Fig. 8, the switching speed is more for higher value of temperature as the temperature increases the device approaches to saturation faster. The most nanoelectronic applications look for high speed CNTs that are well known to have very high mobilities. The low scattering probability in CNTs is responsible for superior mobilities. The ultimate saturation velocity does not sensitively depend on the low- field mobility. It is, therefore, of interest for us to find the ultimate velocity that may exist in an SWCNT. This velocity will necessarily depend on the band structure, the temperature, and the degeneracy level. The carrier drift is the velocity with which a carrier (electron or hole) can propagate through the length of the device encountering collisions on the way and starting its journey fresh on facing a collision. The higher mobility may bring an electron closer to saturation as a high electric field is encountered, but it does not need to elevate the saturation velocity. Fig. 9 shows the curve plotted between average velocity of charge carriers and the gate voltage with reference to three different temperatures.

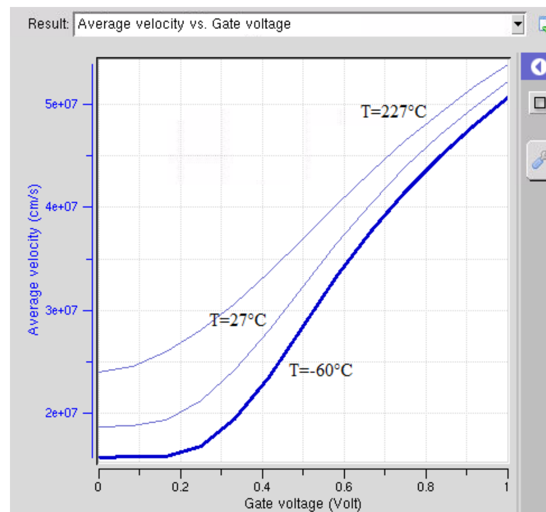

Figure 9. Average velocity vs Gate voltage for three CNTFETs.

CNTFETs have the same values of V_{TH} and temperatures used in the previous simulations.

From Fig. 9, it is clear that as the gate voltage increases at fixed drain voltage, the average velocity of charge carrier at the start, remains constant; but after certain gate voltage the velocity of charge carriers increases linearly. Moreover the plot shows that at higher temperatures correspond to higher average velocity carrier.

In Fig.10 we have reported the output characteristics (i.e. drain current vs drain voltage) for different threshold voltage of CNTFET, that operate at different temperatures.

From Fig. 10, it is clear that the drain current is more for higher values of temperature and lower values of threshold voltage; device that works with V_{TH} = 0.164V T= 227 °C reaches the highest value of voltage saturation.

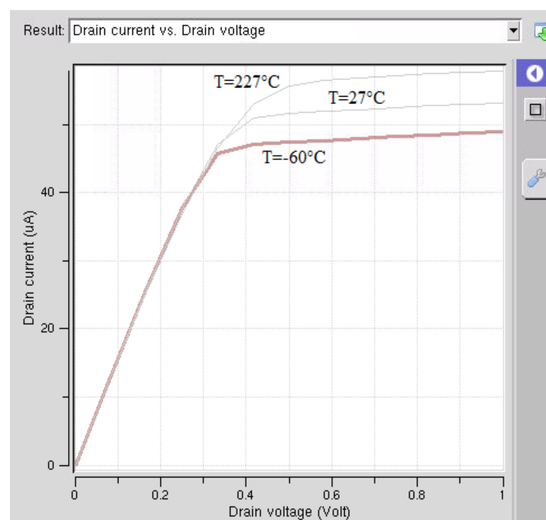

Figure 10. Output characteristics for different threshold voltage of CNTFETs, that operate at different temperatures.

IIIf) Effect of High-K dielectric on threshold voltage

Silicon oxide SiO_2 has been used as gate dielectric, since the inception of MOSFET in 1960, because of its electrical stability interface between Si and SiO_2 and thermal stability. High speed and shrinking of chip area in integrated circuits are achieved by scaling down of physical thickness of the SiO_2 and gate length. However, gate leakage due to direct tunneling of electrons through the SiO_2 will be too high, and circuit power dissipation will increase to an unacceptable value, when the gate dielectric is so thin, especially when it is less than *1.5 nm*. While realizing MOSFET with *1.5 nm* oxide thickness,

the major obstacle is to overcome the high level of direct tunneling current through the gate and the possible solution of which is to incorporate the use of a High-K_{OX} gate dielectric. However high value of dielectric constant is not good for the threshold voltage V_{TH} of the device, which decreases.
In Fig. 11 we have reported drain current vs gate voltage for different gate dielectric of CNTFETs.

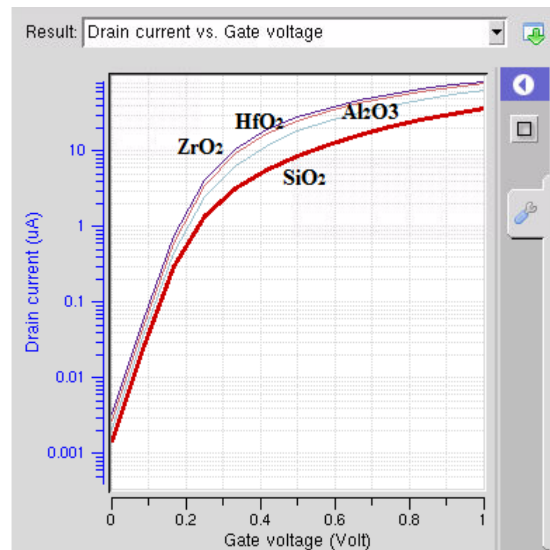

Figure 11. I_D-V_{GS} characteristics for CNTFETs having different K_{ox}.

Devices used for simulation have K_{OX} and V_{TH}:
SiO_2 with $K_{ox} = 3.9$ $V_{TH} = 0.240$ V;
Al_2O_3 with $K_{ox} = 9.0$ $V_{TH} = 0.231$ V;
HfO_2 with $K_{ox}=15.6$ $V_{TH} = 0.224$ V;
ZrO_2 with $K_{ox}=19.0$ $V_{TH} = 0.218$ V.
Moreover, from Fig. 11, the switching speed is more for higher value of K_{OX}, i.e., the device with gate dielectric implemented with ZrO_2. The devolpment of the curves for device with gate dielectric implemented with ZrO_2 and HfO_2 are very close because their K_{OX} and V_{TH} are very similar (HfO_2: $K_{ox}=15.6$ $V_{TH}=0.224V$ vs ZrO_2: $K_{ox}=19.0$ $V_{TH}=0.218V$). As the K_{OX} increases, the device reaches to saturation faster.
For the same CNTFETs we have simulated the average velocity and quantum capacitance vs gate voltage.
The obtained results are shown in Figs. 12 and 13 respectively, in which devices have values of K_{OX} and of V_{TH} equal to those used in the simulation of Fig. 11.
From Fig. 12, it is clear that as the gate voltage increases at fixed drain voltage, the average velocity of charge carrier at the start, remains constant; but after certain gate voltage the velocity of charge carriers increases linearly.
Moreover at higher value K_{OX} and lower value of V_{TH} (device with gate dielectric implemented with ZrO_2) correspond to higher average velocity carrier.
Device with gate dielectric implemented with SiO_2 shows the lowest development of average velocity of charge carriers between the devices analyzed in this simulation.

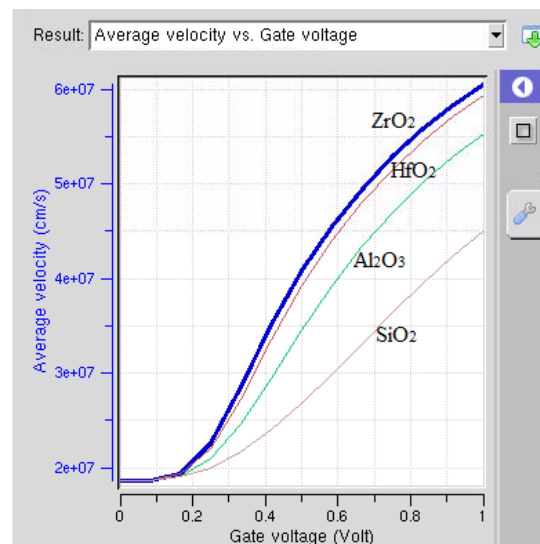

Figure 12. Average velocity vs Gate voltage for the four considered CNTFETs

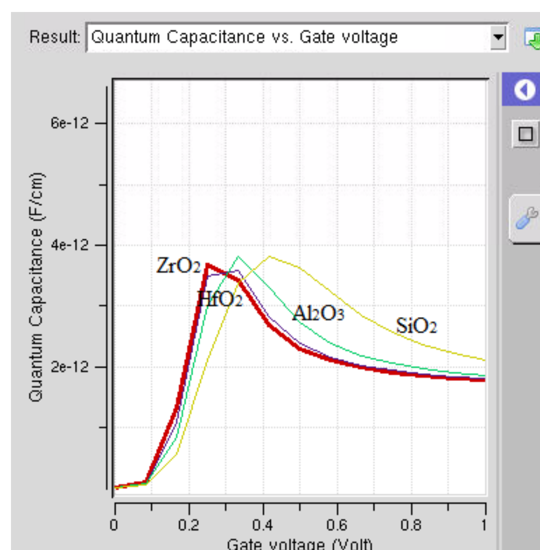

Figure 13. Quantum capacitance vs gate voltage for the four considered CNTFETs.

Fig. 13 underlines that the four CNTFETs, used for simulation, show a similar peak value.
Device with ZrO_2 has highest value of K_{OX} ($K_{ox}=19.0$) which corresponds to lower threshold voltage ($V_{TH}=0.218V$) presents its peak value for lower value of gate voltage (≈ 0.25 V).
Device with SiO_2 has lowest value of K_{OX} ($K_{ox}=3.9$) which corresponds to highest threshold voltage ($V_{TH}=0.240V$) presents its peak value for highest value of gate voltage (≈ 0.40 V).
All four devices, quantum capacitance tends towards to a saturation value, equal to 2. 10^{-12} F/cm.

IV. CONCLUSIONS AND FUTURE DEVELOPMENTS

In this paper we have presented an exhaustive description of the basic types of CNTFETs, analyzing, for each one, the principle of operation. Then we have described and simulated the main second order effects. In particular we have considered the channel length modulation, the hot carrier injection, the subthreshold currents, the effect of oxide thickness, of temperature and of high-K dielectric on threshold voltage. We have discussed the obtained results in order to design CNTFETs having optimal technological characteristics.
Currently we are investigating about the effects of temperature in the design of CNTFET-based analogue and digital circuits.

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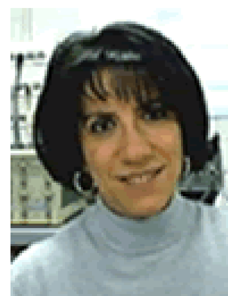

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Actually she works in the design, realization and testing of nanometrical electronic systems, quantum devices and FET on carbon nanotube.
Prof. Perri is the Head of the Electron Devices Laboratory of the Polytechnic University of Bari.
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Prof. Perri is the holder of two italian patents and the Editor of three international books.
She is also responsible for research projects, sponsored by the Italian Government.
Prof. Perri is an Associate Member of National University Consortium for Telecommunications (CNIT).