FUZZY LOGIC CONTROLLED CASCADED SEPIC - QRC FED DC DRIVE SYSTEM WITH IMPROVED DYNAMIC RESPONSE

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ABSTRACT

The objective of this work is to improve the dynamic response using FLC. This paper deals with design, modeling and simulation of closed loop cascaded SEPIC - QRC fed DC drive system. The closed loop SEPIC - QRC System is simulated with PI and FL controllers and their results are compared in terms of settling time and steady state error. The Fuzzy Logic Controlled cascaded SEPIC - QRC System is proposed in the present work to control the speed of the DC drive. The proposed system has advantage like high efficiency, low EMI and low switching losses.

KEYWORDS: *Single – Ended Primary – Inductor Convertor (SEPIC), Quasi resonant Convertor (QRC), Zero current switching (ZCS), Pulse width modulation (PWM), Fuzzy Logic Control (FLC), EMI-Electro Magnetic Interference, PI - Proportional Integrator and SEPICQRCFDD- SEPIC-QRC fed DC Drive.*

I. INTRODUCTION

The single-ended primary inductor converter acts as a buck–boost DC–DC converter, where it changes its output voltage according to its duty cycle. Among known converters, the SEPIC, conventional buck–boost, and Cuk converters have the ability to step up and step down the input voltage. Hence, this converter can transfer energy for all irradiation levels. Another desirable feature is continuous output current, which allows converter output parallel connection, or conversion to a voltage source with minimal capacitance. The buck or boost converters are not preferable, due to the lack of output voltage flexibility. The SEPIC is chosen because the output voltage can be higher or lower than the input voltage. Also the input and output voltages are DC isolated.
Block diagram of the existing system shown in Figure.1. Fixed DC is converted into variable DC using QRC. The output of QRC is applied to the DC motor.

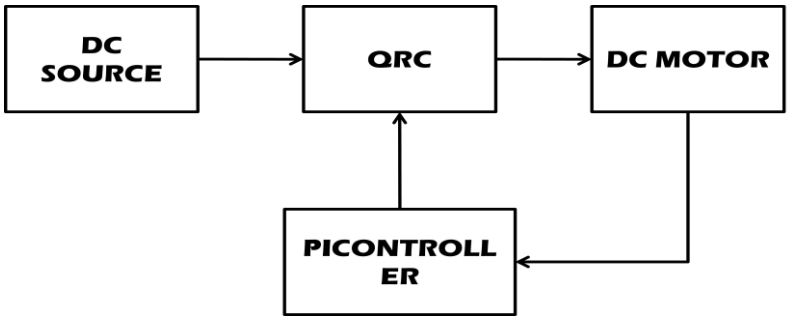

Figure 1. Black Diagram of the Existing System

The block diagram of SEPICQRCFDD is shown in Figure 2. The QRC is replaced by cascaded SEPIC- QRC based converter.

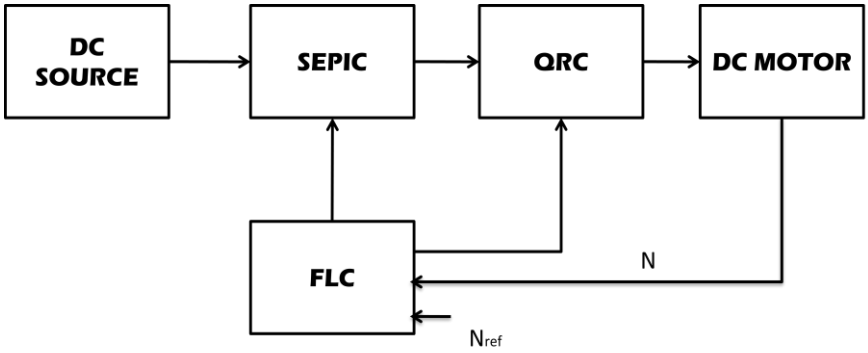

Figure 2. Black Diagram of the SEPICQRCFDD System

SEPICs are useful in applications in which a battery voltage can be above and below that of the regulator's intended output. Section 2 deals with literature survey. The analysis of SEPIC is presented in the section 3. The simulation results are given in section 4. The work is concluded in section 5 and the scope for future work is given in section 6

II. LITERATURE SURVEY

Bridgeless Single-ended Primary Inductance Converter with improved power quality for welding power supplies is given by Narula.S and Singh.B.(2014). Design considerations of a multiple-input isolated single ended primary inductor converter for distributed generation sources is described by Sheng-Yang Yu, Ruichen Zhaoand Kwasinski. A. (2011). Multi-loop controller for wide operating range single-ended primary inductor DC/DC converter said by Tsang. K.M.and Chan. W.L.(2011). Single Ended Primary Inductor Converter reliance of efficiency on switching frequency for use in MPPT application developed by Burmester. D, Rayudu. R and Exley.T.(2011).Maximum power point tracking of single-ended primary-inductor converter employing a novel optimisation technique for proportional-integral-derivative controller given by El Khateb. A,Rahim. N.A,Selvaraj. Jand Uddin. M.N(2013). Multiple input single ended primary inductor converter for distributed generation applications given by Ruichen Zhaoand Kwasinski. A. (2009). A Four-Switch Three-Phase SEPIC-Based Inverter ExplainedbyDiab.M.S, Elserougi. A, Massoud. A.M, Abdel-Khalik. A.S and Ahmed. S. (2015). Fuzzy Logic Controller for MPPT SEPIC converter and PV single-phase inverter described by Khateb. A, Rahim,N.A and Selvaraj. J.(2011). High frequency quasi resonant SEPIC converter for wide range of operation explained by Unnikrishnan.C.Kand Raj. C.R.(2014). Performance of a DC motor fed from series and parallel quasi-resonant converters" developed by S.Rama Reddy and C. Chellamuthu,(1997). A Simple Large signal nonlinear modeling approach for fast simulation of Zero current switching Quasi resonant converters described by .L.K. Wong, Frank H. Leung and Peter KS. Tam,(1997).

The above literature does not deal with SEPIC-QRC controlled DC drive. This work proposes cascaded SEPIC-QRC for the control of DC drive. The comparison of dynamic responses with PI and FLC is not reported in the literature.

III. ANALYSIS

The SEPIC is allowing the electrical voltage at its output to be greater than, less than, or equal to that at its input. The output of the SEPIC is controlled by the duty cycle of the control transistor. A SEPIC is essentially a boost converter followed by a buck-boost converter, therefore it is similar to a traditional buck-boost converter, but has advantages of having non-inverted output, using a series capacitor to couple energy from the input to the output, and being capable of true shutdown when the switch is turned off, its output drops to 0 V, following a fairly hefty transient dump of charge.

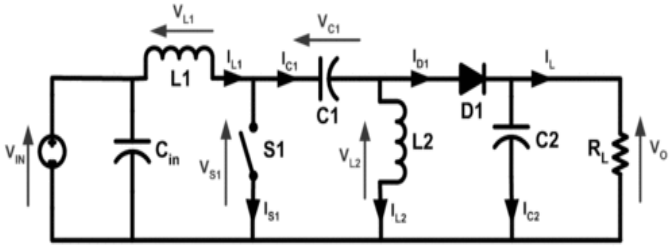

Figure 3. Schematic of SEPIC**.**

The schematic diagram for a basic SEPIC is shown in Figure 3. As with other switched mode power supplies , the SEPIC exchanges energy between the capacitors and inductors in order to convert from one voltage to another. The amount of energy exchanged is controlled by switch S_1, which is typically a transistor such as a MOSFET. MOSFETs offer much higher input impedance and lower voltage drop than bipolar junction transistors (BJTs), and do not require biasing resistors as MOSFET switching is controlled by differences in voltage rather than a current, as with BJTs.

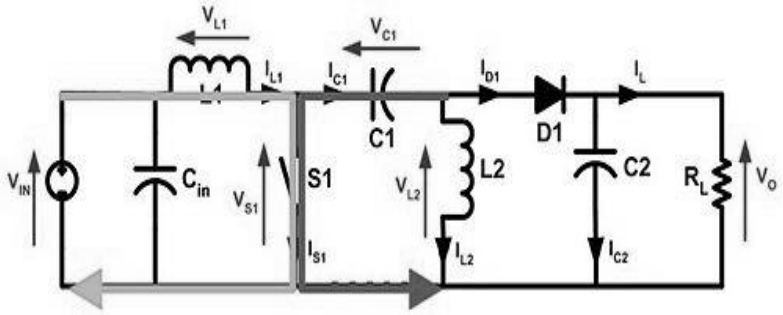

Figure 4. Circuit with S1 closed

A SEPIC is said to be in continuous-conduction mode if the current through the inductor L_1 never falls to zero. During a SEPIC's steady-state operation, the average voltage across capacitor C_1 (V_{C1}) is equal to the input voltage (V_{in}). Because capacitor C_1 blocks direct current, the average current through it (I_{C1}) is zero, making inductor L_2 the only source of DC load current. Therefore, the average current through inductor L_2 (I_{L2}) is the same as the average load current and hence independent of the input voltage. Looking at average voltages, the following can be written:

$$V_{IN} = V_{L1} + V_{C1} + V_{L2} \text{ ----- (1)}$$

Because the average voltage of V_{C1} is equal to V_{IN}, $V_{L1} = -V_{L2}$. For this reason, the two inductors can be wound on the same core. Since the voltages are the same in magnitude, their effects of the mutual inductance will be zero, assuming the polarity of the windings is correct. Also, since the voltages are the same in magnitude, the ripple currents from the two inductors will be equal in magnitude. The average currents can be summed as follows

$$I_{D1} = I_{L1} - I_{L2} \text{ -------- (2)}$$

When switch S_1 is turned on, current I_{L1} increases and the current I_{L2} goes more negative. The energy to increase the current I_{L1} comes from the input source. Since S_1 is a short when closed, and the instantaneous voltage V_{C1} is approximately V_{IN}, the voltage V_{L2} is approximately $-V_{IN}$. Therefore, the capacitor C_1 supplies the energy to increase the magnitude of the current I_{L2} and thus increase the energy stored in L_2. The easiest way to visualize this is to consider the bias voltages of the circuit in a DC state, and then close S_1.

When switch S_1 is turned off, the current I_{C1} becomes the same as the current I_{L1}, since inductors do not allow instantaneous changes in current. The current I_{L2} will continue in the negative direction, in fact it never reverse its direction. It can be seen from the diagram that a negative I_{L2} will add to the current I_{L1} to increase the current delivered to the load. Using Kirchhoff's Current Law, it can be shown that

$I_{D1} = I_{C1} - I_{L2}$. ------- (3)

It can then be concluded, that while S_1 is off, power is delivered to the load from both L_2 and L_1. C_1, however is being charged by L_1 during this off cycle, and will in turn recharge L_2 during the on cycle.

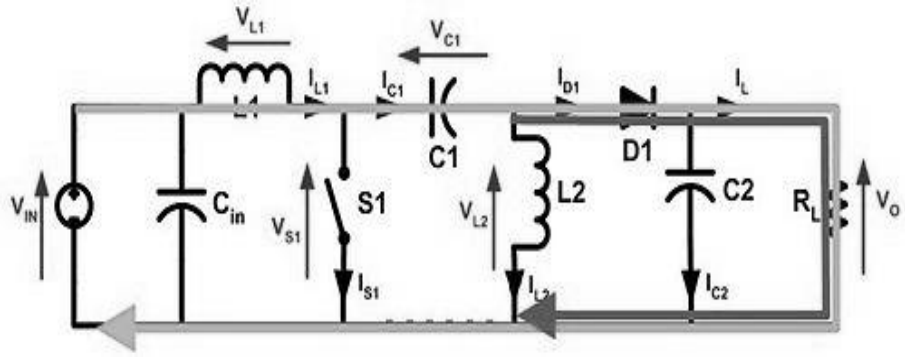

Figure 5. Circuit with S1 open

Because the voltage across capacitor C_1 may reverse its direction every cycle, a non-polarized capacitor should be used. However, a polarized tantalum or electrolytic capacitor may be used in some cases, because the potential across capacitor C_1 will not change unless the switch is closed long enough for a half cycle of resonance with inductor L_2, and by this time the current in inductor L_1 could be quite large.

The capacitor C_{IN} is required to reduce the effects of the parasitic inductance and internal resistance of the power supply. The boost/buck capabilities of the SEPIC are possible because of capacitor C_1 and inductor L_2. Inductor L_1 and switch S_1 create a standard boost converter, which generates a voltage (V_{S1}) that is higher than V_{IN}, whose magnitude is determined by the duty cycle of the switch S_1. Since the average voltage across C_1 is V_{IN}, the output voltage

$V_O = V_{S1} - V_{IN}$. -------- (4)

If V_{S1} is less than double V_{IN}, then the output voltage will be less than the input voltage. If V_{S1} is greater than double V_{IN}, then the output voltage will be greater than the input voltage.

The evolution of switched-power supplies can be seen by coupling the two inductors in a SEPIC converter together, which begins to resemble a Fly back converter, the most basic of the transformer-isolated SMPS topologies.

IV. SIMULATION RESULTS

The values of parameters used for simulation are given in Table1

Table1. Parameters of Proposed System

Name of the parameter	Value
V_{in}	75V
L_1	8Mh
L_2	30mH
C_{in}	2000µF
C_1	0.30µF
C_{bo}	3000µF
MOSFET (IRF840)	500V/8A
DIODE	230V/1A
V_0	150V

The open loop controlled SEPIC-QRC fed DC drive system is shown in Figure 6. The step change is input voltage is shown in Figure 7. The input voltage increases from 70V to 80V at t=2Sec.The speed response is shown in Figure 8.The speed increases from 1700 rpm to 2000 rpm. The torque developed is shown in Figure 9.The torque settles at 14 N-m.

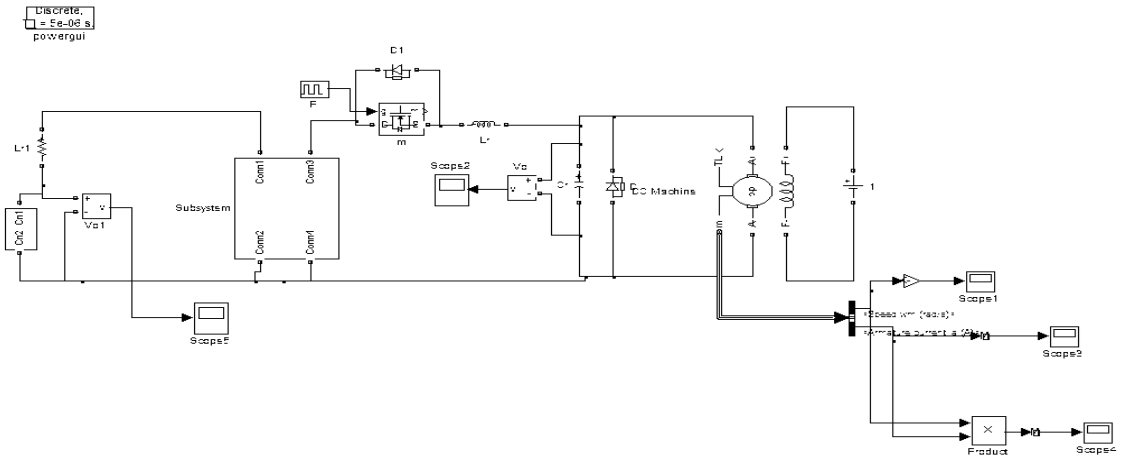

Figure 6. SEPIC-QRC Based Open LoopSsystem

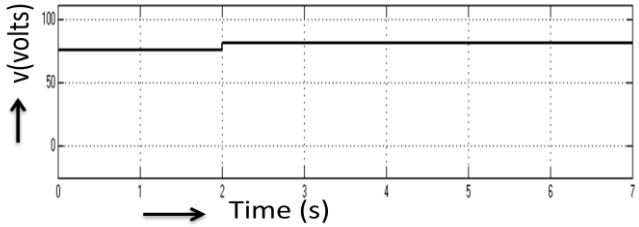

Figure 7. Input Voltage

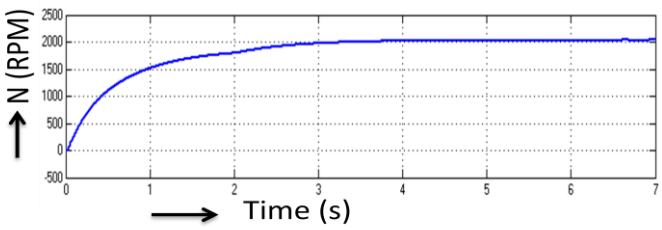

Figure 8. Motor Speed

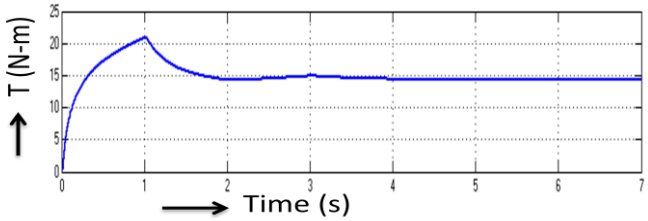

Figure 9. Motor Torque

Closed loop speed controlled system with PI controller is shown in Figure 10.The speed is sensed and it is compared with a reference speed of 1500 rpm. The error is applied to a PI controller and the output of the PI controller is applied to comparator .The comparator updates the pulse width of driving pulse given to the SEPIC converter. The step change in input voltage is shown in Figure 11.The speed response is shown in Figure 12.The speed oscillates and settles at the set reference value. The torque response is shown in Figure 13.

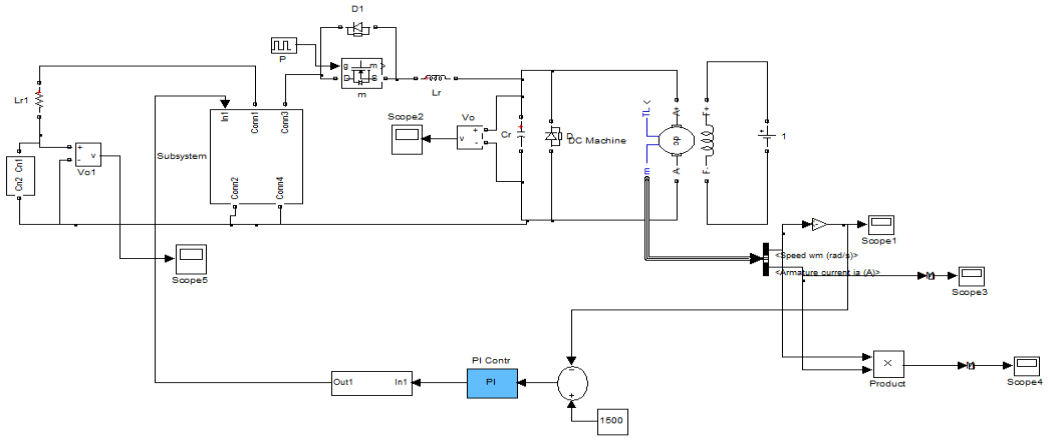

Figure 10. Closed Loop System with PI Controller

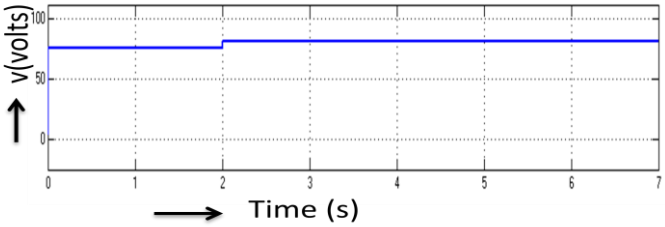

Figure 11. Input Voltage

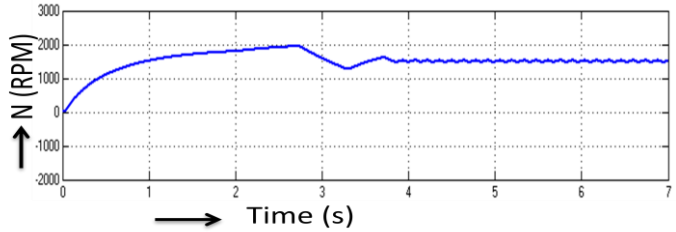

Figure 12. Motor Speed

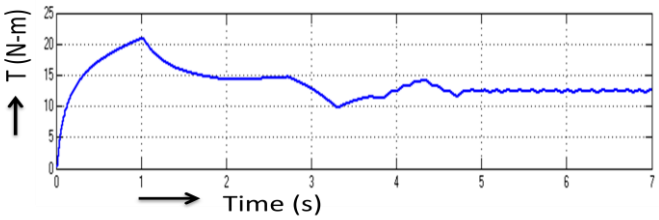

Figure 13. Motor Torque

Closed loop system with fuzzy controller is shown if Figure 14. The PI controller is replaced by a fuzzy logic controller. The inputs to FLC are error and its derivative. The step change in input voltage is shown in Figure 15. The speed response is shown in Figure 16. The speed reaches set value very smoothly. The response is shown in Figure 17. The summaries of time domain parameters are given in Table 2. It can be seen that settling time and steady state error are reduced by using FLC.

Table 2. Summary of responses with PI and Fuzzy Controllers

Controller	t_r	t_s	t_p	E_{ss}
PI Controller	1.3	4	2.8	2.5
Fuzzy	0.6	1.2	0	0.05

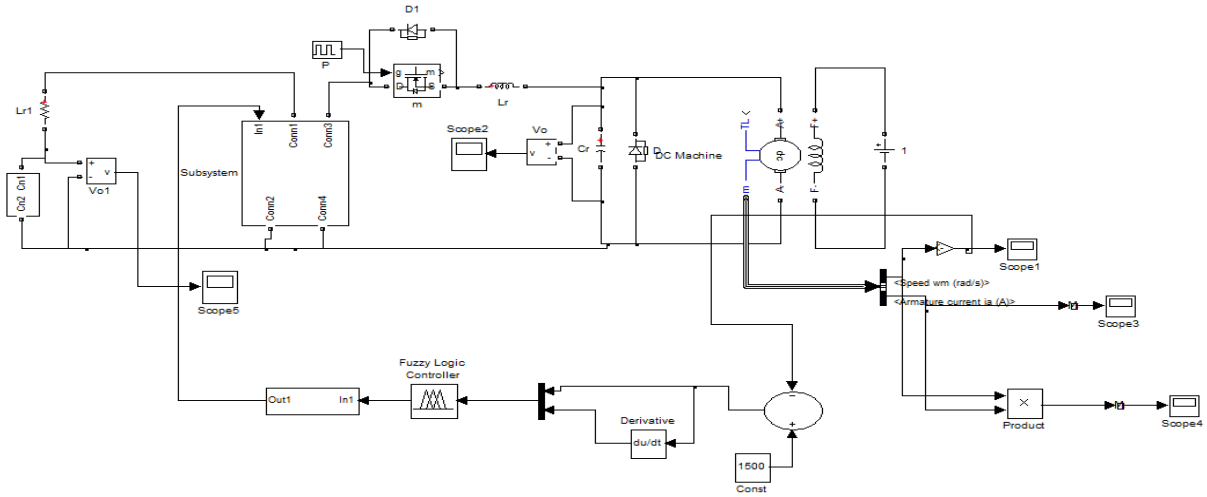

Figure 14. Closed Loop System with Fuzzy Controller

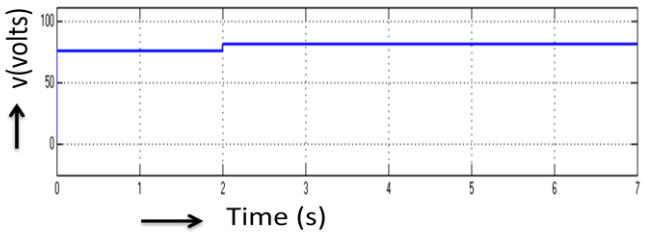

Figure 15. Input Voltage

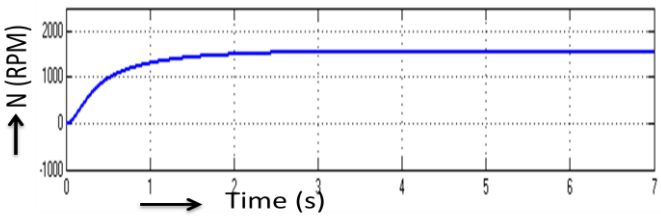

Figure 16. Motor Speed

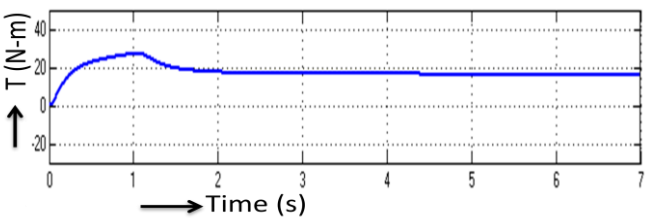

Figure 17. Motor Torque

V. CONCLUSION

Closed loop PI and FLC based SEPIC –QRC fed DC drive systems are designed, modeled and simulated using Matlab successfully. Fuzzy logic controller is proposed in the present work to improve the dynamic response of the closed loop system. The proposed fuzzy logic controlled SEPIC-QRC drive system has improved dynamic response over PI controlled drive system. The disadvantage of the FLC is that it takes longer time for tuning.

VI. FUTURE SCOPE

The Response of multi loop controlled drive system will be compared with FLC based drive system in future. The hardware will be implemented in future using PIC microcontroller for validating simulation results.

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