LOW POWER CRITICAL PATH REDESIGNED ECRL PIPELINE IMPLEMENTATION

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ABSTRACT
A pipeline style of asynchronous type is introduced where its data path is composed of a mixture of redesigned ECRL circuitry and Single Rail Domino circuitry with simple completion detection circuitry offering high performance and low power consumption. In the Low Power Critical Path Redesigned ECRL pipeline implementation method the gate with maximum input in each pipeline stage is selected and is replaced by its equivalent ECRL logic with variance in transistor aspect ratio based on an algorithm and this forms the critical path of that pipeline. The other data paths of the pipeline apart from the ECRL critical path are composed of single rail domino logic. This paper basically deals with a comparative study of the Williams PS0 pipeline technique, APCDP pipeline design and our proposed Low Power Critical Path Redesigned ECRL Pipeline Implementation. The benchmark circuits used for the comparison purpose are 2x2 and 4x4 multiplier. The simulations are done using Tanner EDA tool in 130nm CMOS Technology.

KEYWORDS—*Effective Charge Recovery logic-Critical Path-Single Rail Domino-Transistor length.*

I. INTRODUCTION

The advent of nanotechnology development in VLSI has led to the exploration of high performance asynchronous circuits due to the absence of clocks since clock tree synthesis and timing optimization have become serious problem [1]. It is therefore evident why the asynchronous circuits which do not suffer from these drawbacks have attracted sufficient amount of interest and research activity. There are many techniques adopted for asynchronous pipeline implementation out of which the most widely accepted technique was PS0 [2] and later a better and more efficient APCDP techniques were used for pipelining of asynchronous type [3],[4]. In order to overcome the shortcomings of these techniques a new method of pipelining called the Low Power Critical Path Redesigned ECRL pipeline implementation is introduced.

The LPCREP method focuses on increasing the efficiency of the circuit and making this low power critical path redesigned ECRL pipeline design more practical .In this work, the two pipeline protocols, bundled data protocol and the dual rail protocol are combined avoiding storage elements like registers and buffers thereby saving lots of space and providing a low power consumption. The various pipeline approaches have been analyzed on a 2x2 multiplier and a 4x4 multiplier. The benchmark circuits are implemented in three pipeline implementations that are the PS0 pipeline, APCDP pipeline and the proposed LPCREP pipeline and their power consumption as well as no. of transistors used is compared and the results are drawn. ECRL implementation is proposed in many other papers with Sutherland C pipeline structures but its redesigned implementation with APCDP architecture in our proposed work has far reaching affects on power consumption and silicon area used. [5].

Many possible design configurations can be provided for the simulation purpose but this work has been brought to a possibility by means of Tanner Software. The rest of this paper is constructed as follows: Section II discusses basic architecture of the Low Power Critical path Redesigned ECRL Pipeline Implementation (LPCREP). The proposed LPCREP approach is discussed in Section III.

Simulation results of the benchmark circuits are presented in Section IV. In Section V the conclusion of analysis is presented.

II. LOW POWER CRITICAL PATH REDESIGNED ECRL PIPELINE IMPLEMENTATION

2.1 LPCREP overview

In the proposed redesigned ECRL pipeline method a critical path is arbitrarily constructed by identifying the maximum no. of inputs in a pipeline stage. This gate takes the maximum time to complete its evaluation in that pipeline and thus we replace the gate by the Redesigned ECRL logic. The length of true PDN and its complimentary PDN are adjusted such that the total length will be equal to the maximum series transistor present in the pipeline stage thereby increasing the logical effort of the gate and thus the delay irrespective of the input combination. The rest of the data paths are implemented in non inverting single rail domino logic. The ECRL gate of each pipeline stage is followed by a 2 input NOR gate that acts as completion detection. Since SLG's implemented in the Critical path as in APCDP architecture is replaced by redesigned adiabatic ECRL, the no. of transistors and power are reduced. [6]

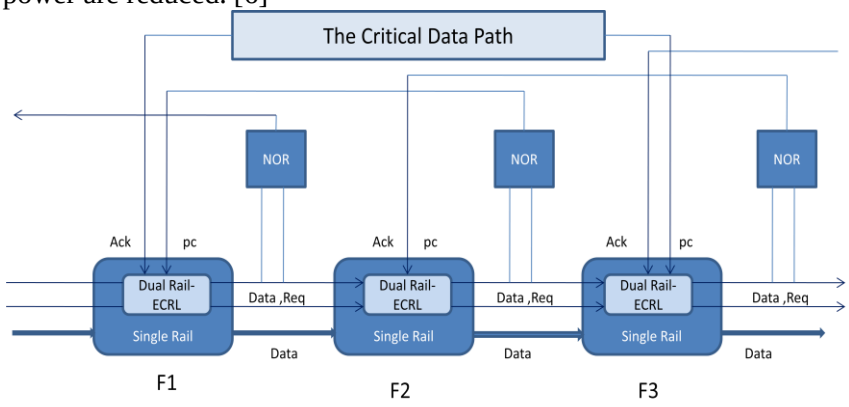
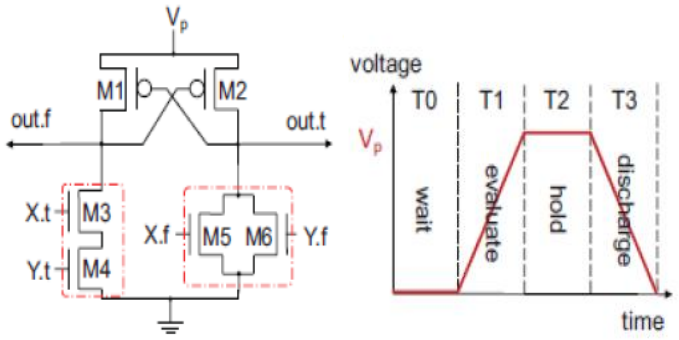


Figure 1. Block Diagram LPCREP

Figure1 shows the block diagram of the proposed architecture. The pipeline is designed based on a critical path that is constructed using a special ECRL logic. The rest of the data paths are composed of single-rail logic and they only transfer data signal and no handshake signal. For the ECRL based pipeline stage, the detection circuit is a simple static NOR. Its output is connected to the precharge of their previous pipeline as shown in the above figure. The protocol followed by Redesigned ECRL is similar to APCDP. The difference is that SLGs of the critical path which uses more no. of transistors and which has more power dissipation is now replaced by a simpler Redesigned ECRL logic gate that uses less no. of transistors causes less power dissipation.

2.2 ECRL Logic Gate

ECRL gate is a type of adiabatic logic gate [7], [8] and thus will have lower power dissipation when compared to the other CMOS logic gates. Figure 2 shows the structure of an ECRL AND gate. It can be observed that by using an ECRL gate we obtain both the true and false logic just like Dual Rail logic. As shown in Figure 2(a) an ECRL gate is powered from the node, Vp. In case of synchronous circuits this Vp is generally connected to the clock used. In the proposed Redesigned ECRL pipeline, the node Vp is connected to the output of the completion detection of the next stage.



(a) (b)

Figure 2.ECRL logic –AND/NAND gate and its operating phases

An ECRL gate consists of four operating phases as shown in the Fig. 2(b). The first phase is the Wait phase and here the node Vp is 0 and thus since the power supply for the ECRL gate is off, both out.t and out.f of the gate is 0 irrespective of its inputs. The second phase is the Evaluation phase and here the node Vp rises from 0 to VDD and the gate draws current from the node and starts its evaluation till out.t and out.f reaches its final values. The third phase is the Hold phase an d here the Vp node remains at VDD and thus the result out.t and out.f is held to its current state as long as Vp is VDD. The final stage is the Discharge phase and as the term discharge suggests the power node Vp falls from VDD to 0 and thus the values stored in the out.t and out.f becomes eventually 0 that is empty.

2.3 ECRL (L) Logic Gate

The operation of ECRL (L) as shown in Figure 3 is same as the normal ECRL gate except for the fact that the evaluation depends upon enable and enable bar signal.

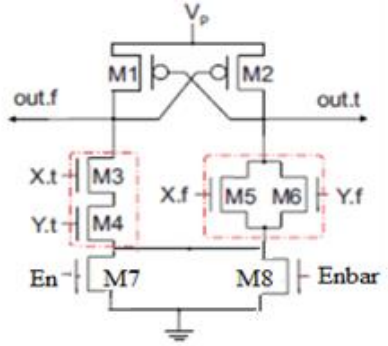


Figure 3.ECRL logic –AND/NAND

In the proposed pipeline, it is always preferred that the ECRL max input gate is connected to ECRL gates of subsequent pipeline stages. In few cases, there won't be a connection of the maximum input gate of the current pipeline stage with that ECRL gate of the previous stage. In that case the complimentary outputs of the ECRL gate of the previous stage is given as enable and enable bar signals to the ECRL(L) gate of the current pipeline stage ensuring that the current pipeline stage begins its evaluation late when compared to the other noncritical path single rail domino gates in the rest of the pipeline.

III. LOW POWER CRITICAL PATH REDESIGNED ECRL PIPELINE ARCHITECTURE

3.1 LPCREP Architecture

Figure 4 shows the structure of Redesigned ECRL implementation. The darkened arrow represents the critical path (ECRL data path), the normal arrow represents the non critical data paths (single rail data paths), and the hollow arrow represents the output of single-rail to dual-rail encoding (SD) converter.

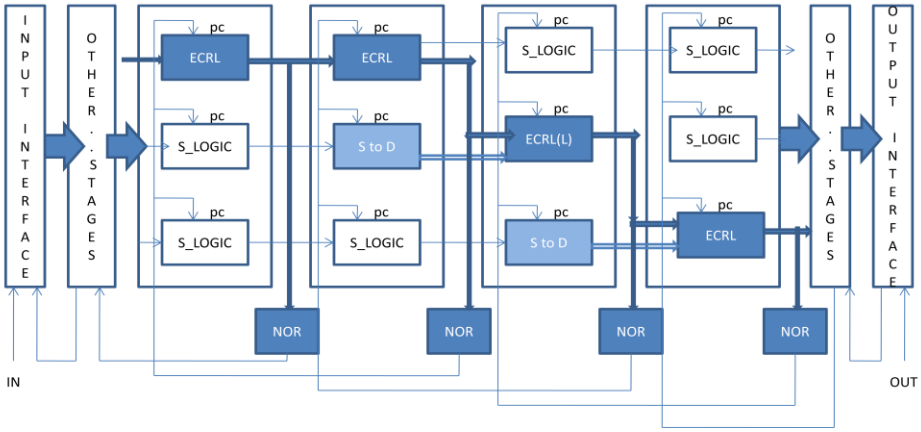


Figure 4. Architecture of LPCREP

In each pipeline stage, a NOR gate is used as the completion detector to generate a total done signal for the entire data paths by detecting the critical data path alone. Each total done signal is fed to the precharge node of the previous pipeline stage. Since the completion detector only detects the constructed critical data path, the noncritical data paths do not have to transfer encoded handshake signal along with the data anymore. Therefore, single rail domino gates are used in the noncritical data path to save logic overhead. SD Converters are used to allow the single rail outputs to be fed as inputs to ECRL logic. [9], [10].

The input data is given to the pipeline with spacer in between as shown in Figure 5, since it follows a Four phase dual rail protocol .Here the first bit of (0,1) is true input and the second bit is the complimentary input representing data0.

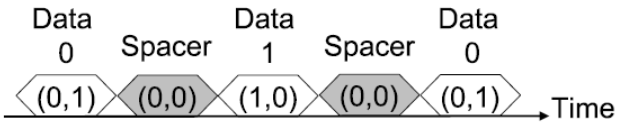


Figure 5. Data Transfer by Four Phase Dual Rail Protocol

3.2 LPCREP Critical Path Design

It is difficult to construct a stable critical data path using traditional logic gates because of their delay dependence on the type of data being fed. The critical signal transition varies from one data path to others according to different input data patterns. Since in the APCDP pipeline implementation, synchronized Logic Gates have solved the gate-delay data dependence problem, a stable critical data path can be easily constructed. The same steps are adopted for an ECRL gate and the steps are as follows with an additional condition of redesigning the ECRL gate used.

1) Find a gate with the largest number of inputs in each pipeline stage;
2) Change these maximum input gates to ECRLs;
3) Connect ECRLs together to form a critical data path.

The basic idea of finding the critical signal transition is that embedding an ECRL in each pipeline stage and making the ECRL to be the last gate to start and finish evaluation. This is made possible by slightly modifying the aspect ratio of the gate PDN. The steps are as follows.

1) Find the maximum no. of series transistor (N) in PDN present in that pipeline stage.
2) The length of the transistors used in ECRL gate in its PDN is adjusted such that the entire PDN takes an equivalent of N transistors to complete the evaluation irrespective of the input pattern.

Consider for example a 2 input AND gate being selected as the maximum input gate of the pipeline stage as shown in Figure 2(a). If the maximum no. of transistors present in the pipeline stage N=3.Then the length of the transistors M3 and M4 should be made (N/n) x L, that is the no. of series transistor in PDN network consisting of M3 and M4 being n=2, we should change the length of these two transistors to 3/2L where L is the minimum length of the transistors used for the rest of the circuitry. Considering the other PDN of the ECRL gate, the no. of series transistor for M5 and M6 is n=1.Thus its length of M5 and M6 are changed to 3/1L.On doing so in the evaluation stage

irrespective of the input pattern the PDN network need to travel 3L of the transistor path which accounts for the maximum time to complete evaluation. Thus it ensures that the Redesigned ECRL gate is the last gate to finish its evaluation when compared to the other gates in the pipeline stage. The result of ensuring maximum delay in the critical path ECRL circuitry can be also be proved by Logical Effort method. [11].

It is always ensured that the ECRL is the last gate in the respective pipeline to start its evaluation by connecting each pipeline stage's ECRL gates. In the first pipeline stage, the critical signal transition is on the output of the ECRL because all gates evaluate at the same time. After connecting each pipeline stage's ECRL together, the ECRL in the following pipeline stage would be the last gate to start evaluation since its evaluation begins from the output of the ECRL gate of the previous stage. As a result, the connected ECRL data path becomes a stable critical data path.

Connecting each pipeline stage's ECRL together is carefully done. When searching for maximum input gate, there might be condition where there may be more than one gate having same no. of max inputs in the pipeline. It is best to select the maximum input gate that is originally linked to the maximum input gate in the previous pipeline stage. After changing these gates to ECRLs, ECRLs are naturally linked. However, if we cannot find the linked maximum input gates in neighbour stages, ECRL (L) needs to be used to solve the linking problem. This is clearly shown in the Figure 4.

IV. SIMULATION RESULTS

The asynchronous pipeline technique was simulated using Tanner software in the high-performance 130-nm technology and with temperature, 25°C. The supply voltage used in the simulations is 5 V and operates at 1-GHz clock frequency. The 2x2 multiplier and a 4x4 multiplier are used as benchmark circuits and their power and the number of transistors used are being compared.

The Simulations shown below are that of a 2x2 and a 4x4 multiplier that are implemented in the proposed LPCREP implementation style with pc denoting the acknowledgement signal of the final pipeline stage that indicates the completion of the module operation.

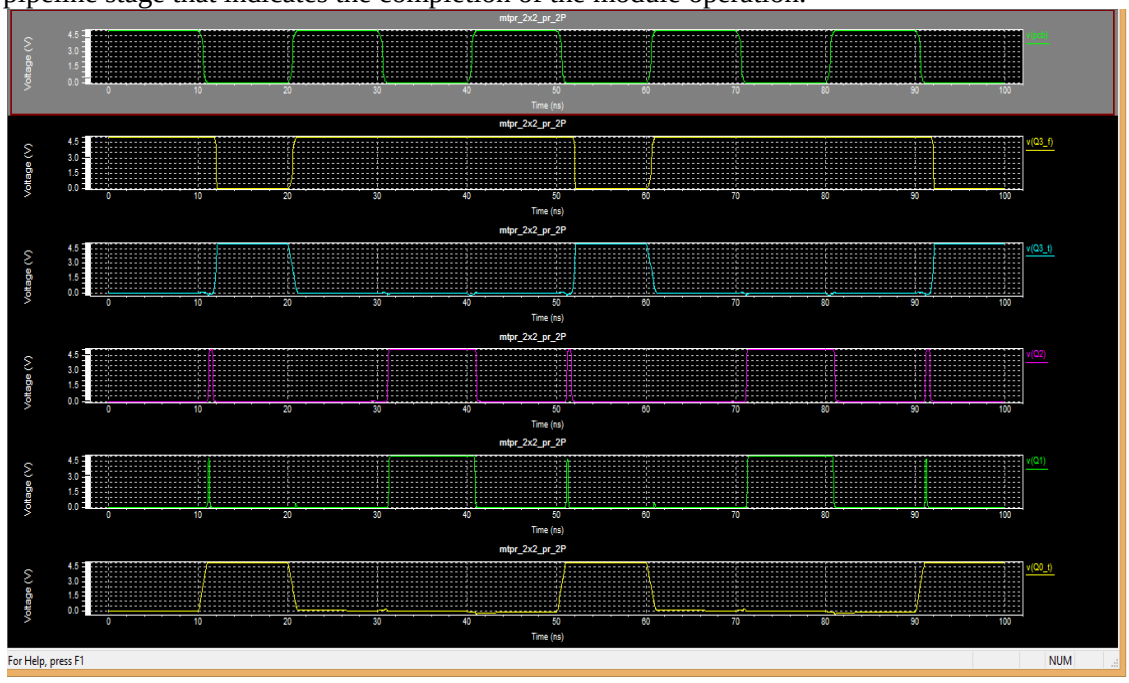


Figure 6. Simulation of a 2x2 multiplier with input 3x3 and 3x2 given alternatively

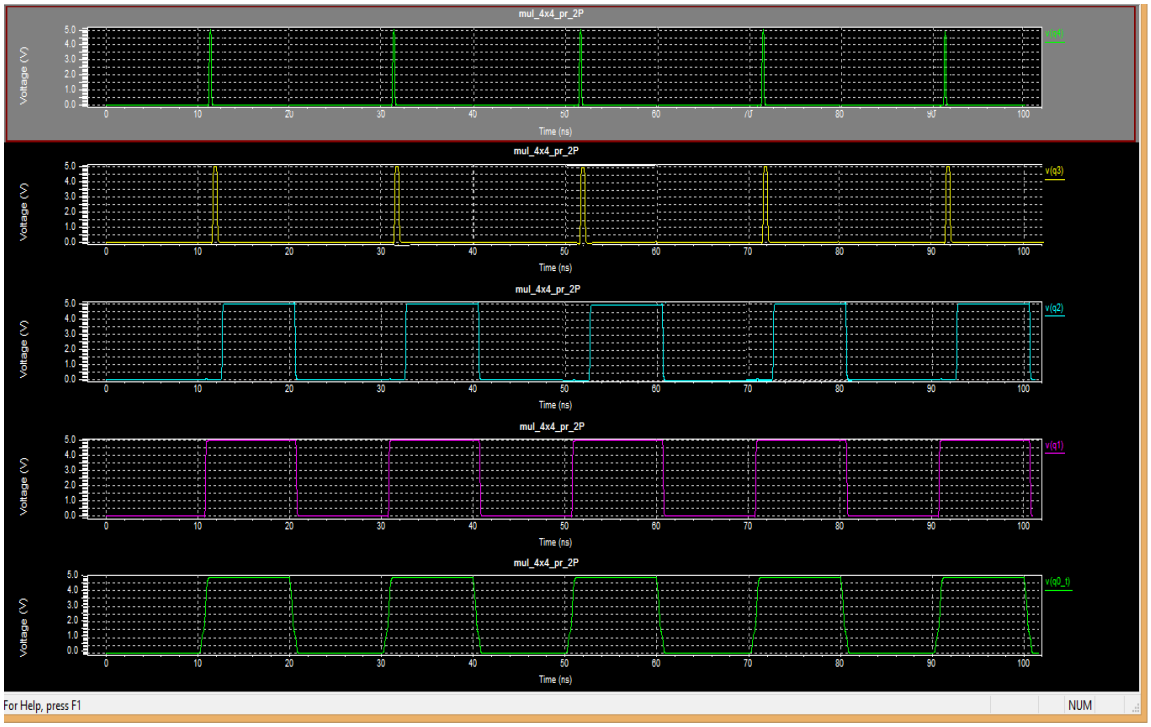


Figure 7. Simulation of 5 LSBs of a 4x4 multiplier with input 13x3

The power consumed and the no. of transistors used in each pipeline stage are compared and shown in the table given below.

Table 1

Evaluation results of 2x2 and 4x4 array multiplier

PIPELINE STYLE	POWER CONSUMED (Watts)		NO. OF TRANSISTORS	
	2x2 multiplier	4x4 multiplier	2x2 multiplier	4x4 multiplier
PS0	5.517 e-002	1.625 e-001	120	841
APCDP	1.937 e-002	1.342 e-001	141	658
LPCREP	1.737 e-002	2.713 e-002	117	446

It has been observed that the PS0 asynchronous pipeline implementation shows maximum power dissipation. When APCDP pipeline implementation is considered the power has reduced by around 62.5% and no. of transistors used has increased by 17.5%.When the proposed LPCPREP pipeline implementation is considered power has reduced by 68.1% and no. of transistors are reduced by 2.5% for a 2x2 multiplier.

Similarly the power has reduced by around 30.5% and no. of transistors used has reduced by 21.8% in APCDP pipeline. Power has reduced by 56.4% and no. of transistors is reduced by 46.9% for a 4x4 multiplier in proposed LPCREP configuration. Thus LPCREP pipeline implementation has lesser power dissipation and smaller silicon area when compared with other pipeline implementations.

V. FUTURE WORKS

Low Power single rail domino/Redesigned ECRL asynchronous pipeline technique can be implemented in various pipeline networks .Its power consumption can be reduced further by reducing the leakage noise and ECRL precharge spikes. Pipeline Technique can be applied not only to the

linear pipeline structure but also for more complex data paths such as fork and join structures they can be applied.

One of the major applications of our proposed work is Arm based asynchronous processors such as AMULET-3 and TITAC-2. It follows RISC based architecture and has micro-pipeline structure. They can also be implemented in few processors based on CISC architectures such as Lutonium and A8051 and also in DSP processors. Here apart from fetch and decode stage, the execution stage consisting of multipliers, shifters, ALUs etc. which were originally implemented in synchronous design can now be implemented with our proposed LPCREP Asynchronous non-buffered Pipeline Implementation. This can considerably reduce the power consumption and the no. of gates used especially for a large data width computation.

VI. CONCLUSIONS

The proposed method of Redesigned ECRL implementation has so far obtained the least power requirement providing transistor sizing constraint for the ECRL circuits that are implemented in the critical path. Not only that but also they have provided a simple detection circuit that does not occupy more space. Apart from few noise spikes that occur during the pre-charging of ECRL there are no prominent setbacks of this design and thus can be used for many applications. This linear pipeline Design can be extended to Fork and Join Structures and one of the main applications of this pipeline design is that it can be implemented in execution stage with large data width consisting of multipliers, shifters, ALUs etc. of the asynchronous ARM processors such as AMULET 3 and TITAC 2.

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