A METHODOLOGY IN THE DESIGN OF TESTABLE SEQUENTIAL CIRCUITS BY USING REVERSIBLE LOGIC

S Mohan Das[1]Challa Madana gopal[2] and Mohammad Mahaboob Basha[3]
[1]Assistant Professor Department of ECE, AVR & SVR CET, Nandyal, India
[2]PG Student, Department of ECE, AVR & SVR CET, Nandyal, India
[3]Associate Professor Department of ECE, AVR & SVR CET, Nandyal, India

ABSTRACT
The methodology is to design conservative logic gates based sequential circuits by using reversible logic gates. The FREDKIN gate based sequential circuit performs the classical conventional based sequential circuits in terms of ATPG operations with stuck at fault models. Every sequential circuit which based on conservative logic can test for stuck-at 0 and stuck-at 1byusing two test vectors 0 and 1.The testable design latches, that is, master-slave flip-flop's and DET (Double edge triggered) flip-flop's with two vectors are presented in this paper in the form of reversible logic. The need for any type of scan path access to internal memory cells can be eliminated in the proposed design. In this approach the methodology cover the overall missing or additional cell defect in the QCA (quantum-dot cellular automata) of the FREDKIN gate and this paper also compare the delay parameters in the form of circuits normal D-latch, testable reversible D-latch with FREDKIN. A new conservative logic gate by name Multiplexer conservative QCA gate which is not reversible in nature but has properties similar to the FREDKIN gate of working as 2:1 multiplexer has been presented. With the schematic and layout representation for the design module the power is calculated.

KEYWORDS: *QCA, ATPG, QED, FREDKIN Double Edge Triggered, TMR, single-event UPSET.*

I. INTRODUCTION ABOUT QCA

QCA (quantum dot cellular automata) concepts with a promising future engineering for computing. It takes nice advantage of a physical effect: the Coulomb force that interacts between electrons. There additionally exists a different implementation that uses magnetic fields; however this sensible course can't cover magnetic QCA for currently [1].Though' it's still troublesome to provide and operate with these devices below typical temperature conditions; simulations predict promising numbers, like theoretical clock rates of several THz.

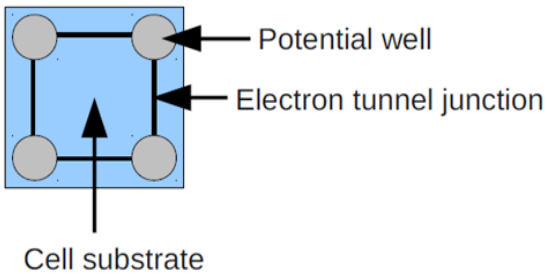

Fig.1 Anatomy of a QCA cell

1.1. The QCA cell:

In distinction to electronic based on transistors, QCA doesn't operate by the transport of electrons, however by the adjustment of electrons in a small limited area of a few square manometers. QCA is

enforced by quadratic cells, the so-called QCA cells. In these squares, specifically four potential wells are located, one in every corner of the QCA cell (see figure). Within the QCA cells, specifically 2 electrons are locked in. they'll solely reside within the potential wells.

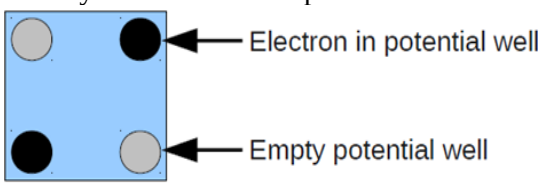

Fig.2 Electrons in potential wells

There are two diagonals in a square, which suggests the electrons will reside exactly two possible changes in the QCA cell. [2]concerning these two arrangements, they're elucidated as a binary '0' and binary '1', i.e. every cell can be often in two states. The state '0' and also the state '1', as depicted in figure 3. A binary representation is acquainted, as Boolean logic is employed already in today's computers. There, a high voltage is usually understood as binary '1' and a low voltage as binary '0'.

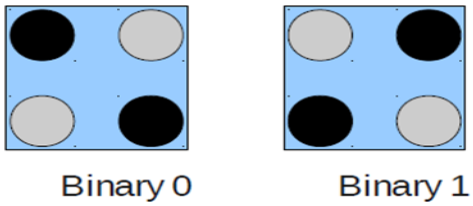

Fig.3 Binary interpretation of adjustments

1.2. Latches and Flip-Flops

The circuit's store data regarding the previous history of inputs are referred to as storage or memory elements. By connecting the outputs back as inputs of smaller range of gates primitive storage component are made. Such circuits are binary cells which capable of storing one bit data. They need two outputs, one for the normal output and other for the complement value of bit of data stored in it. Primitive memory components are represented broadly into two categories: latches and flip-flops. Latch which has only data inputs are called as an unlocked latch or only latch. The Level sensitive latches have an enable input in addition, sometimes referred to as the clock. Level-sensitive latches ceaselessly sample their inputs once they are enabled. Any modifications within the input levels is propagated to the output. State held by the latch determined by the last value of the inputs the once the enable signal is unasserted [2].

Flip-flops differ from latches in their output which change with the clock edges, whereas latches changes output once their inputs modify during level sensitive of the clock. Flip-flops are characterized on the idea that output modifies only on the clock transition. Flip-flops are of master-slave flip-flops, positive edge triggered flip flops and the negative edge triggered flip flops. The inputs samples on the low-to-high clock transitions in a positive edge triggered flip flop's while a negative edge-triggered flip-flop works in a similar fashion to it, during the high-to-low clock transitions the input is sampled. A master-slave flip-flop is made from two stage separate flip-flop. The initial stage samples the inputs on the clocks rising edge. On the clocks falling edge the second stage transfer the input signals to the output. These circuits have two inputs in addition to the control inputs as third input. The output of the flip-flop and latch are forced to the logic 1(high) and logic 0(low) states by Preset, Clear inputs respectively, irrespective of the flip flop and latch inputs.

Section II describes Design of testable Reversible sequential circuits, Construction of online testable sequential circuits using reversible logic presents in Section III, Section IV presents different types of Reversible Gates, Section V demonstrates about Reversible logic, Section VI describes architecture and design of Reversible Sequential Circuits, Section VII presents Proposed Multiplexer, Results are presented in Section VIII, Section IX illustrates QCA design of Mux-Cqca gate and Section X Concludes with Future scope.

II. DESIGN OF TESTABLE REVERSIBLE SEQUENTIAL CIRCUITS

The proposed sequential circuits based on conservative logic gates[5] outperform the sequential circuits enforced in classical gates in terms of testability. Any serial circuit based on conservative logic gates is tested for classical unidirectional stuck-at faults employing only two test vectors. The two test vectors are all 1's, and all 0's. The design styles of two vectors testable latches, master-slave flip-flops and double edge triggered (DET) flip-flops are presented in this project. The importance of the projected work lies within the fact that it provides the design of reversible sequential circuits completely testable for any stuck-at fault by only two test vectors, thereby eliminating the necessity for any type of scan-path access to internal memory cells [3].The reversible design style of the DET flip-flop is proposed for the first time within the literature. The top module also depicted the application of the proposed approach toward 100% fault coverage for any single missing/additional cell defect within the quantum-dot cellular automata (QCA) layout of the Fredkin gate [4].modules are presenting a new conservative logic gate known as Multiplexer conservative QCA gate (MX-cqca) [6]that's not reversible in nature however has similar properties because the Fredkin gate operating as 2:1 multiplexer. The proposed MX-cqca gate surpasses the Fredkin gate in terms of complexness (the number of majority voters), speed, and area.

III. CONSTRUCTING ONLINE TESTABLE CIRCUITS USING REVERSIBLE LOGIC

With the discovery of nano-technology, circuits are susceptible to risk of transient faults which will occur in its operation. Of the various sorts of transient faults described within the literature, the single-event upset (SEU) is notable [7]. Traditional techniques like triple-modular redundancy (TMR) consume larger area and power. Reversible logic has been gaining interest in the recent overdue to its less heat dissipation characteristics. This project proposes the following:

1) A unique universal reversible logic gate (URG) and a set of basic sequential elements that would be used for building reversible sequential circuits, with 25% less garbage.

(2) A reversible gate which will minimize the functionality of a lookup table (LUT) which can be used to construct a reversible field-programmable gate array (FPGA); and

(3) Automatic conversion of any given reversible circuit into an online testable circuit which will detect for any single-bit errors, together with soft errors within the logic blocks, employing theoretically proved minimum garbage that is considerably lesser than the most effective.

Conservative logic may be a logic family which exhibits the property of equal number of 1's within the outputs as there are within the inputs. Conservative logic are often reversible in nature or might not be reversible in nature in certain cases. Reversibility is that the property of circuits in which inputs and outputs exhibits one to-one mapping.[5] In other words for every input vector there's a unique output vector and similarly for every unique output vector there exists a unique input vector. This paper tends to propose the design of testable sequential circuits supported by conservative logic gates. The proposed technique can watch out the fan-out at the reversible latches output which may additionally disrupts the feedback to make them appropriate for testing only by two test vectors, all 0's and 1's. In alternative words, circuits can have feedback when functioning in the normal mode.[4] Nevertheless, in order to find faults within the test mode, our proposed technique can disrupt feedback to form combinational circuits from conservative reversible latches testable. In the projected technique aimed towards the design of two vectors testable flip-flops like master-slave flip-flops, double edge triggered (DET) flip-flops. This work is critical as it was providing the design of reversible sequential circuits which are completely testable for unidirectional stuck-at faults by only two test vectors i.e. all 0's and 1's. Further, this paper tends to enforce the Fredkin gate within the QCA [3] technology and ascertained that all 0's and 1's test vectors cannot offer 100 percent fault coverage for any single missing or additional cell defect within the QCA(quantum dot cellular automata) layout of the Fredkin gate. Therefore, to possess the 100 percent fault coverage for any single missing or additional cell defect by all 0s & 1's test vectors, it was detected the QCA devices within the QCA layout of the Fredkin gate which can be replaced with their fault tolerant components so as to provide 100 percent fault coverage.

IV. REVERSIBLE GATES

A combinational digital logic circuit is said to be reversible in nature if it maps every unique input pattern to a corresponding unique output pattern.Many types of reversible gates are available like Fredkin, Toffoli, Feynman, and inverter/NOT. Both inputs A and B are passed directly through the gate to P and Q outputs respectively. The R output uses additional complex logic, R = C ⊕ AB. By setting C = zero, it becomes a logic AND gate R = AB.

4.1. Fredkin Gate:

It is a 3x3 gate and its logic circuit is as depicted in the figure.4 It has a quantum cost of five. It is used to Multiplexer's [6].

4.2. Peres Gate:

It is a 3x3 gate and its logic circuit is as depicted in the same figure. It has a quantum cost of four. It is used to implement various Boolean functions like AND, XOR.

4.3. HNG Gate:

It is a 4x4 gate and its logic circuit is also depicted in the same figure. It has a quantum cost of six. It is used to realize ripple carry adders. It will produce both sum and carry in not exceedingly single gate therefore minimizing the garbage gate counts.

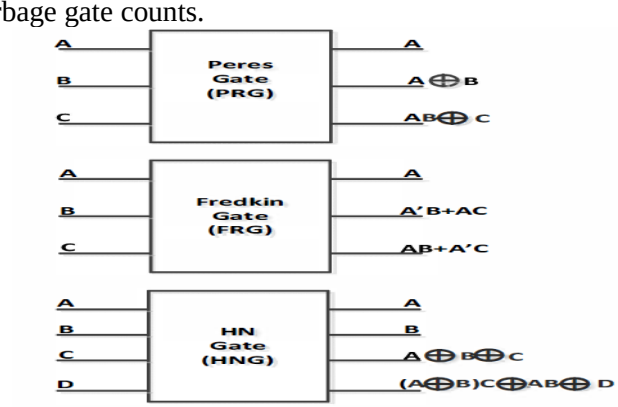

Fig.4 Reversible logic gates

V. REVERSIBLE LOGIC

Reversible logic may be a promising computing design style paradigm that presents a technique for constructing computers that manufacture no heat dissipation. Reversible computing emerged as a result of the application of quantum mechanics principles towards the manufacture of a universal computing machine. Specifically, the basics of reversible computing are supported by the connection between entropy, heat transfer between molecules in system, the chance of a quantum particle occupying a selected state at any given time, and also the QED (quantum electro dynamics) between electrons when they are in dose proximity. The fundamental principle of reversible computing is that a objective device with a similar number of input and output lines can create a computing surroundings wherever the electrodynamics of the system yield prediction of all future states based on known past states, and also the system reaches each possible state, which results in no heat dissipation. A reversible logic gate associates N-input N-output logic device in which one to one mapping exists between both the input and also the output. It not only helps us to see the outputs from the inputs however it additionally helps us to unambiguously recover the inputs from the outputs. Garbage outputs are those that don't contribute to the reversible logic realization of the design. Quantum cost refers to the value of the circuit in terms of the value of a primitive gate. Gate count is that the range of reversible gates used to realize the given logic functions. Gate level refers to the different number of levels that are needed to realize the given logic functions.

VI. ARCHITECTURE AND DESIGN OF REVERSIBLE SEQUENTIAL CIRCUITS

Conservative logic may be a logic family which exhibits the property of equal number of 1's within the outputs as there are within the inputs. Conservative logic is often reversible in nature or might not be reversible in nature in certain cases. Reversibility is that the property of circuits in which inputs and outputs exhibits one to-one mapping. In other words for every input vector there's a unique output vector and similarly for every unique output vector there exists a unique input vector. Conservative logic is termed as reversible conservative logic whenever there exists a injective mapping in between the inputs and the outputs vectors in conjunction with the property that there's equal range of 1's within the outputs as within the inputs. Conservative logic circuits aren't reversible, if injective mapping in between the inputs and the outputs vectors isn't preserved.

6.1. Design of Testable Negative Enable Reversible D Latch:

When E = 0, negative enabled reversible D latch can propagate the input D to the output Q. Otherwise it remains in a similar state. The characteristic equation of the negative enabled D latch is Q+ = D•$\bar{E}$+E•Q.[10].

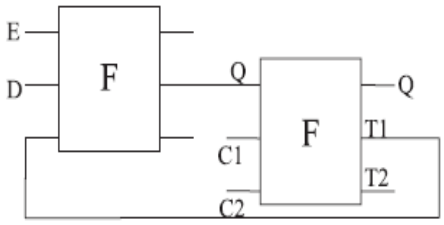

Fig .5 Negative enable testable D latch Using FREDKIN gate.

The negative enable reversible D latch characteristic equation are often mapped on to the Fredkin gate second output as depicted in Fig 5. The second Fredkin gate within the design take cares of the Fan out. The second Fredkin gate within the design additionally helps in creating the design which is testable by only two test vectors i.e. all 0's and 1's by disrupting feedback based on control signals C1 and C2 values same as explained for the positive enable reversible D latch. It in designing testable reversible master-slave flip-flop's negative enabled D latch can be useful, because as it works as a slave latch within the testable reversible master-slave flip-flops during which no clock inversion is needed. The main points of it are mentioned within the section describing reversible master-slave flip-flop's.

6.2. Design of Testable Reversible DET Flip-Flops:

The DET flip-flop is a computing circuit which samples and stores the information at each edge of the clock, that's at each of the rising and falling edges of the clock. The most common approach used in designing this flip-flop is master- slave strategy [8]. In the planned work, E employed interchangeably used in situ of clock. When E = 1 (high clock), the master propagates the input date whereas the slave latch remains in the previous state in the negative edge triggered master-slave flip-flop. Once E = 0 (clock low), the master remains in the storage state and the slave latch propagates the output of master to its output.

In order to overwhelm the problem, concept of DET flip-flops is introduced, which samples the information at both edges of the clock. Thus, DET flip-flops will receive and sample two data values in same clock period therefore frequency of the clock are often reduced to half the master-slave flip flop while retaining a similar data rate. The half frequency operations enable the DET flip flops substantially useful for low power computing as frequency is directly proportional to consumed power.

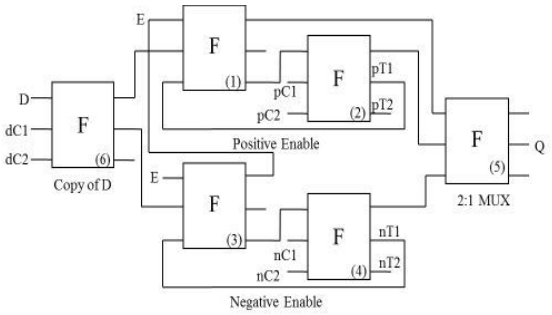

Fig.6 Fredkin gate-based DET flip-flop

In the proposed design style of the positive enable testable reversible D latch, testable reversible DET flip-flop, and also the negative enabled testable reversible D latch are organized in parallel. The Fredkin gate which is labelled as 5 functions as the 2x1 MUX which transfer the output from one among these latches which is in the storage state to the output Q. Here pC1 and pC2 are the control signals of the testable positive enabled testable reversible D latch and testable reversible negative enabled D latch has the control signals nC1 and nC2. Depending on the values of the control signals pc1, pc2, nc1, and nc2 the testable DET flip-flops functions either in test mode or within the normal mode.

VII. PROPOSED MULTIPLEXER

7.1. Conservative QCA Gate:

For many of the design styles, the designer might probably have an interest in using the testing advantages of conservative logic but not saving the number of QCA cells [9]. Thus, in this project, the top module tends to propose a new conservative logic gate that's conservative in nature however isn't reversible. The proposed conservative logic gate is termed as multiplexer conservative QCA gate.

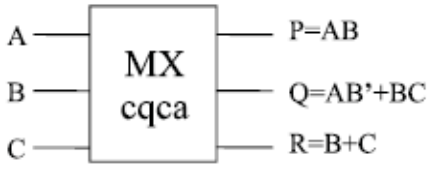

Fig.7 Proposed MX-CQCA gate

It has 3 inputs and 3 outputs. MX-cqca [11] has one of its outputs operating as a multiplexer which will facilitate in mapping the sequential circuits based on it, whereas the other 2 outputs work as AND and OR gates, severally. The mapping of the inputs to outputs of the MX-cqca is: P = AB; Q= $A\bar{B}$+BC; R = B + C, where A, B, and C are the inputs while P, Q, R are the outputs, severally. Fig 7 depicts the diagram of the MX-cqca gate. Table V depicts the truth table of the MX-cqca gate. The table verifies the gate's conservative logic nature, i.e., that the number of 1's within the inputs is equal to the number of 1's within the outputs. Figs.8 shows the QCA design style of the proposed MX-cqca gate. From the QCA style, in this paper the schematic results can observe that the proposed MX-cqca gate needs four clocking zones and 5 majority gates for its QCA implementation.

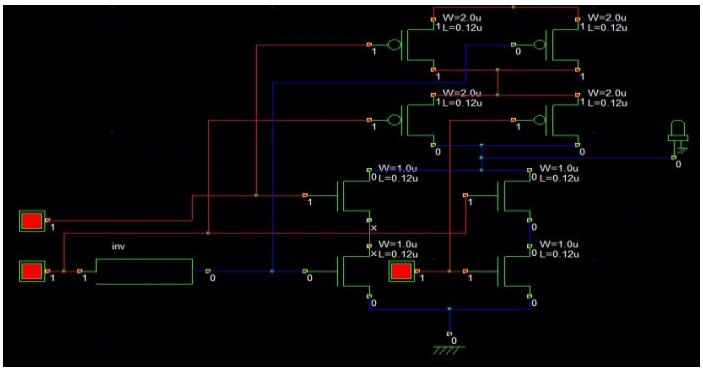

Fig. 8 Design of MX-CQCA gate.

7.2. Design Methodology for Non reversible Testable Design Based on MX-CQCA Gate:

The proposed conservative logic gate MX-cqca is helpful to design any majority logic and multiplexer logic-based testable non-reversible sequential circuits. In the existing literature, 13 standard functions are proposed to represent all three-variable Boolean functions. These 13 functions are wide employed in QCA and majority logic-based synthesis so as to design any complicated function supported by MX-cqca, the proposed design methodology is often summarized within the following 3 steps. In first step the input is decomposed into the Boolean network in which each node has virtually 3 variables. This step is analogous to the design methodology proposed. In second step the 3 variable functions generated at each node of first step is mapped to its MX-cqca based implementation. The mapping relies on the library of thirteen standard functions enforced using the MX-cqca. In third step the nodes that have fan-out of greater than 1 are identified, and MX-cqca gates are used to form the copy of these signals, that have fan-out of greater than 1.

VIII. RESULTS

8.1. Simulation Results:

The simulation results for stuck-at 1 and stuck-at 0 faults are shown in figure 9 and figure 10

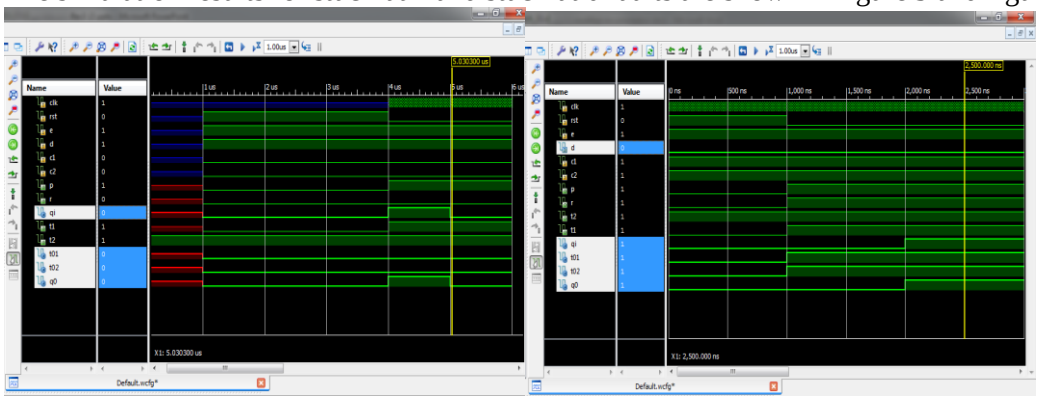

Figure 9.simulation result of stuck-at 1**Figure 10.**simulation result of stuck-at 0

IX. QCA DESIGN OF MUX-CQCA GATE

The transistor level and gate level schematic of QCA based mux-cqca logic is shown in figure 11 and figure 12. The simulated output waveforms for the designed gate is shown in figure 13.

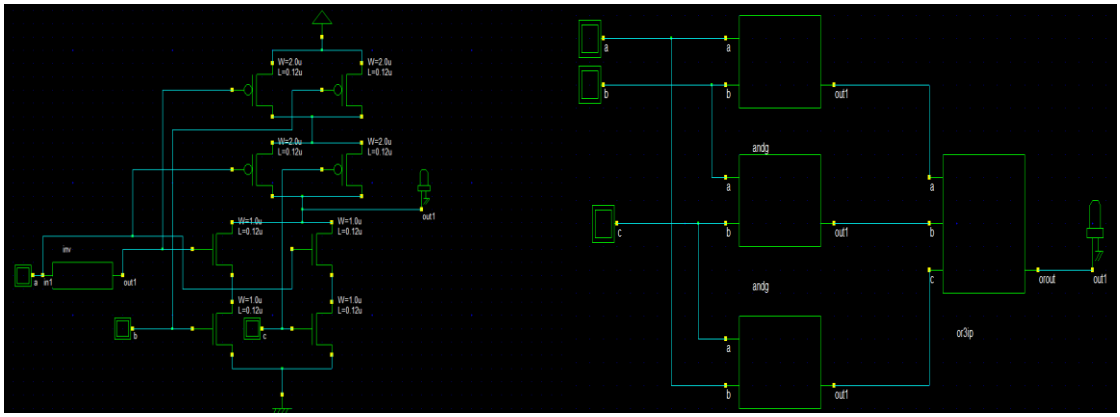

Figure 11.Figure 12.

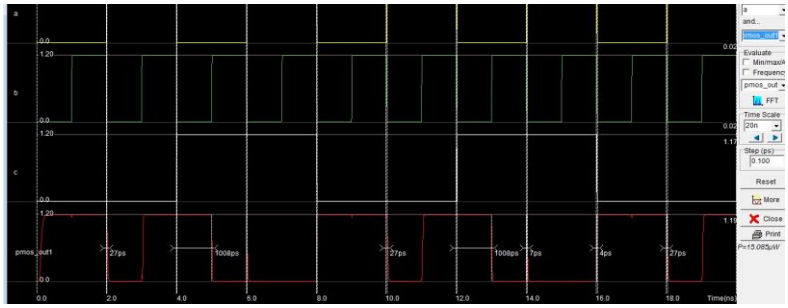

Figure 13. Output waveformsof mux-cqca gate.

9.1. Synthesis results:

Table 1 Performance Calculations of Testable Reversible Fredkin D Latch

Parameter	Generated value
Total delay	4.063ns
Total REAL time to Xst completion	6.00 secs
Total CPU time to Xst completion	5.30 secs

Table 2 Power calculations

Total device power	76mw
Total LUT's of selected device	9312
Total LUT'S generated for top propose module	2
Power generated for top propose	0.0163mw [(2*76)/9312]

Table 3 Energy factor calculations:

Parameter	Generated value
Energy factor (power*time)	0.09 J

Table 4 Comparison Table

	Timing report	Energy
D latch testable reversible	4.063ns	0.1048j
Normal D latch	5.009ns	0.09j

X. CONCLUSION AND FUTURE WORK

Testing is required to ensure the quality and reliability of a circuit. Testing reversible circuits is a challenging parameter as the levels of logic are significantly larger than the standard logic. Thus reversible sequential circuits are designed using reversible and conservative logic and tested for stuck-at-faults. In this paper reversible Fredkin D Latch and QCA based mux-cqca sequential circuits have been designed, the parameters like performance, delay, power and energy calculated by simulation and the values are tabulated in table 1, table 2, table 3 and table 4. From the simulation results it is observed that the designed gates consume less power while testing is performed. In future, with different types of reversible gates like feyman, TSG, Peres, double feyman and Toffoli gates by enhancing the gate level structures with the improvements of various parameters based on research analysis eventually further power consumption can be reduced on both combinational and sequential circuits.

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AUTHORS BIOGRAPHIES

S.Mohan Das received the B.Tech degree in Electronics and Communication Engg. from JNTUH, Hyderabad, India, the M.Tech degree in Digital Systems and Computer Electronics from JNTUH, Hyderabad, He Presented more than 7 International/Natio-technical papers His area of interest includes. Microwaves and Low Power Design.

Challa Madana Gopal Received the B.Tech. Degree in Electronics and Communication Engineering from J.N.T.U.A, Ananthapuramu, India and persuing M.Tech degree in VLSI System Design from A.V.R & S.V.R College of Engineering and Technology, Nandyal, Andhra Pradesh, India.

M. Mahaboob Basha received the B.Tech degree in Electronics and Communication Engineering from JNTUH, Hyderabad, India, the M.Tech degree in Communication and Signal Processing from SKU, Anantapuramu, India and pursuing Ph.D. in Low Power VLSI Design from JNTUA, Anantapuramu, India. He presented more than 10 International/National technical papers His area of interest includes Signal Processing and Low Power Design