SIMULATION AND ANALYSIS OF NOVEL CASCADED Z SOURCE INVERTER

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ABSTRACT

Multilevel Inverter (MLI) has been recognized as an attractive topology for high voltage conversion. As the number of levels increases, the synthesized staircase output waveform has more steps, approaching the desired sinusoidal waveform but the main drawback of MLI is its output voltage amplitude is limited to DC sources voltage summation. To overcome this limitation five-level cascaded multilevel inverter based Z-source inverter has been proposed. This paper presents the output voltage amplitude can be boosted with Z network shoot-through state control. In this paper Z source inverter is cascaded with new multi-level inverter topology was introduced. The topology has reduced number of switches when compared with conventional multi-level inverter. The performance of Z source MLI have been analyzed and simulation results are presented using MATLAB/SIMULINK

KEYWORDS: *Multilevel Inverter, Z source Converter, THD.*

I. INTRODUCTION

Multilevel inverter is an effective and practical solution for increasing power demand and reducing harmonics of AC waveforms. Function of a multilevel inverter is to synthesize a desired voltage wave shape from several levels of DC voltages. As the number of levels increase, the synthesized staircase output waveform has more steps, approaching the desired sinusoidal waveform. They are of special interest in the distributed energy sources area because several batteries, fuel cell and solar cell can be connected through multilevel inverter to feed a load [1].

The principal function of multilevel inverters is to synthesize a desired ac voltage from several separate dc sources, which may be obtained from batteries, fuel cells, or solar cells [2]. Multilevel inverter obtains a desired output voltage from several levels of input DC voltage sources. With an increasing number of DC voltage sources, the inverter voltage output waveform level increases.[3] [4]

The multilevel inverters have more advantages which include lower semiconductor voltage stress, better harmonic performance, low Electro Magnetic Interference (EMI) and lower switching losses. Despite these advantages, multilevel inverters output voltage amplitude is limited to DC sources voltage summation. An intermediate DC to DC converter is required for the boost or buck operation of MLI output voltage. Occurring of short circuit can destroy multilevel inverters. To solve these problems, multilevel inverter based Z-source inverter is proposed in this paper and similarly a new multilevel inverter was introduced. The Z-source inverter utilizes Z impedance network between the DC source and inverter circuitry to achieve buck-boost operation. The Z-Source inverter utilizes shoot-through state to boost the input dc voltage of inverter switches when both switches in the same phase leg are on. The Z-Source inverters with respect to traditional inverters are lower costs, reliable, lower complexity and higher efficiency. This paper deals with the analysis, when the new multi-level inverter topology is cascaded with Z source DC – DC converter [4][5]. The new topology has reduced

switches than conventional multilevel inverter. Performance parameters have been analyzed for cascaded Z-Source new MLI topology. The performance of Z-Source Multilevel inverter is compared with the Z source new multilevel inverter topology. Simulation of the circuit configurations have been performed in MATLAB/SIMULINK

II.   NEW MULTILEVEL INVERTER TOPOLOGY

In order to reduce the overall number of switching devices in conventional multilevel inverter topologies, a new topology has been proposed. The circuit configuration of the new 5 -level inverter is shown in Fig.1. It has four main switches in H-bridge configuration Q1~Q4, and four auxiliary switches Q5, Q6, Q7 and Q8. The number of dc sources (*two*) is kept unchanged as in similar 5-level conventional cascaded H-bridge multilevel inverter. Like other conventional multilevel inverter topologies, the proposed topology can be extended to any required number of levels. The inverter output voltage, load current, and gating signals are shown in Fig.2. The inverter can operate in three different modes according to the polarity of the load voltage and current. As these modes will be repeated irrespective of the number of the inverter levels, and for the sake of simplicity, the modes of operation will be illustrated for 5-level inverter, these modes
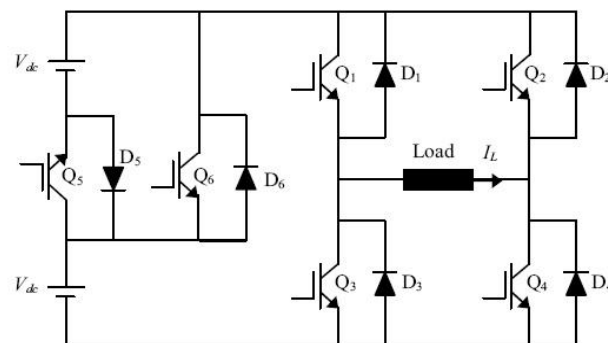

Fig 1 : The 5-level inverter of the new topology

Powering Mode

This occurs when both the load current and voltage have the same polarity. In the positive half cycle, when the output voltage is *Vdc*, the current pass comprises; the lower supply, D6, Q1, load, Q4, and back to the lower supply. When the output voltage is *2Vdc*, current pass is; the lower source, Q5, the upper source, Q1, load, Q4, and back to the lower source. In the negative half cycle, Q1 and Q4 are replaced by Q2 and Q3 respectively.

Free-Wheeling Mode

Free-wheeling modes exist when one of the main witches is turned-off while the load current needs to continue its pass due to load inductance. This is achieved with the help of the anti-parallel diodes of the switches, and the load circuit is disconnected from the source terminals. In this mode, the positive half cycle current pass comprises; Q1, load, and D2 or Q4, load, and D3, while in the negative half cycle the current pass includes Q3, load, and D4 or Q2, load, and D1.
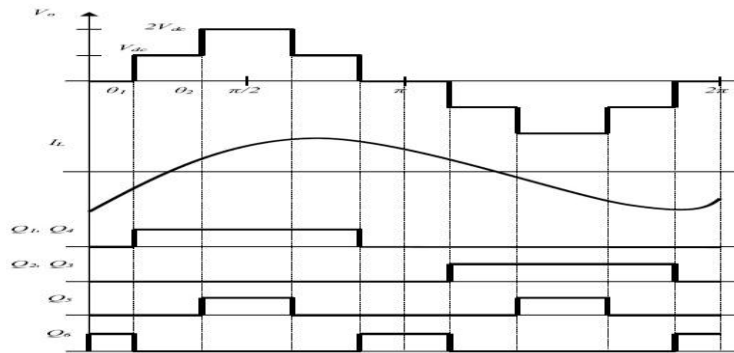
Fig 2 : Waveforms of the proposed 5-level inverter

Regenerating Mode

In this mode, part of the energy stored in the load inductance is returned back to the source. This happens during the intervals when the load current is negative during the positive half cycle and vice-versa, where the output voltage is zero. The positive current pass comprises; load, D2, Q6, the lower source, and D3, while the negative current pass comprises; load, D1, Q6, the lower source, and D4.

A generalized circuit configuration of the new topology is shown in Fig.5. The proposed topology has the advantage of the reduced number of power switching devices, but on the expense of the high rating of the main four switches. Therefore, it is recommended for medium power applications.
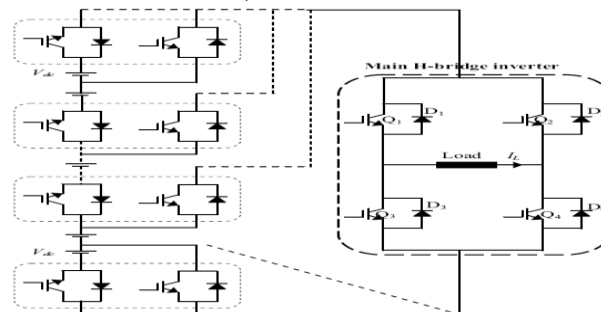

Fig 3 : Generalized multilevel inverter configuration of the new topology

The percentage reduction in the number of power switches compared to conventional H-bridge multilevel inverter is shown in Table 1 and the order of switching sequence of the switches as shown in table 2
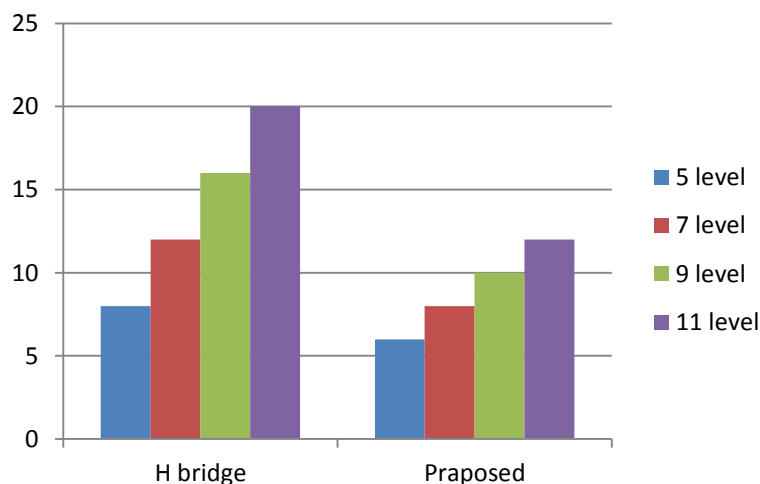
Table 1: Percentage reduction in switching devices

	5 level	7 level	9 level	11 level
H bridge	8	12	16	20
Proposed	6	8	10	12

Table 2: Switching of proposed MLI

S.No	Conducting Switches	Amplitude Of the Output Voltage
1	Q1, Q4,, Q6, Q5	2 Vdc
2	Q1 , Q4, Q6	Vdc
3	NIL	0
4	Q2, Q3,, Q6, Q5	-Vdc
5	Q2 , Q3, Q6	-2 Vdc

III. MATHEMATICAL METHOD OF SWITCHING

In order to verify the ability of the proposed multilevel inverter topology to synthesize an output voltage with a desired amplitude and better harmonic spectrum, programmed PWM technique is applied to determine the required switching angles. It has been proved that in order to control the fundamental output voltage and eliminate n harmonics, therefore n+1 equation is needed..

The Fourier series expansion of the output voltage waveform using fundamental frequency switching scheme shown in Fig.2 is as follows:

$$V\,(\omega t) = (\frac{4VDC}{\pi})\,\Sigma\,[\cos\,(n\,\theta_1)+\cos\,(n\,\theta_2)+\ldots+\cos\,(n\,\theta_s)]\,\sin\,(n\omega t) \quad \text{where n = 1, 3, 5, 7,} \qquad (1)$$

The conducting angles $\theta_1, \theta_2, \theta_3, \ldots, \theta_s$ can be chosen such that the voltage total harmonic distortion is a minimum. Normally, these angles are chosen so as to cancel the predominant lower frequency harmonics [6], [7].

Where $m = V1/(4Vdc/\pi)$, and the modulation index ma is given by ma=m/s, where $0 \leq m_a \leq 1$

One approach to solving the set of nonlinear transcendental equations (2), is to use an iterative method such as the Newton-Raphson method [8]. In contrast to iterative methods, the approach here is based on solving polynomial equations using the theory of resultants which produces all possible solutions [9]. The set of nonlinear transcendental equations can be solved by an iterative method such as the Newton–Raphson method.
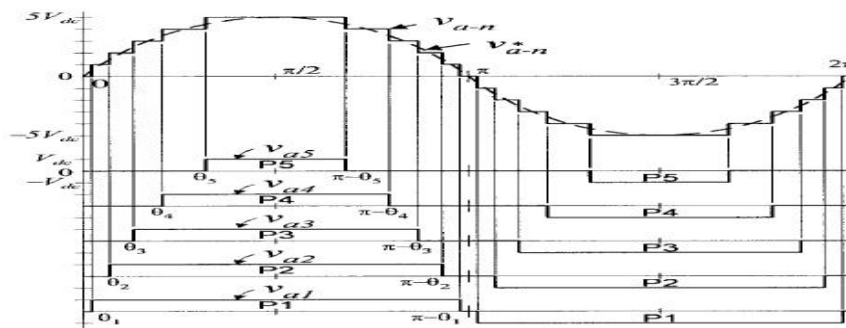

Fig 4: Waveforms and switching method of the 11-level cascade inverter

IV. CASCADED Z-SOURCE MULTILEVEL INVERTER

Multilevel inverter synthesizes a desired output voltage from several levels of input DC voltage sources. With an increasing number of dc voltage sources, the inverter voltage output waveform approaches a nearly sinusoidal waveform[10].As compared to traditional two level inverters, the

multilevel inverters have more advantages which include lower semiconductor voltage stress, better harmonic performance, low electromagnetic interference (EMI) and lower switching losses . Despite these advantages, multilevel inverters output voltage amplitude is limit to DC sources voltage summation[10]. For the boost or buck of multilevel output voltage the other converters as a DC/DC converter is needed. Occurring of short circuit can destroy multilevel inverters; therefore multilevel inverters need to operate with dead-time protection. To solve these problems, multilevel inverter based Z-source inverter is proposed. The Z-source inverter utilizes Z impedance network between the DC source and inverter circuitry to achieve boost operation[11][12]. The Z-Source inverter, unlike traditional inverters can utilize shoot-through states to boost the input dc voltage of inverter switches when both switches in the same phase leg are on. The Z-Source inverters with respect to traditional inverters are lower costs, reliable, lower complexity and higher efficiency. In addition to cascade inverter advantages, proposed topology employs Z-source inverter advantages such as shoot through capability and ability of voltage boosting. The output voltage of proposed inverter can be controlled using modulation index and shoot through state [13].
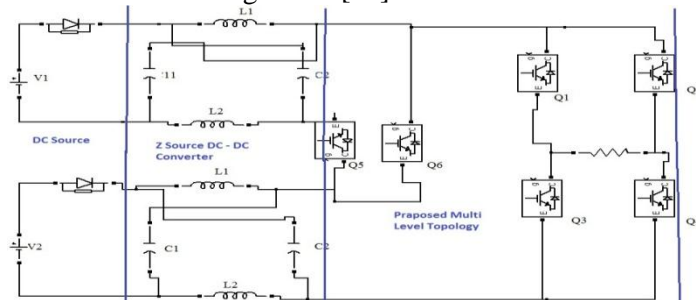

Fig.5 Circuit diagram of 5-Level cascaded Z-Source MLI

In Figure 5, a two-port network that consists of an inductors (L1, L2) and capacitors (C1, C2) and connected in X shape is employed to provide an impedance source (Z-Source) coupling the inverter to the dc source. The switches used in this inverter are IGBT

4.1 Operating Principle

The unique feature of the Z-source inverter is that the output ac voltage can be any value between zero and infinity. That is, the Z-source inverter is a buck–boost inverter that has a wide range of obtainable voltage. The single-phase Z-Source inverter bridge has seven permissible switching states. The single phase Z-source inverter bridge has three extra zero state (or vector) when the load terminals are shorted through both the upper and lower devices of any one phase leg (i.e., both devices are gated on) or any two phase legs. This zero state (vector) is called as the shoot-through zero state (or vector). The Z-source network makes the shoot-through zero state possible. This shoot-through zero state provides the unique buck-boost feature to the inverter. Inductors L1 and L2 have the same values. L1=L2=L and VL1=VL2=VL Capacitors C1 and C2 have the same values. C1=C2=C and VC1=VC2=VC Z-Source network is a symmetrical network. The operating states of the Z-Source inverter are: Shoot through zero state and Non Shoot through zero state

V. SIMULATION RESULTS

Simulation of double input Z-source dc-dc converter fed dc motor was performed using MATLAB SIMULINK to confirm above analysis. The block diagram of the proposed Cascaded Z source inverter with reduced switches as shown in fig 6.
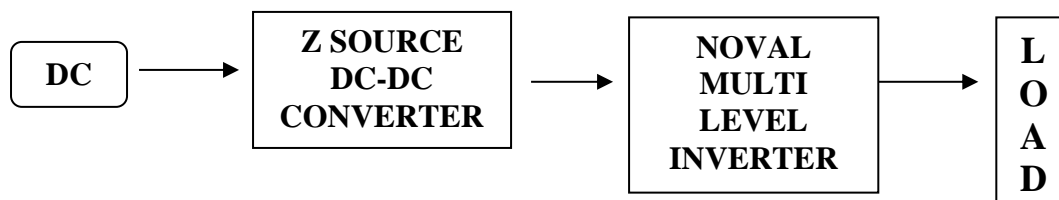

Fig 6 : Block Diagram of Cascaded Z source MLI

A new strategy with reduced number of switches is employed[14]. For cascaded H bridge 5 level inverter requires 8 switches to get five level output voltage and with the proposed topology requires 6 switches as shown in the fig 7.The new topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter. Fig 7 shows the Simulink model for proposed Five level Inverter topology The generated output pulses from the pulse generator as shown in the Fig. 8 and those pulses generated are to drive the devices in to ON for a five level inverter of the proposed topology and five level output voltage is presented in fig 9
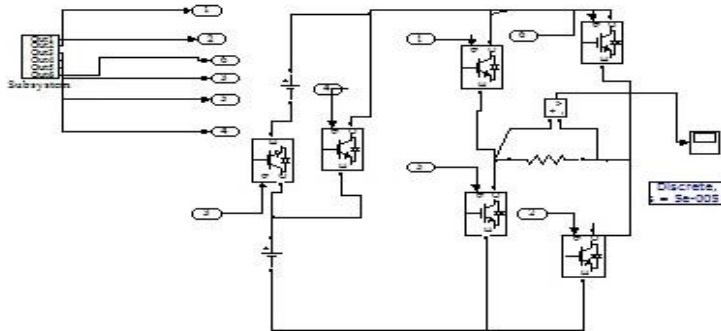

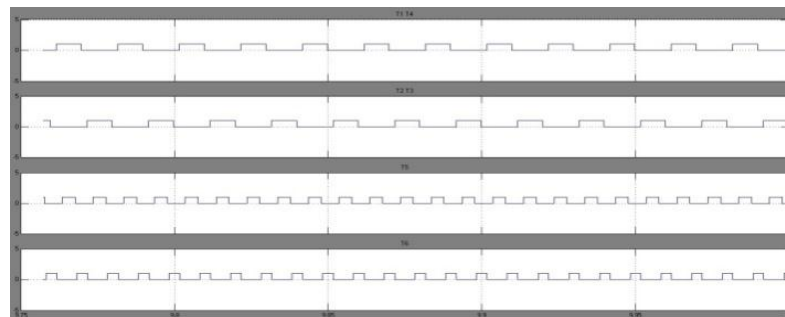**Fig.7** Simulink model for proposed Five Level Inverter

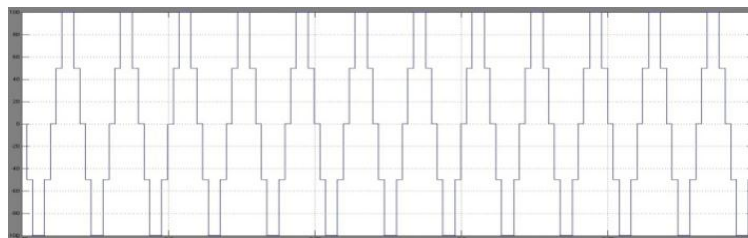**Fig.8** Generated Gate pulse for Five Level Inverter

Fig. 9 Five Level Output Voltage

The simulation model for proposed cascaded Z source DC – DC converter as shown in fig 10, the output voltage amplitude can be boosted with Z network and the corresponding boosted output voltage is as shown in fig 11
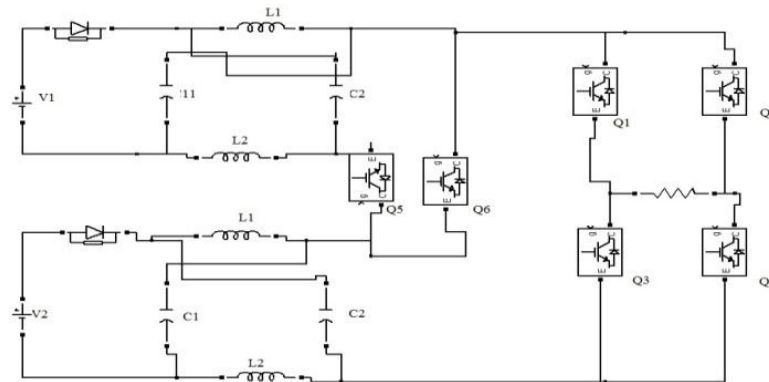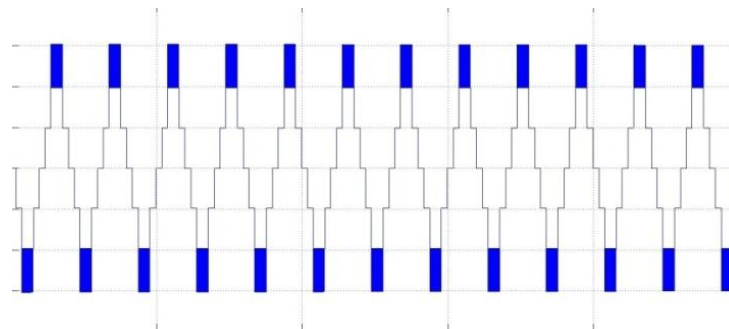
Fig. 10 Cascaded Z source MLI model

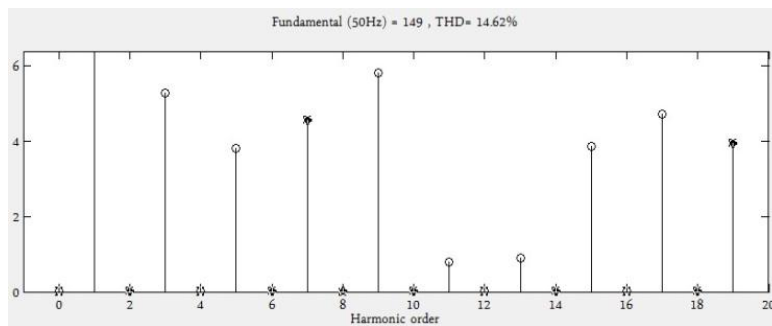**Fig. 11** Proposed Five level Output Voltage

Fig. 12 FFT analysis

VI. CONCLUSION

A new family of multilevel inverters has been presented and built in MATLAB-Simulink. It has the advantage of its reduced number of switching switches compared to conventional similar inverters. However the output voltage amplitude can be boosted with Z network and the THD value is reduced to 8.18 as shown in the fig 11. those schemes confirmed by simulation results. This proposed prototype can be extended to m-level inverter. Other PWM methods and techniques are also expected to be successively applied to the proposed topology [15]. The simulation results and experimental results show that the algorithm can be effectively used to eliminate specific higher order harmonics of the new topology and results in a dramatic decrease in the output voltage THD.

VII. FUTURE WORK
- The proposed topology focused on the Sine PWM method and this method can be applied to different voltage levels, other modulation techniques and similarly other PWM techniques can be applied.
- Also if the comparison is done from an economical point of view, it gives a better picture in construction in reduction in circuit complexity, requiring a less number of power switches in industrial application

- Another interesting topic that can be studied in the modeling and control of multilevel inverters in FACTS devices application, HVDC transmission lines and large wind turbine applications

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