IMPLEMENTATION AND SIMULATION OF CMOS TWO STAGE OPERATIONAL AMPLIFIER

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ABSTRACT

Operational amplifiers are an integral part of many analog and mixed signal systems. As the demand for mixed mode integrated circuits increases, the design of analog circuits such as operational amplifiers in CMOS technology becomes more critical. Operational amplifiers with moderate DC gain, high output swing and reasonable open loop Gain Band Width product (GBW) are usually implemented with two stage structures. This paper presents a two stage CMOS operational amplifiers, which has been designed, exhibits a Unity Gain Frequency (UGF) of 20MHz and a gain of 42dB with 50 degree phase margin. To increase the gain and phase margin new technique has been proposed. Simulation results are gain of 48dB, unity gain frequency of 40MHz, Phase margin of 89 degree. Design has been carried out in Cadence tool.

KEYWORDS: *Two stage OTA, GBW, Mixed signal design.*

I. INTRODUCTION

Op-amps are among the most widely used electronic devices today, being used in a vast array of consumer, industrial, and scientific devices. In many applications [1,2] of operational amplifiers, the gain of a single-stage amplifier is not adequate. Operational amplifier architectures that use two or more gain stages [3] are widely used when higher gains are needed. This results in introduction of additional phase shift and compensation of these structures is required to maintain acceptable magnitude response or time-domain response of feedback circuits that use the multiple-stage architectures. Op-amps are available in many topologies, a two stage op-amp is one such of its kind, which are used when high input impedance and low output impedance is required.

CMOS operational amplifiers can be used efficiently for practical consequences for example designing of a switched capacitor filters, analog to digital converters [4] etc. Figure 1 shows a basic two-stage CMOS op-amp configuration. M5 provides biasing for the entire operational amplifier. M1 and M2 form a differential pair and thus the input of the first gain stage of the op amp. The M5 and M7 supplies the differential pair with bias current *IB*1. The input differential pair is actively loaded with the current mirror formed by M3 and M4. Node 1 forms the output of the first stage of the op amp. The second stage consists of M6 which is a common-source amplifier actively loaded with the transistor M7. The transistor M7 does not provide biasing for M6, indeed M6 is biased from the gate side.

In this paper design procedure with design steps explained in the next section. After this simulation results are provided.

II. DESIGN PROCEDURE

Before actually beginning with the designing part, let us discuss some important relationships describing performance of an op-amp.

Slew rate, $SR = \frac{I_5}{C_c}$ (1)

First-stage gain, $A_{v1} = \frac{-g_{m1}}{g_{ds2} + g_{ds4}} = \frac{-2g_{m1}}{I_5(\lambda_2+\lambda_4)}$ (2)

Second-stage gain,

$$A_{v2} = \frac{-g_{m6}}{g_{ds6} + g_{ds7}} = \frac{-g_{m6}}{I_6(\lambda_6+\lambda_7)} \quad (3)$$

Gain bandwidth, $GB = \frac{g_{m1}}{C_c}$ (4)

Output pole, $p_2 = \frac{-g_{m1}}{C_L}$ (5)

RHP zero, $z_1 = \frac{g_{m6}}{C_c}$ (6)

Positive CMR,

$$V_{in}(max) = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - [\, V_{T3}(max) + V_{T1}(min) \,] \quad (7)$$

Negative CMR,

$$V_{in}(min) = V_{SS} - \sqrt{\frac{I_5}{\beta_1}} + V_{T1}(max) + V_{DS5}(sat) \quad (8)$$

Saturation voltage,

$$V_{DS}(sat) = \sqrt{\frac{2I_{DS}}{\beta}} \quad (9)$$

For the above relationships it is assumed that all the transistors shown in figure 1 are in saturation and that

$$g_{m1} = g_{m2} = g_{mI}, g_{m6} = g_{mII}, g_{ds2} + g_{ds4} = G_I \text{ and } g_{ds6} + g_{ds7} = G_{II} \quad (10)$$

The design procedure [7] in a broader sense involves the following sequence of steps. Firstly selecting a specific topology, secondly determining the DC currents, thirdly calculating the W/L ratios of each transistor, at the end deciding the passive component values used in the circuit. This is clearly classifies in the figure 2.

The design procedure assumes that the DC gain(A_v), unity-gain bandwidth (GB), Input common-mode range[$V_{in}(min)$ and $V_{in}(max)$], Load capacitance(C_L), slew rate(SR), Settling Time(T_s), Output voltage swing[$V_{out}(max)$ and $V_{out}(min)$] and Power dissipation(P_{diss}) are given.

1. The smallest device length that will keep the channel modulation parameter constant and give good matching for current mirrors has been chosen.
2. From the desired phase margin, the minimum value for C_c is chosen ,that is for a 60^0 phase margin. We have used the following relationship. This assumes that $z \geq 10GB$.

$$C_c > 0.22\, C_L$$

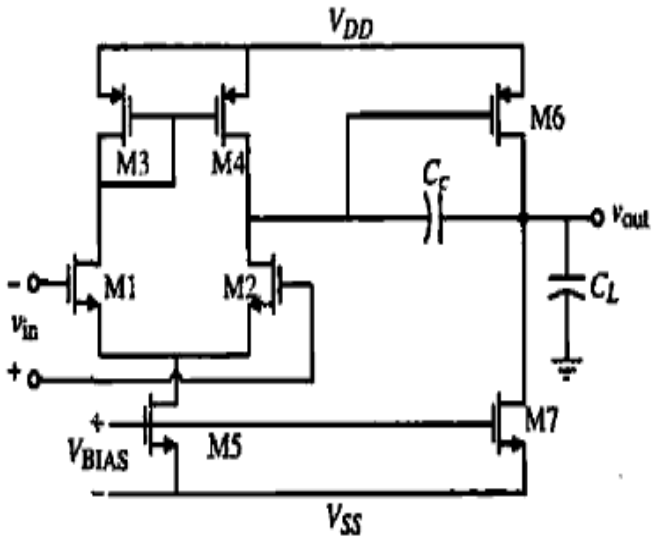

Figure 1: Two Stage Op-Amp

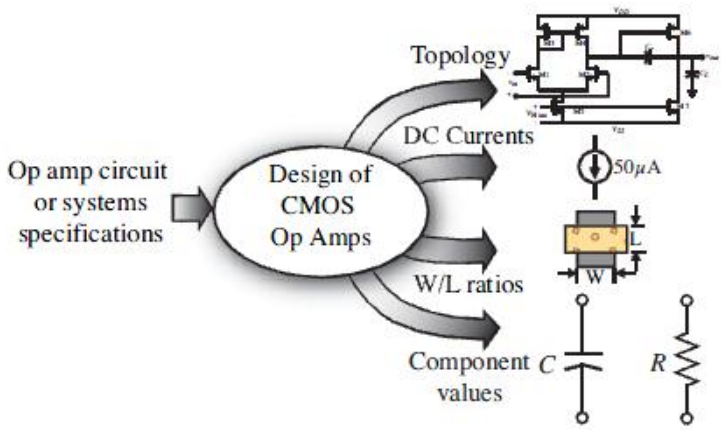

Figure 2: Design procedure of Op-Amp

3. The minimum value for the tail current (I_5) from the largest of the two values is determined.

$$I_5 = SR.C_C$$

I_5 nearly equal to $\frac{10(V_{DD}+|V_{SS}|)}{2T_S}$

4. Design for S_3 from the maximum input voltage specification.

$$S_3 = \frac{2I_3}{K_3^1 V_{DD} - V_{in(max)} - [V_{T3(max)} + V_{T1(min)}]^2} \geq 1$$

5. The pole and zero due to C_{gs3} and C_{gs4} $(=0.67W_{3L3}C_{ox})$ will not be dominant by assuming pole p_3 to be greater than 10GB.

$$\frac{g_{m3}}{2C_{gs3}} > 10GB$$

6. Design for $S_1(S_2)$ to achieve desired GB.

$$g_{m1} = GB.C_c \geq S_1 = S_2 = \frac{g_{m2}}{K_2^1 I_5}$$

7. Design for S_5 from the minimum input voltage. First we have calculated $V_{DS5(sat)}$ and then we have find S_5.

$$V_{DS5(sat)} = V_{in(min)} - V_{SS} - \left(\frac{I_5}{\beta_1}\right)^{\frac{1}{2}} - V_{T1(max)} \geq 100mV$$

$$S_5 = \frac{2I_5}{K_5^1 [V_{DD(sat)}]^2}$$

8. Find S_6 and I_6 by letting the second pole(p_2) be equal to 2.2 times GB.

$$g_{m6} = 2.2\, g_{m2} \left(\frac{C_L}{C_c}\right)$$

Let $V_{SG4} = V_{SG6}$, which gives $S_6 = S_4 \left(\frac{g_{m6}}{g_{m4}}\right)$

Knowing g_{m6} and S_6 allows us to solve for I_6 as $I_6 = \frac{g_{m6}^2}{2K_6^1 S_6}$

9. Alternately, I_6 can be calculated by solving for S_6 using

$$S_6 = \frac{g_{m6}}{K_6^1 V_{DS6(sat)}}$$

And then using the previous relationship to find I_6. The proper mirror between M_3 and M_4 is no longer guaranteed.

10. Design S_7 to achieve the desired current ratios between I_5 and I_6.

$$S_7 = \left(\frac{I_5}{I_6}\right) S_6$$

11. Check gain and power dissipation specifications.

12.By simulating the circuit we have seen that all the specifications are met.

III. SIMULATION RESULTS

In AC analysis gain band width product, Gain and Phase margin are determined. Both Gain and Phase margin are calculated using DC operating point and AC analysis. Figure 3 is the basic structure of two

stage operational amplifier. This architecture is designed at 3.5V power supply. All transistors aspect ratio (W/L) calculated according to biasing dc current.

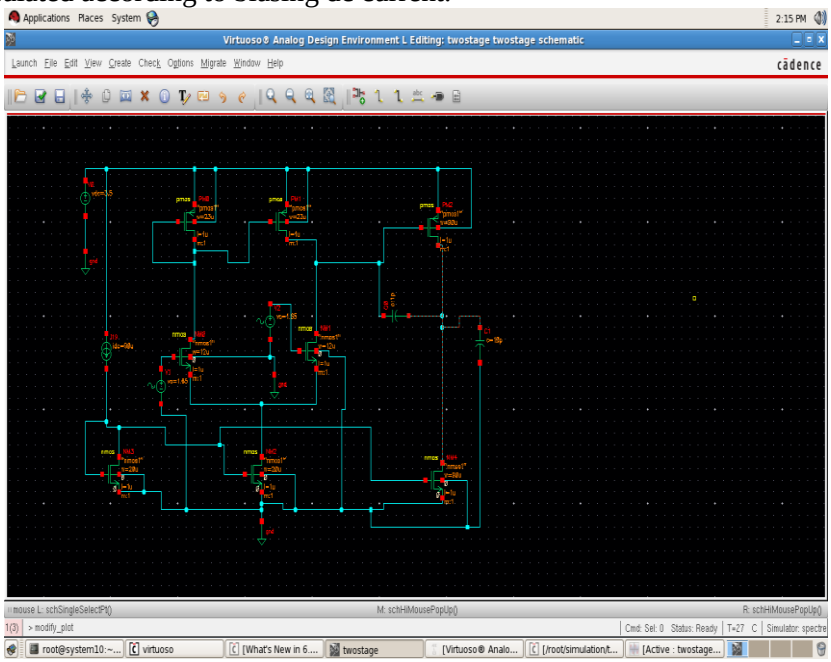

Figure 3: Basic two stage opamp.

Figure 4 shows the simulated AC Analysis of Basic two stage operational amplifier. Gain of the architecture is 42dB, unity gain frequency of 20MHz, Gain margin of 15dB and Phase margin of 49 degree.

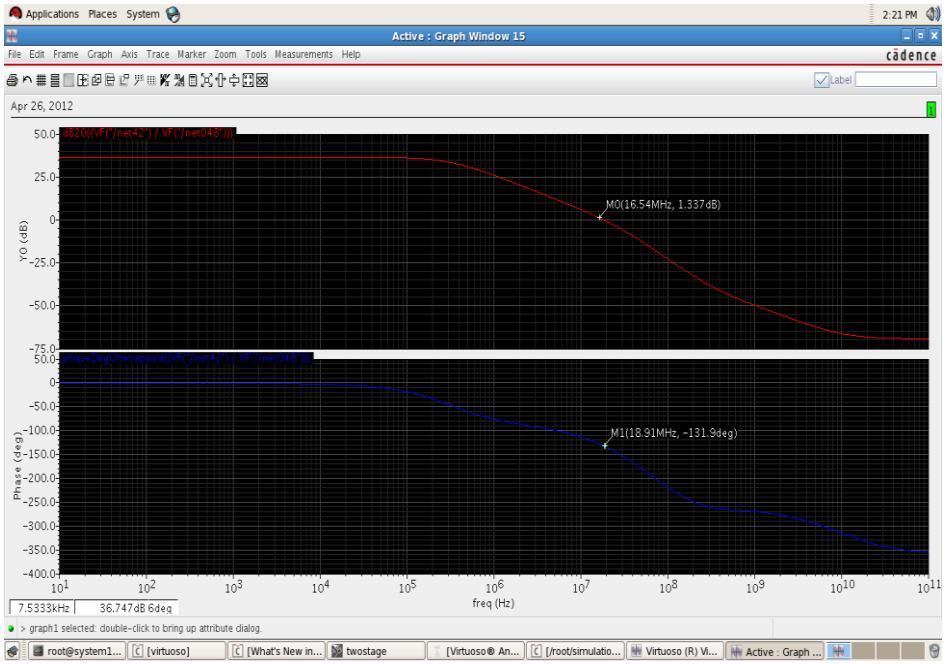

Figure4: Output of AC Analysis

To improve the gain and phase margin new technique is introduced in Figure 5.

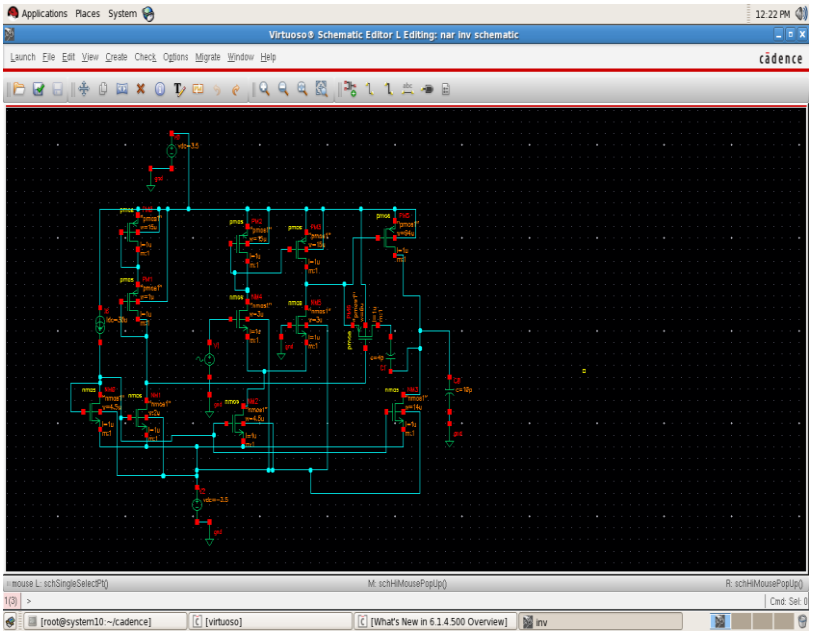

Figure5: Two stage modified OTA

This architectures simulated results are gain is 48db, unity gain frequency is 40MHz, gain margin of 46db and phase margin of 89.8 degree.

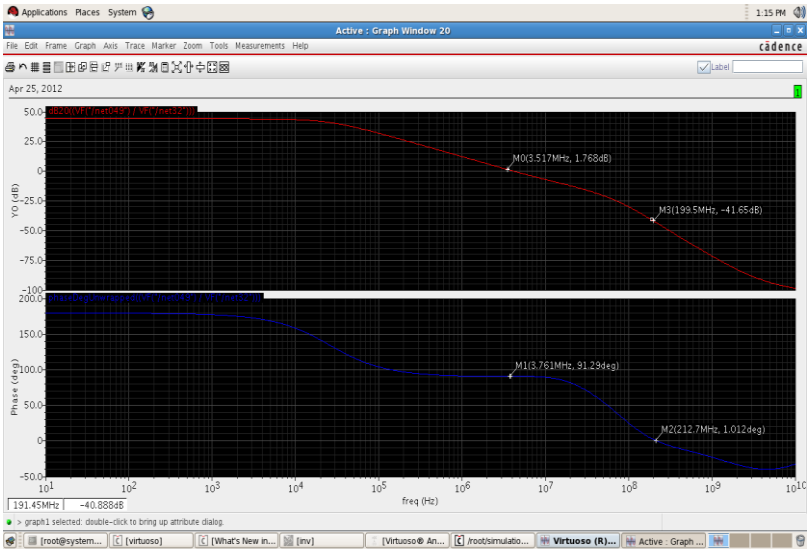

Figure 6: Output of AC Analysis

IV. CONCLUSION

Two stage operational amplifier is designed and simulated in 0.18um technology. Power supply of the architecture is 3.5V. Gain of the architecture is 42dB, unity gain frequency of 20MHz, Gain margin of 15dB and Phase margin of 49 degree. Gain and phase margin is improved in new architecture. The simulated results of the modified architecture gain of 48db, unity gain frequency of 40MHz, gain margin of 46db and phase margin of 89.8 degree.

V. FUTURE WORK

Design of accurate A/D converters and filters are challenging task for present applications. So this work can be extended further for communication applications.

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