LOW TRANSITION TEST PATTERN GENERATOR ARCHITECTURE FOR MIXED MODE BUILT-IN-SELF-TEST (BIST)

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ABSTRACT

In Built-In Self-Test (BIST), test patterns are generated and applied to the circuit-under-test (CUT) by on-chip hardware; minimizing hardware overhead is a major concern of BIST implementation. In pseudorandom BIST architectures, the test patterns are generated in random nature by Linear Feedback Shift Registers (LFSR). Conventional LFSRs normally requires more number of test patterns for testing the architectures which need long test time. Approach: This paper presents a novel test pattern generation technique called Low-Transition Generalized Linear Feedback Shift Register (LT-GLFSR) with Bipartite (half fixed), Bit-Insertion (either 0 or 1) and its output bits positions are interchanged by swapping techniques (Bit-Swapping). This method introduces Intermediate patterns in between consecutive test vectors generated by GLFSR which is enabled by a non overlapping clock scheme. This process is performed by finite state machine generate sequence of control signals. LT-GLFSR, are used in a circuit under test to reduce the average and peak power during transitions. LT-GLFSR patterns high degree of randomness and improve the correlation between consecutive patterns. LT-GLFSR does not depend on circuit under test and hence it is used for both BIST and scan-based BIST architectures. Results and Discussions: Simulation results prove that this technique has reduction in power consumption and high fault coverage with minimum number of test patterns. The results also show that it reduces power consumption during test for ISCAS'89 bench mark circuits. Generally LT-GLFSR is called GLFSR with Bipartite Technique. Proposed technique is called as LT-GLFSR with BI and BS.

KEYWORDS: *Low Transition Generalized Linear Feedback Shift Register (LT-GLFSR (Bipartite)), Bipartite Technique, LT-GLFSR (BI and BS), Finite State Machine(FSM), Bit Swapping(BS),Bit Insertion(BI).*

I. INTRODUCTION

Importance of testing in Integrated Circuit is to improve the quality in chip functionality that is applicable for both commercially and privately produced products. The impact of testing affects areas of manufacturing as well as those involved in design. Given this range of design involvement, how to go about best achieving a high level of confidence in IC operation is a major concern. The desire to attain a high quality level must be tempered with the cost and time involved in this process. These two design considerations are at constant odds. It is with both goals in mind (effectiveness and cost/time) that Built-In-Self Test (BIST) has become a major design consideration in Design-For-

Testability (DFT) methods. BIST is beneficial in many ways. First, it can reduce dependency on external Automatic Test Equipment (ATE) because it is large, vendor specific logic, non-scalable and expensive equipment. This aspect impacts the cost/time constraint because the ATE will be utilized less by the current design. The paper is organised into nine sections which are follows as: Section I describes the introduction about testing. Section II eloborates the prior works carried out by the reasearchers in the field of testing of VLSI circuits. Section III describes the proposed work. Materials and methods of the proposed work and their implemenations are discussed in sections IV, Vand VI respectively. Finally the results and their discussions are illustrated in sections VII and VIII.

In addition, BIST provides high speed, in system testing of the Circuit-Under-Test (CUT) [13]. This is crucial to the quality component of testing. that stored pattern BIST, requires high hardware [3] overhead due to memory devices is in need to store pre computed test patterns, pseudorandom BIST, where test patterns are generated by pseudorandom pattern generators such as Linear Feedback Shift Registers (LFSRs) and cellular automata (CA), required very little hardware overhead.

However, achieving high fault coverage for CUTs that contain many random pattern resistant faults (RPRFs) only with (pseudo) random patterns generated by an LFSR or CA often requires unacceptably long test sequences thereby resulting in prohibitively long test time. In general, the dissipation of power of a system in test mode is higher than in normal mode operation. Power increases during testing because of high switching activity [2], parallel testing of nodes, power due to additional load (DFT) and decrease of correlation [4] among patterns. This extra power consumption due to switching transitions (average or peak) can cause problems like instantaneous power surge that leads to damage of circuits (CUT), formation of hot spots, and difficulty in verification.

Solutions that are commonly applied to relieve the extravagant power problem during test include reducing frequency and test scheduling to avoid hot spots. The former disrupts at-speed test philosophy and the latter may significantly increase the time. The aim of BIST is to detect faulty components in a system by means of the test logic that is incorporated in the chip. It has many advantages such as at-speed testing and reduced need of expensive external automatic test equipment (ATE).

In BIST, LFSR is used to generate pseudorandom test patterns which are primary inputs for a combinational circuit or scan chain inputs for a sequential circuit [7]. BIST-based structures are very vulnerable to high-power consumption during test. The main reason is that the random nature of patterns generated by an LFSR significantly reduces the correlation not only among the patterns but also among adjacent bits within each pattern; hence the power dissipation is more in test mode like instantaneous power surge that leads to damage of circuits (CUT), formation of hot spots, and difficulty in verification. Solutions that are commonly applied to relieve the extravagant power problem during test include reducing frequency and test scheduling to avoid hot spots. The former disrupts at-speed test philosophy and the latter may significantly increase the time.

II. PRIOR WORK

GLFSR [11], a combination of LFSR and cellular arrays, that is defined over a higher order Galois field GF (2^{δ}), $\delta>1$. GLFSR's yield a new structure when the feedback polynomial is primitive and when ($\delta>1$) it is termed as MLFSR.

Cellular automata algorithm for test pattern generation was applied [5] in combinational logic circuits. This maximizes the possible fault coverage and minimizes length of the test vector sequences. Also it requires minimum hardware.

A low power/energy BIST architecture based on modified clock scheme test pattern generator was discussed [12], [8] it was discussed that an n bit LFSR is divided into two n/2 bit length LFSRs. The fault coverage and test time were the same as those achieved in conventional BIST scheme.

A dual speed LFSR [16] test pattern for BIST was generated. The architecture comprised of a slow speed and a normal speed LFSR for test pattern generation. Slow speed LFSR was clocked by dual clocked flip-flop, this increased the area overhead than normal speed LFSR.

Effective pattern generator should generate [6] patterns with high degree of randomness and should have efficient area implementation. GLFSR provide a better random distribution of the patterns and potentially lesser dependencies at the output. EGLFSR is known to be an enhanced GLFSR, which comprises of few more XOR gate in a test pattern generator than LFSR which achieves a better performance.

Low power test patterns were generated [10] for BIST applications. It exploited low transition LFSR which was a combination of conventional LFSR and insertion of intermediate patterns (bipartite and random insertion technique) between sequences of patterns generated by LFSR that was implemented by modified clock scheme.

A low transition generalized [14] LFSR based test patterns are generated for BIST architecture. LT-GLFSR consists of GLFSR with bipartite technique. In Bipartitite technique (half fixed), among the available test patterns a portion of the bits are changed and remaining bits are unchanged inorder to obtain new vectors in between two consecutive patterns generated by GLFSR. Then multiplexer circuits are used to select either swapped output of GLFSR(bipartite) or output of bit insertion circuit [15] In this method,generated patterns has greater degree of randomness and improves corelation between consecutive patterns but it has slightly high transitions in sequence of patterns generated. Generally, power consumption is with respect to number of transition between consecutive patterns, by introducing the enable signals to activate the GLFSR, to reduce the number of transitions.In proposed method, LT-GLFSR can activated by four non-overlaping enable signals.This enable signal is to activate test pattern generator partly and remaining in idle when period of test pattern generation.

III. PROPOSED WORK

This paper presents a new test pattern generator for low- power BIST (LT-GLFSR), which is employed for combinational and sequential architectures. The proposed design composed of GLFSR and intermediate patterns insertion technique (Bipartite, Bit Insertion and Bit Swapping techniques) that can be implemented by modified clock scheme and its control signals (codes) generated by finite state machine (FSM). FSM generates sequence of codes (en1en2sel1sel2) which are given in terms of 1011, 0010, 0111, and 0001. Enable signals (en1en2) are used to enable part of the GLFSR (bipartite) and selector signals (sel1sel2) are used to select either GLFSR output (bipartite and swapped output) or bit insertion circuit output. Intermediate patterns are in terms of GLFSR output and Bit-Insertion technique output. Swapped output is obtained by interchanging the position of output of the adjacent cells of the GLFSR.The proposed technique improves the correlation in two dimensions: 1) the vertical dimension between consecutive test patterns (Hamming Distance) and 2) the horizontal dimension between adjacent bits of a pattern sent to a scan chain. It results in reducing the switching activity which in turn results in reducing the average and peak power consumption [13]. The GLFSR [12] structure is modified in such a way that automatically inserts three intermediate patterns between its original pairs generated. The intermediate patterns are carefully chosen using bipartite and bit insertion techniques [10] and impose minimal time to achieve desired fault coverage. Insertion of intermediate pattern is achieved based on non overlapping clock scheme [12]. The Galois field (GF) of GLFSR (3, 4) [17]) is divided into two parts, it is enabled by two different clock schemes. The randomness of the patterns generated by LT-GLFSR has been shown to be better than LFSR and GLFSR. The favourable features of LT-GLFSR in terms of performance, fault coverage and power consumption are verified using the ISCAS benchmarks circuits.

IV. MATERIALS AND METHODS

GLFSR Frame Work: The structure of GLFSR is illustrated in Fig.1. The circuit under test (CUT) is assumed to have δ outputs which form the inputs to that GLFSR to be used as the signature analyzer [11], [9]. The inputs and outputs are considered δ bit binary numbers, interpreted as elements over GF (2^{δ}).The GLFSR, designed over GF (2^{δ}), has all its elements belonging to GF (2^{δ}). Multipliers, adders, and storage elements are designed using conventional binary elements. The feedback polynomial is represented in equation. 1 as

$$\Phi(x) = x^m + \Phi_{m-1}x^{m-1} + \cdots + \Phi_1 x + \Phi_0 \text{—}(1)$$

The GLFSR has m stages, D_0, D_1...D_{m-1} each stage has δ storage cells. Each shifts δ bits from one stage to the next. The feedback from the $D_{m-1}{}^{th}$ stage consists of δ bits and is sent to all the stages. The coefficients of the polynomial Φ_i are over GF (2^{δ}) and define the feedback connections.

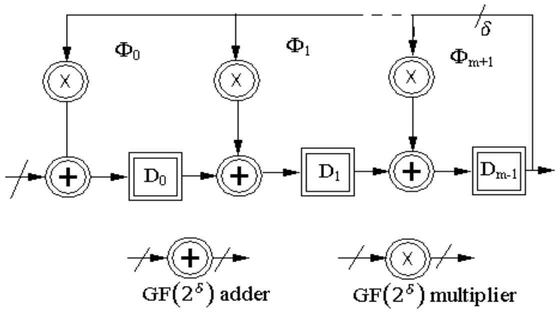


Fig. 1 The generalized GLFSR

The GLFSR when used to generate patterns for circuit under test of n inputs can have m stages, each element belonging to GF (2^δ) where ($m \times \delta$) is equal to n. A non zero seed is loaded into the GLFSR and is clocked automatically to generate the test patterns. In this paper GLFSR with (δ>1) and (m >1) are used, where all possible $2^{m\delta}$ test patterns are generated. The feedback polynomial is a primitive polynomial of degree m over GF (2^δ). The polynomial from [17] is described as in equation. 2:

$$\Phi(\mathrm{x}) = \left(x + \beta^{2^{\delta_0}}\right)\left(x + \beta^{2^{\delta_1}}\right)\ldots\left(x + \beta^{2^{\delta m-1}}\right) \qquad (2)$$

Where β is the primitive element of GF ($2^{m\times\delta}$) and Constructing a primitive polynomial of degree m over GF(2^δ) using(equation.2) coefficients Φ_0, Φ_1.., Φ_{m-1} as powers of β, the primitive element of GF($2^{m\times\delta}$). Let δ =3,m = 4,(GF(3,4))The primitive polynomial GF(2^{12}) and GF(2^3) are denoted by β and α respectively in equation. 3.

$$\Phi(x) = (x+\beta)(x+\beta^8)(x+\beta^{64})(x+\beta^{512}) \qquad (3)$$

the Expand form of polynomial is given in equation. 4

$$\Phi(x) = (x^4 + \beta^{1755}x^3 + \beta^{2340}x^2 + \beta^{585}) \qquad (4)$$

Solving the roots α of primitive polynomial p(x)

$$p(x) = x^3 + x + 1 \qquad (5)$$

primitive polynomial of GF (2^3), in GF (2^{12}), β^{1755} becomes an element which corresponds to a primitive element of GF (2^3)' α. Substituting the corresponding values, the feedback polynomial is as in equation.6

$$\Phi(x) = x^4 + \alpha x^3 + \alpha^6 x^2 + \alpha^5 \qquad (6)$$

The element α, α^5 and α^6 are represented as x, x^5 and x^6 respectively in the polynomial form. The four Storage element of the GLFSR are represented as $D_I = a_2x^2 + a_1x + a_0$ $D_{II} = a_5x^2 + a_4x + a_3$, $D_{III} = a_8x^2 + a_7x + a_6$ and $D_{IV} = a_{11}x^2 + a_{10}x + a_9$ respectively. Each storage element has δ storage cells. Storage elements are D_I (D_0,D_1 & D_2),D_{II} (D_3,D_4 & D_5),D_{III}(D_6,D_7 & D_8) and D_{IV} (D_9,D_{10} & D_{11}).

At each cycle, the values that are to be fed back into the storage elements are given by polynomials

$$(a_{11}x^2 + a_{10}x + a_9)\Phi_0$$
$$(a_{11}x^2 + a_{10}x + a_9)\Phi_1 + a_2x^2 + a_1x + a_0$$
$$(a_{11}x^2 + a_{10}x + a_9)\Phi_2 + a_5x^2 + a_4x + a_3$$
$$(a_{11}x^2 + a_{10}x + a_9)\Phi_3 + a_8x^2 + a_7x + a_6$$

with the above explanations the generalize GLFSR in Fig.1 is applied for GLFSR (3, 4) defined over GF (2^3) and its structure is given in Fig.2.

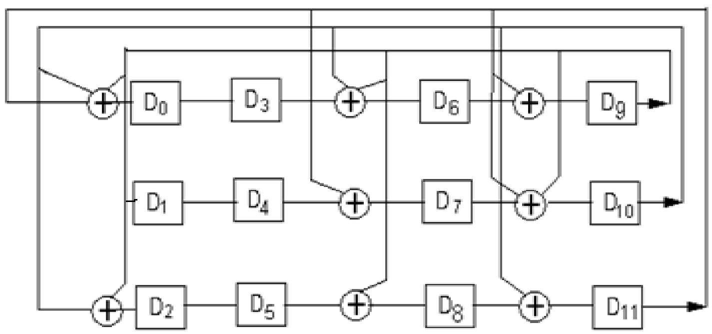


Fig. 2 Structure of GLFSR (3, 4)

Table 1 shows the first 15 states of the GLFSR (3, 4) with the initial seed “1111, 1111, 1111”, and the GLFSR (1, 12), which is a 12 stages LFSR as a comparison.

Table 1. First 15 states of the GLFSR and LFSR

S.No.	GLFSR(3,4)	LFSR(n=12)
1	1111,1111,1111	1111,1111,1111
2	1101,1110,0010	0111,1111,1111
3	1011,1001,1101	0011,1111,1111
4	0111,0100,1111	0001,1111,1111
5	1100,1111,0100	1000,1111,1111
6	1111,1011,0100	0100,0111,1111
7	1111,1101,1100	0010,0011,1111
8	1111,1101,0001	1001,0001,1111
9	1001,1110,1100	0100,1000,1111
10	1111,0001,0111	1010,0100,0111
11	1101,1111,1111	0101,0010,0011
12	1101,1010,0010	1010,1001,0001
13	1011,1001,0101	0101,0100,1000
14	0111,0100,1110	1010,1010,0100
15	0100,1110,0010	0101,0101,0010
16	1010,1011,1101	1010,1010,1001

V. BIPARTITE (HALF-FIXED), BIT INSERTION AND BIT SWAPPING TECHNIQUE (INTERMEDIATE PATTERNS INSERTION TECHNIQUE)

The implementation of a GLFSR is to improve design features, such as testing power. However, such a modification may change the order of patterns or insert new pattern that affect the overall randomness. Intermediate bit patterns between T^i and T^{i+1} of GLFSR are introduced by bipartite and bit insertion [10] technique. Two cells in an each field of the GLFSR are considered to be adjacent without intervening XOR gate.

5.1. Bipartite (half fixed) Technique

The maximum number of transitions is n when $T^{i\ \mathrm{and}}$ T^{i+1} are complements of each other. One strategy, used [19] to reduce number of transitions to maximum of n/2, is to insert a pattern T^{i1}, half of which is identical to T^i and T^{i+1}. This Bipartite (half-fixed) strategy is shown symbolically in Fig. 3a.

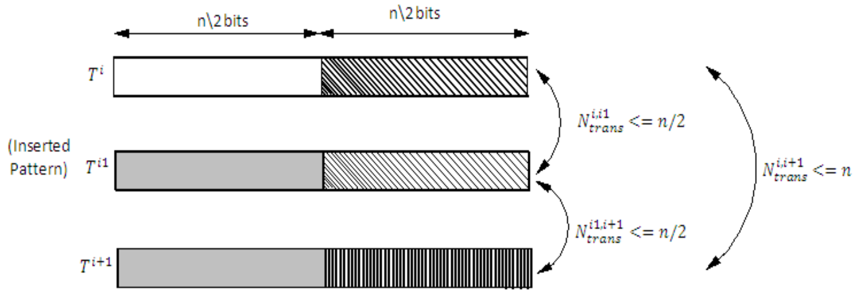


Fig. 3a Patterns Insertion based on Bipartite Strategy

5.2. Bit Insertion Technique (0 or 1)

Bit Insertion Technique (either 0 or 1) is called randomly insert a value in positions,

where $t^i_j \neq t^{i+1}_j$, Briefly,

$$t^{i1}_j = \begin{cases} t^{i1}_j \ if \ t^i_j = t^{i+1}_j. \\ I \quad if \ t^i_j \neq t^{i+1}_j. \end{cases} \qquad (7)$$

Bit insertion technique symbolically represented as shown in Fig.3b. The cells (indicated b) show those bit positions where $t^i_j \neq t^{i+1}_j$

A random bit (shown as I in T^{i1}) is inserted, if the corresponding bits in T^i and T^{i+1} are not equal (0 & 1) and is shown in equation. Note that, inserted bits are uniformly distributed over the length of the test vector.

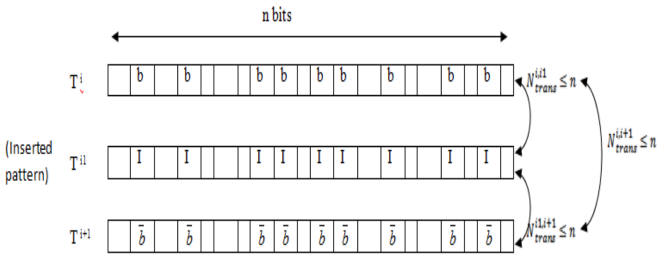


Fig. 3b Patterns insertion based on Bit insertion strategy

5.3. Bit Swapping Technique

Bit Swapping Technique is obtained by inter changing the positions of the bits of the test pattern. For example LT-GLFSR outputs of D_0,D_1 and D_2 are interchanged by D_3,D_4 and D_5. in LT-GLFSR, This process is done by 2x1 multiplexer enabled by selector signals. Multiplexer is used to select either bit swapped GLFSR output or Bit Insertion output. In this modifications [1] the output of the two cells will have its transition count reduced by $T_{saved} = 2^{(n-2)}$ transitions. Hence, it reduced the 25% of total number of the transition for each cell swapped.

VI. Implementation of GLFSR with Bipartite Bit Insertion and Bit Swapping Technique (LT-GLFSR)

Implementation of proposed methods, the GLFSR combine with Bipartite, Bit-Insertion and Bit-Swapping technique for low-power BIST. It is called as LT-GLFSR. The proposed method generates three intermediate patterns (T^{i1}, T^{i2}, and T^{i3}) between two consecutive random patterns (Ti and T^{i+1}) generated by GLFSR which is enabled by non overlapping clock schemes. LT-GLFSR provides more power reduction compared to LT-GLFSR (bipartite), conventional GLFSR and LFSR techniques. An intermediate pattern inserted by this technique has high randomness with low transitions can do as good as patterns generated by GLFSR in terms of fault detection and high fault coverage.
In bipartite technique, each half of T^{i1} is filled with half of T^i and T^{i+1} is shown in equation 8.

$$T^{i1} = \left\{t_1^i, \ldots, t_2^i, t_{\frac{n}{2+1}}^{i+1}, \ldots, t_n^{i+1}\right\} \qquad (8)$$

GLFSR with bipartite technique [14], GLFSR is divided into two parts by applying two complementary (non-overlapping) enable signals (En1 & En2). First part of GLFSR includes flip-flop that are D_0, D_1, D_3, D_4, D_6, D_7, D_9 and $D_{10\ldots}$Second part is D_2, D_5, D_8 and $D_{11.}$ In other words, one of the two parts of GLFSR is working, when other part is in idle mode. GLFSR including flip-flops with two different enable signals is shown in Fig.4a.

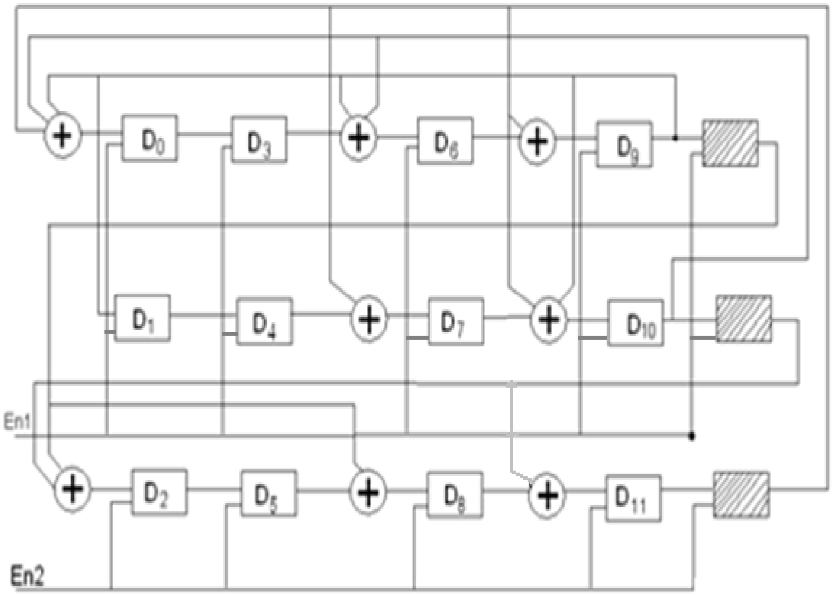


Fig. 4a Architecture of LT- GLFSR with Bipartite Technique

In proposed method, GLFSR with bipartite and bit insertion technique has four different enable signals as shown in Fig. 4b.It has four non overlapping enable signals are En1, En2, Sel1 and Sel2.Generally, En1 & En2 are to activate GLFSR with bipartite technique as shown in Fig.4d and Sel2 & Sel2 are to activate the GLFSR with bit insertion technique as shown in Fig.4e by bit insertion circuit as shown in Fig.4c. Sequence of enable signals generated by finite state machine are given as 1011,0010,0111 and 0001. En1 and En2 are enable a part of GLFSR.Sel1 and Sel2 are selector signals of multiplexers and Hence, its select output of either GLFSR or Bit insertion circuit with respect to enable and selector signals. The first part of GLFSR is working and second part is idle, When En1En2Sel1Sel2 =1011. The second part works and first part is in idle, when En1En2Sel1Sel2= 0111. Idle mode part has to provide output as present state (stored value). Output of test pattern generator is in terms of part of GLFSR output in idle mode and remaining part is output of bit insertion circuit, when En1En2Sel1Sel2=0001&0010. The additional flipflops (shaded flip-flops(D)) are added to the LT- GLFSR architecture in order to store the n^{th},$(n-1)^{th}$ and $(n-2)^{th}$ bits of GLFSR. Initially, to store the $(n-1)^{th}$ and $(n-2)^{th}$ bits of GLFSR , when En1En2 = 10 and send $(n-2)^{th}$ bit value into the XOR gate of D_2 and D_8 flip-flop and $(n-1)^{th}$ bit value into the XOR gate of D_2 and D_{11} flip-flop, when second part becomes active, that is En1En2 =01.Finally, to store the n^{th} bit of GLFSR, when En1En2 = 01 and send its value into the XOR gate of D_0,D_7 and D_{10} flip-flop when the first part becomes active En1En2 =10.

Generally, the output of LT-GLFSR is based on enable and selector signals. Note carefully that the new (shaded (D)) flip-flop does not change the characteristic function of GLFSR. The GLFSR's operation is effectively split into two parts and it is enabled by the four different enable signals as shown in Fig. 4f. This method is similar to the Modified clock scheme LFSR (Girard *et al*, 2001). They were used two n/2 length LFSRs with two different non-overlapping clock signals which increases the area overhead. Insertion of Intermediate patterns T^{i1}, T^{i2} and T^{i3} between two consecutive patterns generated by GLFSR (3, 4) is T^i and T^{i+1}.

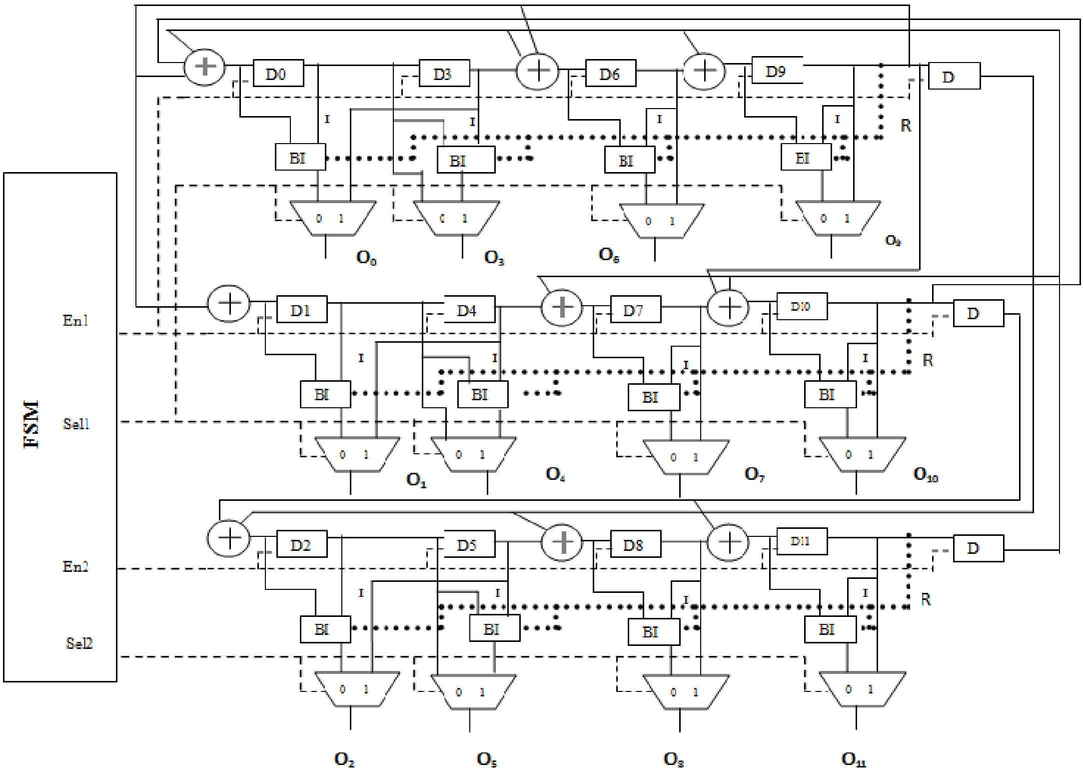
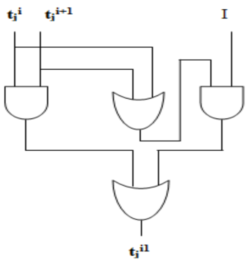


Fig. 4b Architecture of LT- GLFSR with Bipartite, BI and BS Technique



t_j^i	t_j^{i+1}	t_j^{i1}
0	0	0
1	1	1
0	1	I
1	0	I

Fig. 4c an BI Circuit

One part of the LT-GLFSR flip-flops are clocked in each cycle, but in conventional LFSR and GLFSR flip-flops are clocked at the same time in each clock cycle, thus its power consumption is much higher than LT-GLFSR. The power consumed by LFSR, GLFSR, LT-GLFSR (Bipartite) and LT-GLFSR (Bipartite and BI) with ISCAS bench mark circuits are tabulated as shown in Table.III and IV.

The following steps are involved to insert the intermediate patterns in between two consecutive patterns

Step 1. en_1en_2 = 10, sel_1sel_2 = 11(1011).

The first part (D_0, D_1, D_3, D_4, D_6, D_7, D_9 and D_{10}) of GLFSR is active and the second Part (D_2, D_5, D_8 and D_{11}) is in idle mode. Selecting sel_1sel_2 = 11, both parts of GLFSR are sent to the outputs (O_1 to O_n). In this condition first part (D_0,D_1,D_3,D_4,D_6,D_7,D_9 and D_{10}) of GLFSR are send to the outputs (O_0,O_1,O_3,O_4,O_6,O_7,O_9 and O_{10}) as next state and no bit change in second part (D_2,D_5,D_8 and D_{11}) of GLFSR are send to the outputs (O_2,O_5,O_8 and O_{11}) as its present state (Stored value) and also position of outputs of D_0,D_1 and D_2 are interchanged by D_3,D_4 and D_5 . In this case, T^i is generated.

Step 2. en_1en_2 = 00, sel_1sel_2 = 10(0010).The both parts of GLFSR are in idle mode. The first Part of GLFSR is sent to the outputs (O_0,O_1,O_3,O_4,O_6,O_7,O_9 and O_{10}) as its present state (stored value) but the bit insertion circuit inserts a bit (0 or 1) to the outputs (O_2,O_5,O_8 and O_{11}) and also position of outputs of D_0 and D_1 are interchanged by D_3 and D_4. T^{i1} is generated.

Step 3. en_1en_2 = 01, sel_1sel_2 = 11(0111).
The first part of GLFSR is in idle mode. The second part of GLFSR is active. In this condition first part (D_0,D_1,D_3,D_4,D_6,D_7,D_9 and D_{10}) of GLFSR is send to the outputs (O_0,O_1,O_3,O_4,O_6,O_7,O_9 and O_{10}) as present state and second part (D_2,D_5,D_8 and D_{11}) of GLFSR is send to the outputs (O_2,O_5,O_8 and O_{11}) as its next state and also position of outputs of D_0,D_1 and D_2 are interchanged by D_3,D_4 and D_5. T^{i2} is generated.
Step 4. en_1en_2 = 00, sel_1sel_2 = 01(0001).
Both Parts of GLFSR are in idle mode. The second part of GLFSR is send to the Outputs (O_2, O5, O8 and O_{11}) as its Present state. Bit insertion circuit will insert a bit (0 or 1) into the outputs (O_0, O_1, O_3, O_4, O_6, O_7, O_9 and O_{10}) and also positions of output of D2 are interchanged as D_5. T^{i3} pattern is thus generated.
Step 5. The process continues by going through Step 1 to generate T^{i+1}

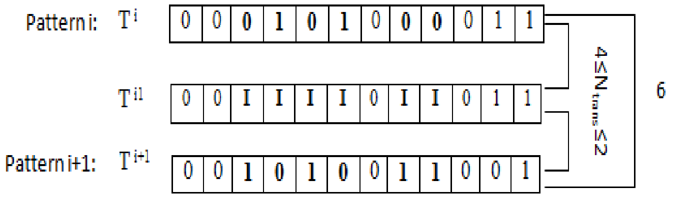


Fig.4d Bit Insertions in LT-GLFSR Bipartite Technique

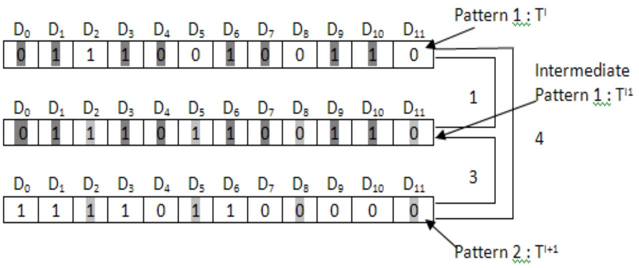


Fig.4e Bit Insertions in LT-GLFSR Bipartite Technique

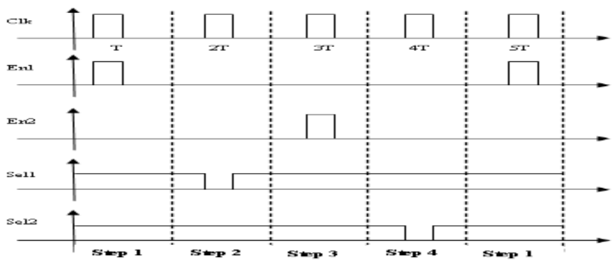


Fig. 4f Timing diagram of Enable signals

VII. RESULTS

The test patterns generated by LFSR, GLFSR,LT-GLFSR(Bipartite) and LT-GLFSR(BI and BS) are used for verifying the ISCAS85 benchmark circuits S298 and S526. Simulation and synthesis are done in Xilinx 13 and power analysis is done using Power analyzer. The results in Table 3and 4, are the test patterns for fault coverage and the reduction in the number of test patterns. Power analysis is carried out with the maximum, minimum and typical input test vectors for stuck-at faults and transition faults of sequential circuits (CUT).
Fig.5a shows the distribution of the number of transitions in each bit of the pattern generated using GLFSR, LT-GLFSR (BS) and LT-GLFSR (BI & BS) for 50 patterns. A transition in each bit of the patterns generated LT-GLFSR (bipartite) is varies in between 5 to 10 transitions. It has comparatively less number of transitions with patterns generated by GLFSR. Fig.5b shows the output of the LT-

GLFSR (BI &BS). These test patterns reduce switching transitions in test pattern generator as well as for the circuit under test.

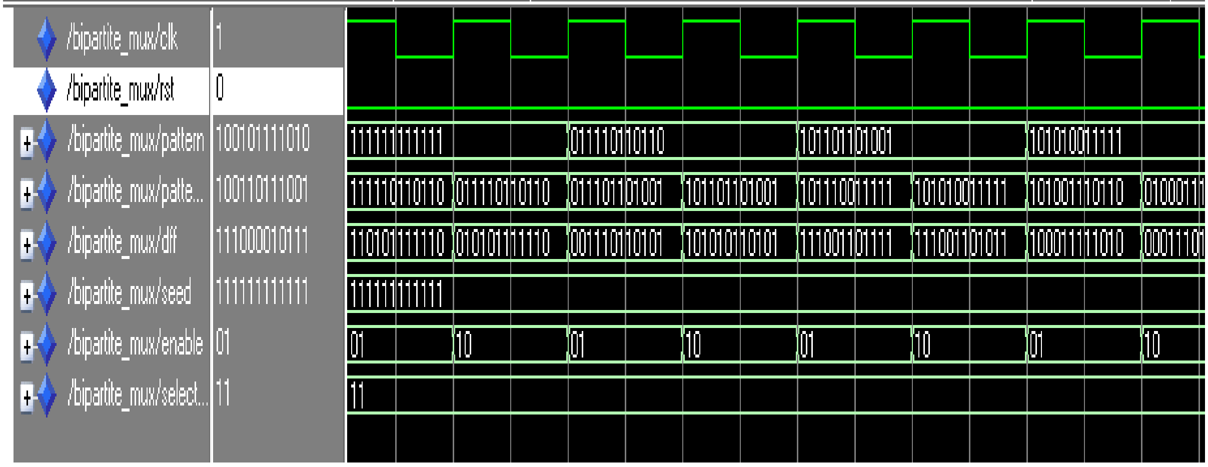


Fig.5c LT-GLFSR (Bipartite, BI and BS) Test pattern generator

VIII. DISCUSSIONS

Test patterns are generated by LFSR, LT-GLFSR(bipartite) and LT-GLFSR(bipartite and bit insertion) and the analysis of randomness or closeness among the bit patterns are done. From the analysis the test patterns generated by LT-GLFSR(bipartite and bit insertion) has significantly greater degree of randomness, resulting in improved fault coverage when compared to standard LFSR and GLFSR. GLFSR is modified by means of clocking such that during a clock pulse one part is in idle mode and other part in active mode. This modification is known as LT-GLFSR which reduces transitions in test pattern generation and increases the correlation between and within the patterns by inserting intermediate patterns. From the discussed three methods, the LT GLFSR has less number of test patterns required for high fault coverage with high degree of closeness, randomness and low power consumption for the CUT.

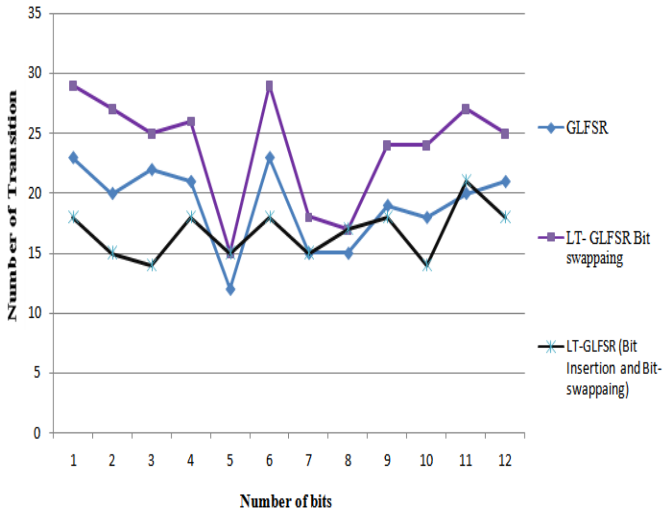


Fig.5a Distribution of the number of transitions in each Bit of the pattern generated using GLFSR & LT-GLFSR (bipartite) for 50 patterns

Table 2. Test Patterns for first 20 states

Test pattern	LFSR	LT-LFSR (Bipartite)	LT-LFSR (bit insertion & bit swapping)
1	111111111111	111111111111	111111111111
2	011111111111	011100100110	011110110110
3	001111111111	101111011100	101101101001
4	100111111111	111101100000	010100111111
5	001001111111	101110011000	010001110110
6	000100111111	101001111000	010011101100
7	000010011111	000110111101	110101011000
8	100001001111	111011111010	011011111101
9	110000100111	000010111100	100101111010
10	011000010011	110011111000	111010111001
11	001100001001	010010111000	100100111010
12	000110000100	000101100000	011100111001
13	000011000010	001011000000	011111110111
14	000001100001	110110000101	001011101011
15	000000110000	001111000111	010001010110
16	000000011000	101000011011	010011011000
17	000000001100	000101111011	100000110000
18	100000000110	100000000110	110010101000
19	110000000011	110000000011	110100011000
20	111000000001	011011011011	111101111101
21	011100000000	010110100110	011110110111

Table 3 Transition Fault Detected in S298

No. Of faults: 25			
Pattern Generation	Number of test Pattern	Pattern Reduction (%)	Power (mW)
LFSR	53	--	45.56
GLFSR	17	32.09	25.98
LT-GLFSR (BS)	12	22.67	21.23
LT-GLFSR(BI &BS)	13	23.65	22.25

Table 4 Transition Fault Detected in S526

No. Of faults: 20			
Pattern Generation	Number of test Pattern	Pattern Reduction (%)	Power (mW)
LFSR	567	--	58.9
GLFSR	234	41.26	39.7
LT-GLFSR (BS)	197	34.74	31.6
LT-GLFSR(BI &BS)	180	31.2	29.12

IX. CONCLUSION AND FUTURE SCOPE

An effective low-power pseudorandom test pattern generator based on LT- GLFSR (BI & BS) is proposed in this paper. Power consumption of LT-GLFSR is reduced due to the Bipartite, Bit insertion and Bit swapping technique. Only half of the LT-GLFSR flip-flops are clocked in each cycle then bit swapped with respect to selector signal. LT-GLFSR's provide for greater randomness than standard LFSR and GLFSR, which have the potential to detect most stuck-at and transition faults for CUT with a fraction of patterns. This will be significance for the faults detection for ISCAS circuits with a minimum number of input test patterns. The switching activity in the CUT and scan chains, their power consumption are reduced by increasing the correlation between patterns and also within each pattern. This is achieved with almost no increase in test length to hit the target fault coverage. As a future scope the proposed work is applied for the complex sequential circuits. Concept of GLFSR and Cellular Automata can be combined in order to get better degree of randomness and cover more number of faults with few numbers of patterns.

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