DESIGN OF LOW POWER VITERBI DECODER USING ASYNCHRONOUS TECHNIQUES

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ABSTRACT

In today's digital communication systems, Convolutional codes are broadly used in channel coding techniques. The Viterbi decoder due to its high performance is commonly used for decoding the convolution codes. Fast developments in the communication field have created a rising demand for high speed and low power Viterbi decoders with long battery life, low power dissipation and low weight. Despite the significant progress in the last decade, the problem of power dissipation in the Viterbi decoders still remains challenging and requires further technical solutions. The proposed method is focused on the design of VLSI architecture for a Viterbi Decoder using low power VLSI design techniques at circuit level with asynchronous QDI templates and Differential Cascode Voltage Switch Logic (DCVSL). The design of various units of Viterbi Decoder is done using T – SPICE in 0.25um Technology. The simulation results of the asynchronous design shows 56.20% power reduction with a supply voltage of 2.5 Vdd is achieved when compared to synchronous design.

KEYWORDS: *Viterbi decoder, Asynchronous, DCVSL, QDI templates, PCHB, Low-Power, T -SPICE*

I. INTRODUCTION

The Viterbi decoding [2] algorithm, proposed in 1967 by Viterbi, is a decoding process for convolutional codes in memory-less noise. The algorithm can be applied to a host of problems encountered in the design of communication systems like Satellite, (WLAN), etc. It offers an alternative to block codes for transmission over a noisy channel. Convolutional codes are usually described using two parameters, the code rate and the constraint length. The code rate r=k/n, is expressed as a ratio of the number of bits into the convolutional encoder (k) to the number of channel symbols output by the convolutional encoder (n) in a given encoder cycle. The constraint length parameter K denotes the length of the convolutional encoder and it indicates how many k-bit stages are available to feed the combinational logic that produces the output symbols. The decoder is designed for a code of rate ½ - with a constraint length of K = 3 to 7. The Viterbi decoder comprises of Branch metric Unit (BMU), Add Compare Select Unit (ACS) And Survivor Memory Unit (SMU). The BMU calculates the branch metrics by the hamming distance or euclidean distance, and the ACSU calculates a summation of the branch metric from the BMU and previous state metrics, which are called the path metrics. After this summation, the value of each state is updated and then the survivor path is chosen by comparing path metrics. The SMU processes the decisions made in the BMU and ACSU, and outputs the decoded data. The feedback loop of the ACSU is a major critical path for the Viterbi decoder. The Author has discussed a QDI based asynchronous Viterbi decoder [11], but it does not concentrate on SMU design.

This paper presents a low power asynchronous VLSI architecture for Viterbi decoder to reduce power dissipation with increased speed; Section I discuss the introduction and advantage of asynchronous design, literature survey carried out for the proposed work. Section II explains about the asynchronous BMU, ACS and SMU with interal transistor level circuits and reveals the integrated design of asynchronous viterbi decoder. At last section III discusses the simulation results and performance comparison of the proposed work with synchronous and existing literature survey. In SMU the registers are designed using transparent latches. Thus the objective of the author is to analyse the performance of the decoder in terms of area, speed and power. The asynchronous design is based upon Quasi Delay Insensitive (QDI) timing model which leads to a robust and low power purpose and synchronous architecture uses a hybrid CMOS–Pseudo NMOS technology [1] to improve area and throughput factors. A combined approach of traceback and register exchange survivor path processing of [3] Viterbi decoders was discussed. In Combinational logic technique QDI Boolean functions can be synthesized [5] using a small set of standard cells. Quasi-Delay-Insensitive circuits are more robust and amenable to reuse and verification than other circuit styles.

II. ASYNCHRONOUS VITERBI DECODER

Asynchronous circuits are composed of blocks that communicate to each other using handshaking via asynchronous communication channels, in order to perform the necessary synchronization, communication, and sequencing of operations.

Asynchronous communication channel consists of a bundle of wires and a protocol to communicate the data between the blocks. There are two types of encoding scheme in asynchronous channels. If the encoding scheme uses one wire per bit to transmit the data and a request line to identify when the data is valid is called single-rail encoding. The associated channel is called a bundled-data channel.

Alternatively, in dual-rail encoding the data is sent using two wires for each bit of information. Dual-rail encoding allows for data validity to be indicated by the data itself. They are often used in QDI designs. Hence in the proposed asynchronous design of Viterbi decoder 4 phase handshaking protocol in dual rail encoding scheme is used.

The two modules used instead [4] of clocking strategies are the Weak Charge Half Buffer (WCHB) and Pre Charge Half Buffer (PCHB).

2.1 Branch Metric Unit (BMU)

The architecture of the BMU comprises of a xor gate and a counter. The branch word depends on the constraint length, the generator matrix, and the code rate. One input to the xor gate is the received code symbol and the other input is the expected sequences which are the encoder output. Xor gate determines the difference in the number of transitions in the inputs and counter counts the total number of differing bits. The hardware realization of the BMU computation block is shown in figure.1.The outputs of the encoder i.e expected word and the received word are taken as a0 and b0 (2) inputs for the xor gate with a C-element, Realization of trellis into a hardware require two paths i.e upper path and a lower path. Output of the xor gate is given to the counter. Here 3 bit counter is used. Normally the hamming distance does not exceed seven. The output is buffered using WCHB so that the corresponding branch metric values are obtained without any delay. C-element ensures completion of operation between the transistors.

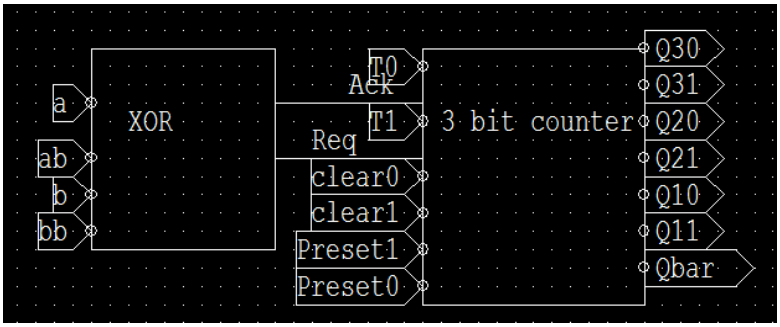

Figure1 Hardware realization of Branch Metric Computation Block

2.2 Add Compare and Select Unit

Hardware realization of ACS unit in figure.2 has adder, comparator and selector. Two inputs a and b are given to the one of the two inputs of the adders. Initial value of the other input of the adder i.e the path metric value is taken as zero. In this method a 4 bit asynchronous ripple carry PCHB is constructed by rippling four 1-bit asynchronous full adders shown in figure 3. The lower bits to the adder are the path metrics (previous branch metrics). Inputs to the adder are a [0:4], b [0:4], Carry C and their complements. Delays between the adders are balanced by adding WCHB buffers. A comparator then compares the resulting path metrics, and the lesser one is the output from the ACS unit.

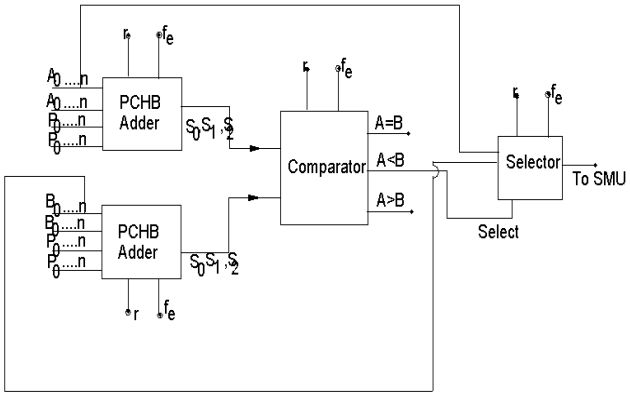

Figure 2 Hardware Realization of Add Compare Select Unit

The circuits are implemented by using DCVSL logic. For the constraint length of K=3 and code rate-1/2, it has four states and it requires 4-bit adder, comparator and selector. Normally carry signal will limit the speed of the circuit. Hence to construct an n bit adder, it is easier to connect n '1' bit adders. This adder is called Ripple Carry adder. The delay for an n bit adder is

$$t_{rca} = (n-1)t_c + t_s \qquad (2)$$

Where tc is the carry delay and ts is the sum delay.

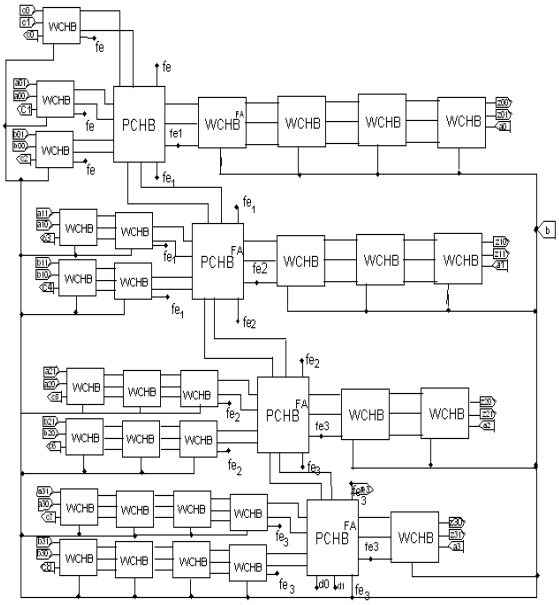

Figure 3 Four Bit Ripple Carry Asynchronous Adder

SMU design is based on modified register exchange method [12]. A pointer keeps track of the minimum value of the path metric. This minimum value is stored in the registers. Hence there is minimum power consumption when compared to trace back and register exchange methods. So Instead of memory units which consume more power due to the decoding of column and row address, registers are used to shift and store the data temporarily. For example if the constraint length is K=3, there is 2^{k-1} registers for each state. If the required row of memory is predetermined, then there is no need for the storage of the other rows.

Four x four registers are used for each stage with a multiplexer. The less than output of the comparator is given to the select line of the Mux and the minimum value of associated inputs is shifted to each registers.

In the architecture the inputs a, abar, b, bbar are the inputs to the SMU and the configuration of the registers are Serial In Serial Out fashion. The asynchronous memory unit shown in figure.4, the construction of SMU using asynchronous FF (latches) and DCVS logic based 2:1 multiplexer.

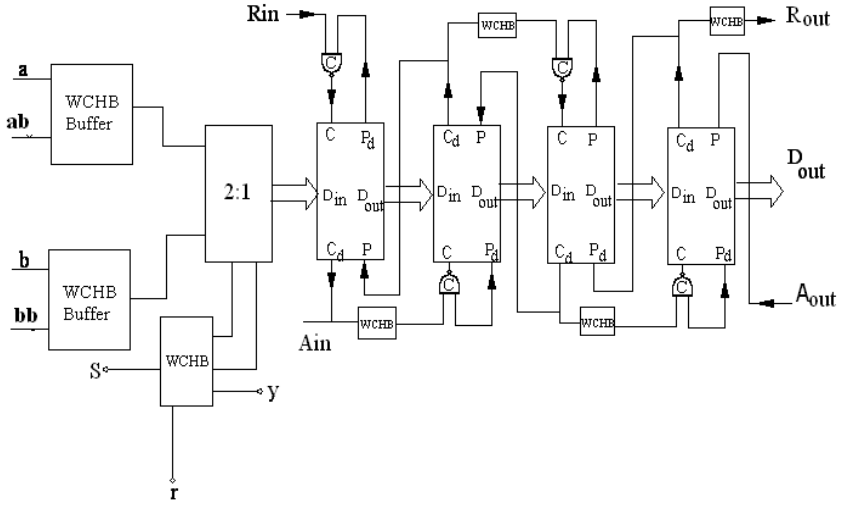

Figure 4 Survival Memory Unit for Single State

Registers are constructed by means of asynchronous latches (Transparent latch) [10]. Data shift register is constructed by transition latches [7]. Basic structure of capture passes storage logic is involved in the design of latches [9]. Only drawback that has to be adjusted is that the control circuits for protocol signals. The capture-pass latch is transparent until an event occurs on the capture line. This causes the latch to hold any data that was on its input line. Din at that time. The capture done event indicates that the capture operation has been finished. Dout has the input value; further change in the input does not affect the output. An event on the pass signal makes the latch to go its transparent state and to ensure this operation was completed an event pass done signal takes place.

1.3 Differential Cascaded Voltage Switch Logic (DCVS)

The following figure shows the DCVSL Arithmetic circuits used in the architectures of BMU, PMU and SMU. Figure 5 Shows the asynchronous PCHB and DCVS logic based full adder sum and carry transistor level design. a and b represent the 2 input signals of the adder, s1 (d1) and s0 (d0) represents the true and complement sum (carry) output signal, en and se (de) are asynchronous PCHB logic handshaking signals. When the en and se signals are active low, the PMOS pull-up transistors turned on and s0, s1 are set to logic high. When the en, se signals become active high, the PMOS transistors are turned off , depending on the input signals either s0 (d0) or s1 (d1) is pulled to ground. The same operation is performed for carry also.

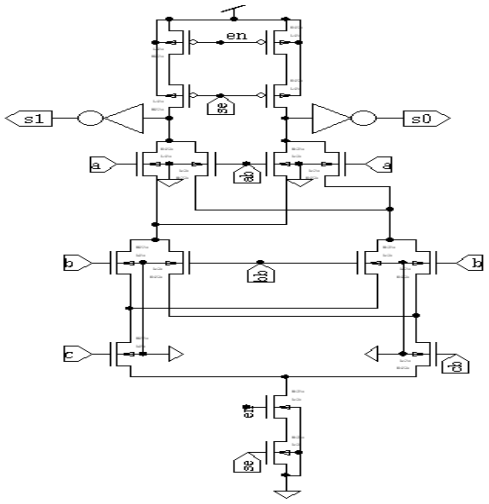

Figure 5 Full Adder sum and carry

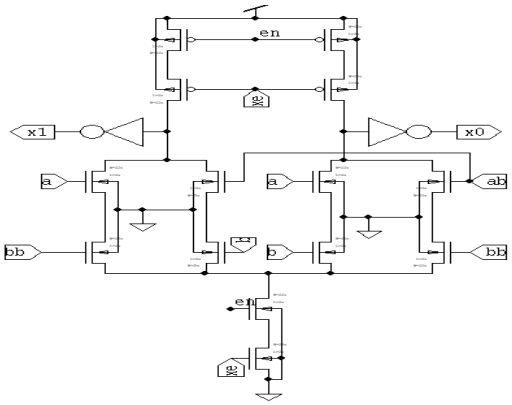

Figure 6 DCVS based XOR gate

The above figure 6 gives the implementation of XOR gate used in the comparator design of BMU and ACS unit. The transistor level diagram in figure.7 shows the multiplexer mainly used in selector of ACS Unit and SMU. When en and se signals are active low, evaluation of the buffer takes place. If the input to the transistor a=1 and b=0, the n transistors evaluates the logic and give high output at s1.

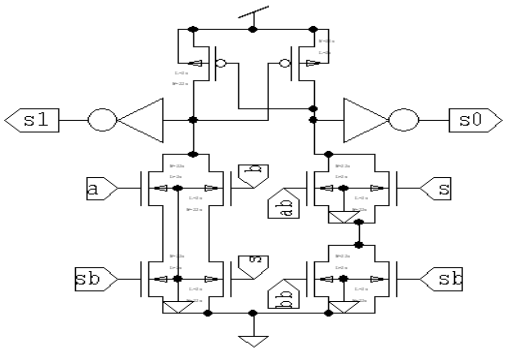

Figure 7 DCVS based Multiplexer

The inputs to the multiplexer are a and b, select lines are given by sa and sb respectively. Outputs of the multiplexer are s0 and s1.

2.4 Integrated Design of Viterbi Decoders using QDI Templates

Viterbi decoder comprises of three blocks and in the proposed design the three stages are connected in a linear fashion using the WCHB and PCHB templates shown in Figure 11. The operation of the asynchronous design is explained with respect to a state transition graph. When the first data is given

as input for the BMU, LCD1 generates a signal to turn on C1 in order to enable the pc and en signals. The given input data is evaluated by the BMU. When the outputs of BMU are validated, completion signal from the RCD1 is sent to the C1 of the BMU stage and LCD2 of the ACS stage, now ACS starts evaluating the data. As soon as the output of ACS is valid, RCD2 generates a completion signal to C2 and acknowledgement signal to Lack in the BMU stage, also a request signal to LCD3 unit of SMU. Now BMU unit goes to the precharge phase and SMU is ready for evaluation of data. Thus the three stages executes in a linear pipeline fashion without pipelining registers. The control signals such as se, en, pc, Lo, L1, Ro, R1, and C are designed separately and the signals are connected in the design wherever necessary. The control signals such as se, en, pc, Lo, L1, Ro, R1, and C are designed separately and the signals are connected in the design wherever necessary

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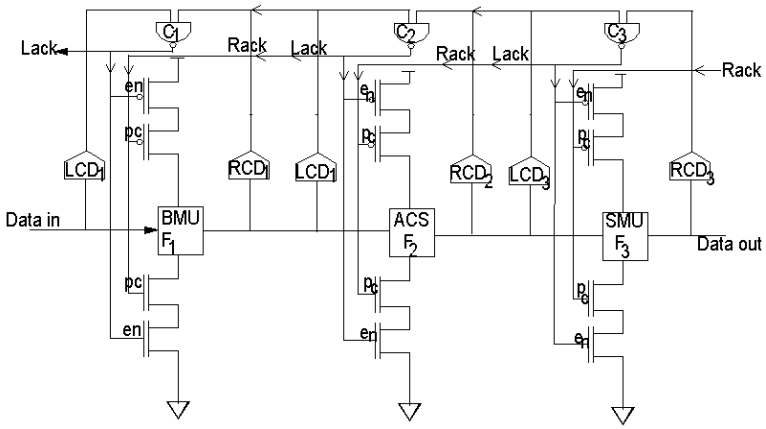

Figure 8 Integrated Design of Viterbi Decoder

2.5 Synchronous Viterbi Decoder

Synchronous Viterbi decoder is designed in order to compare the performances with the asynchronous design. In synchronous design a global clock is used to synchronize the operation. The DCVS logic based transistor level designs are used. Figure 9 shows the Output Waveform of Synchronous Viterbi decoder . The inputs of the two branch metric units are the received sequence and the expected sequence. The received sequence input is a=c=11 01 11 and the expected sequence are b= 00 10 01 & d= 11 01 10. The output of the Viterbi decoder is the decoded sequence VD_out is "11 01 10"

III. SIMULATION RESULTS AND DISCUSSION

The Viterbi Decoder is simulated in T-SPICE to obtain timing behavior and power consumption for the constraint lengths of K=3 to 7 with a code rate of 1/2. For K>9 the complexity of the decoder increases. Random of inputs are fed to the convolutional encoder and the outputs of the encoder is fed as input to the Viterbi decoder. Both synchronous and asynchronous designs based on DCVSL logic is simulated with T-SPICE. This work is also compared with an existing asynchronous technique.

For each constraint length random of 5 sets of message sequence was given and the outputs are verified. Architecture of the Viterbi decoder comprises of two paths upper path and lower path. Hence the inputs are a (expected sequence) and b (received sequence) to the decoder. First step execution is the result of branch metric unit obtained by the hamming distance. Then the path metric value is calculated, added, compared and selected for the given input sequence. The dual rail output of the Viterbi decoder is VD_out^0 and VD_out^1. Viterbi decoder uses two branch metric units since each state have two branches in the trellis. Here the expected sequence is a=c="11 01 10" and the received sequence for the first branch metric is b="00 10 01" and received sequence for the second branch metric is d="11 01 11" and the decoded output sequence is VD out="11 01 10" which is

obtained with errors. Bit Error Rate analysis in not considered in this design. Complete set of input and output sequence is given in figure 10.

Since the asynchronous design comprises of control signals se, en, pc, R0, R1, L0, L1, they are collectively represented in the waveform shown in figure 11. Signals like en and pc are kept at low logic when the transistors are in precharge phase, when they are at high value, evaluation phase takes place. R0, R1, L0, L1 represent the control signals of WCHB buffer. In all the figures, Req and Ack signals are not shown, as they are represented in the complete integrated Viterbi decoder block diagram.

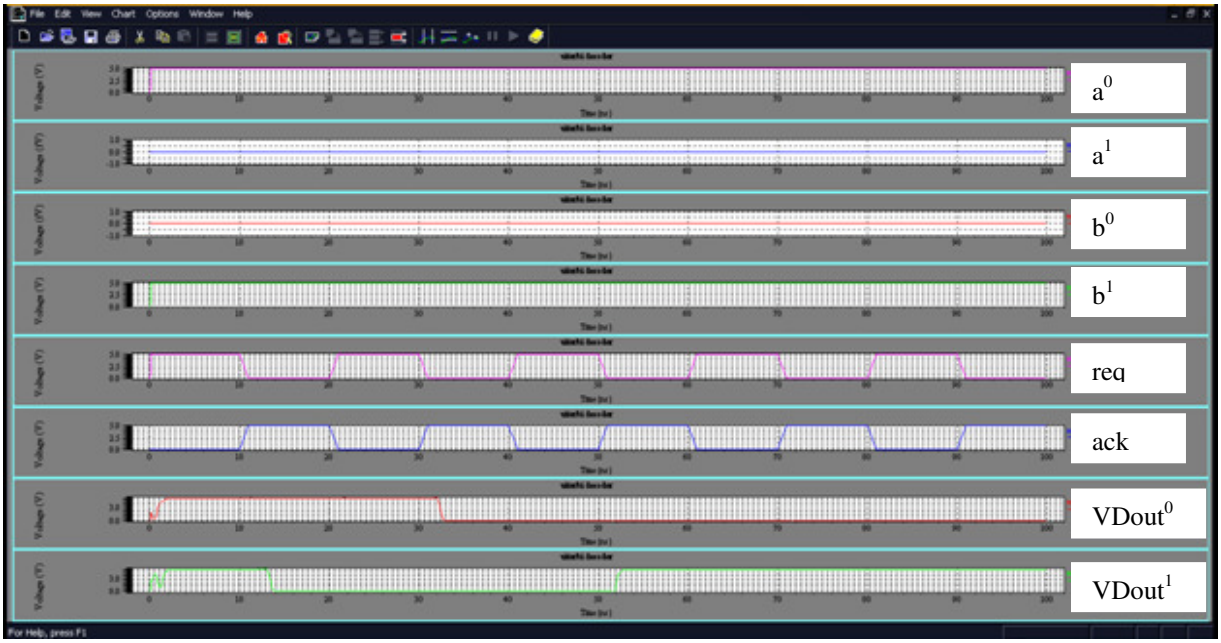

Figure 9 Output waveform of asynchronous Viterbi decoder

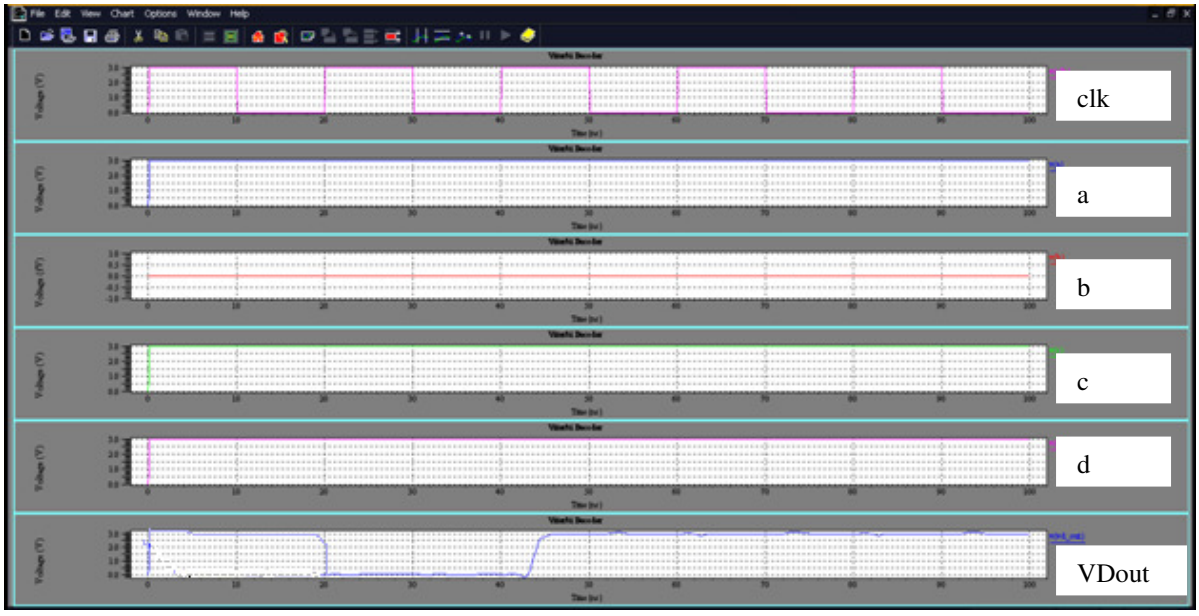

Figure 10 Output of Synchronous Viterbi Decoder for K=3

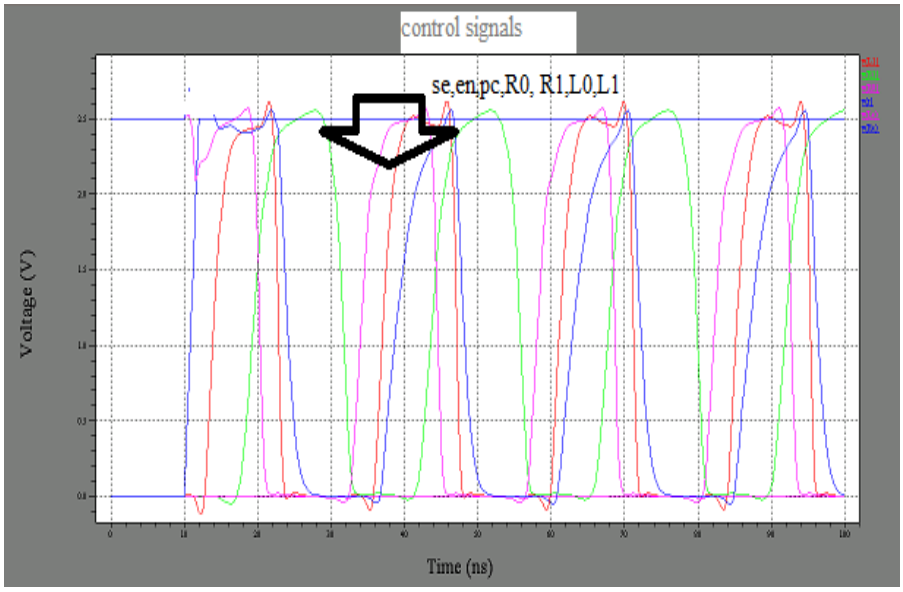

Figure 11 Buffer and Control Signals

Simulation results in Table 1 show that the asynchronous circuit has a high transistor count with a frequency of 425 MHz when compared to the synchronous circuit. Table 2 shows the average power consumption of Viterbi decoder for various constraint lengths. Asynchronous design has 56.20% less power consumption when compared to synchronous design. Also it has 27% reduced amount of power consumption than the existing 4 phase protocol with single rail encoding [8] asynchronous design.

Table 1 Comparison of Parameters for the Viterbi Decoder

Module Name	Parameters		
	No. of Transistors	Frequency in MHz	Delay in sec
Synchronous Design	9215	320MHz	3.12ns
Asynchronous Design	16802	425MHz	2.13ns

Table 2 Comparison of Power Dissipation of the Viterbi Decoder

Viterbi decoder Power consumption (mW)			
Constraint Length K	Proposed Synchronous Method	Existing 4 Phase Single Rail Encoding Asynchronous Design	Proposed Asynchronous QDI Method
3	140.14		61.736
4	141.26		61.79
5	140.23		6 1.82
6	142		62.85
7	141.65		61.765
Average power (mW)	141.56 mW @ 320MHz	85mW @ 426 MHz	61.99 mW @425MHz

Table 3 Comparison of Viterbi Decoder Design [6]

Design	Technology	Vdd (v)	Power in mW
Synchronous (reference)	0.35µm	n/a	203
Systolic array	0.5 µm	3.3	280
SPL	0.35µm	2.5	88
Self timed	0.35µm	n/a	1333[8]
Asynchronous QDI[javadi]	0.35µm	3.3	166
Asynchronous QDI[javadi]	0.35µm	2.5	85
Optimized ACS	0.35µm	3.3	109
Optimized ACS	0.35µm	2.5	62
Proposed Asynchronous PCHB & DCVS design	0.25µm	2.5	61.9

Table 3 shows the comparison of proposed asynchronous technique with the techniques from the literature survey. Proposed Asynchronous method featured a power reduction from 4.6 % to 72.9% with that of the existing asynchronous [6] method.

IV. CONCLUSION

Viterbi decoders employed in digital mobile communications are complex in its implementation and dissipate large power. The proposed Viterbi decoder uses asynchronous design techniques to reduce power consumption. The asynchronous design was based upon Quasi Delay Insensitive (QDI) timing model implemented in DCVSL which is used for robust and low power applications. The simulation results show the asynchronous design has the decrease in power consumption by 56.20% with increase in transistor count by 1.8 times in relative to synchronous Viterbi decoder with code rate of ½ and constraint length of 3 to 7 in 0.25µm CMOS technology with a power supply of 2.5V.

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