COMPARATIVE ANALYSIS OF ENERGY-EFFICIENT LOW POWER 1-BIT FULL ADDERS AT 120NM TECHNOLOGY

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ABSTRACT

In this Paper we present new Low power and Energy efficient 1-Bit Full adder designs featuring Centralized, XOR-XOR and XNOR-XNOR CMOS design styles. Energy efficiency is one of the most required features of the modern electronic System designed for high performance and Portable applications. We carried out a Comparison between these designs reported as having a low PDP, in terms of Speed, Power consumption and Area. The proposed full adders are energy efficient and outperform several standard Full adders without trading of driving capabilities and reliabilities. The new Full adders successfully operate at low voltage with excellent Signal integrity and Driving Capability. Centralized based design full adder is more reliable in terms of Area, Power dissipation and Speed than other two proposed designs. All the Schematics and Layouts of these full adders were designed with a 120nm CMOS technology using Micro wind 3.1.

KEYWORDS: *Full Adder, Centralized, XOR, XNOR, Low Power*

I. INTRODUCTION

The increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits.The necessity and Popularity of portable electronics is driving designers to endeavor for smaller area, higher speed, longer battery life and more reliability. Power and delay are the premium resources a designer tries to save when designing a system. In the absence of low-power design techniques such applications generally suffer from very short battery life, while packaging and cooling them would be very difficult and this is leading to an unavoidable increase in the cost of the product. So far several logic styles have been used to design full adders. One example of such design is the standard static CMOS full adder. The main drawback of static CMOS circuits is the existence of the PMOS block, because of its low mobility compared to the NMOS devices. Therefore, PMOS devices need to be seized up to attain the desired performance. Another conventional adder is the complementary pass-transistor logic (CPL) [1]. Due to the presence of lot of internal nodes and static inverters, there is large power dissipation. Some other full adder designs include transmission function full adder (TFA) and transmission Gate full adder (TGA). The main disadvantages of these logic styles are that they lack driving capability and when TGA and TFA are cascaded, their performance degraded significantly.
These Full adder designs can be broken into three Parts. Part I comprises of either XOR or XNOR circuits or both. Part II and part III comprises of mainly multiplexers and also from gates like xor and xnor. Part I produces intermediate signals that are passed onto part II and part III that generate SUM and CARRY outputs respectively [6][15].

This Paper is structured as Follows: Section II introduce the related work regarding Full adders.Section III briefly introduce the Full adder categroziation.Section IV reprsents the Schematics of three full adders designed in DSCH and their waveforms. Section V reprsents the layout designed in microwind 3.1 version.Section VI shows the simulation results of Area, Power Dissipation and Delay of these designs.Section VII includes the future work.Finally Section VIII comprises of conclusion.

II. PREVIOUS FULL ADDER OPTIMIZATION

Many Papers have been published regarding the optimization of Low power full adders, trying different options for the Logic styles like standarad CMOS logic[1],Differential cascode voltage switch (DCVS)[2], Complementary pass-transistor logic (CPL)[3],Double pass-transistor logic (DPL)[4],Swing restored CPL(SR-CPL)[7],and hybrid styles[6]. Regarding this there is an alternative Logic structure for a full adder. Examining the full adder truth table, It can be seen that the Sum output is equal to the A⊕B value when C=0 and it is equal to (A⊕ B)' value when C=1. Thus, a multiplexer can be used to obtain the respective value taking the C input as the selection signal. Following the same criteria, the Carry output is equal to the A.B value when C=0 and it is equal to A+B value when C=1. Again, C can be used to select the respective value for the required condition, driving a multiplexer. Hence, an alternative logic scheme to design a full-adder cell can be formed by a logic block to obtain the A⊕B and (A⊕ B)' signals, another block to obtain the A.B and A+B signals, and two multiplexers being drive by the C input to generate the Sum and Carry outputs [7][14].Regarding this paper Mohammad Shamim Imtiaz et.al. proposed the Hybrid logic sturucture.In these Adder designs use more one Logic Styles for their implementation which we call the Hybrid-CMOS logic design style[6],e.g a full adder is designed using a DPL logic design style to build the xor/xnor gates and a Pass Transistor based multiplexer to obtain Sum output.

III. FULL ADDER CATEGORIZATION

Depending upon their structure and logical expression we classified these full adder cells into three categories.The expression of Sum and Carry outputs of 1-bit full adder based on binary inputs A,B, C are [3].

$$SUM = A \oplus B \oplus C$$
$$CARRY = AB+BC+CA$$

These output expression can be expressed in various logic styles and that's why by implementing those logics different full adders can be conceived.

3.1 CENTRALIZED FULL ADDER

In this category the sum and carry outputs are generated by following expression.

$$SUM = H.C' + H'C \quad H = A \oplus B$$
$$CARRY = AH' + CH$$

Part I is a XOR-XNOR circuit producing H and H' signals. Part II and part III are 2:1 multiplexers with H and H' as select lines.In the expression of sum C and C' are select lines [2].

3.2 XOR-XOR BASED FULL ADDER

In this category, the sum and carry ouputs are generated by the following expression, where H is equal to A⊕B and H' is complement of H.

$$SUM = A \oplus B \oplus C = H \oplus C$$
$$CARRY = AH' + CH$$

The output of the sum is generated by two consecutive two-input XOR gates and the carry output is the output of a 2-to-1 multiplexer with the select lines coming from the output of first XOR gate..

3.3 XNOR-XNOR BASED FULL ADDER

In this category, the sum and carry ouputs are generated by the following expression where A, B and C are XNORed twice to from the Sum and expression of carry is as same as previous category.

$$SUM = ((A \oplus B)' \oplus C)' = (H' \oplus C)'$$
$$CARRY = AH' + CH$$

IV. FULL ADDER REALIZATION

4.1 CENTRALIZED FULL ADDER SCHEMATIC

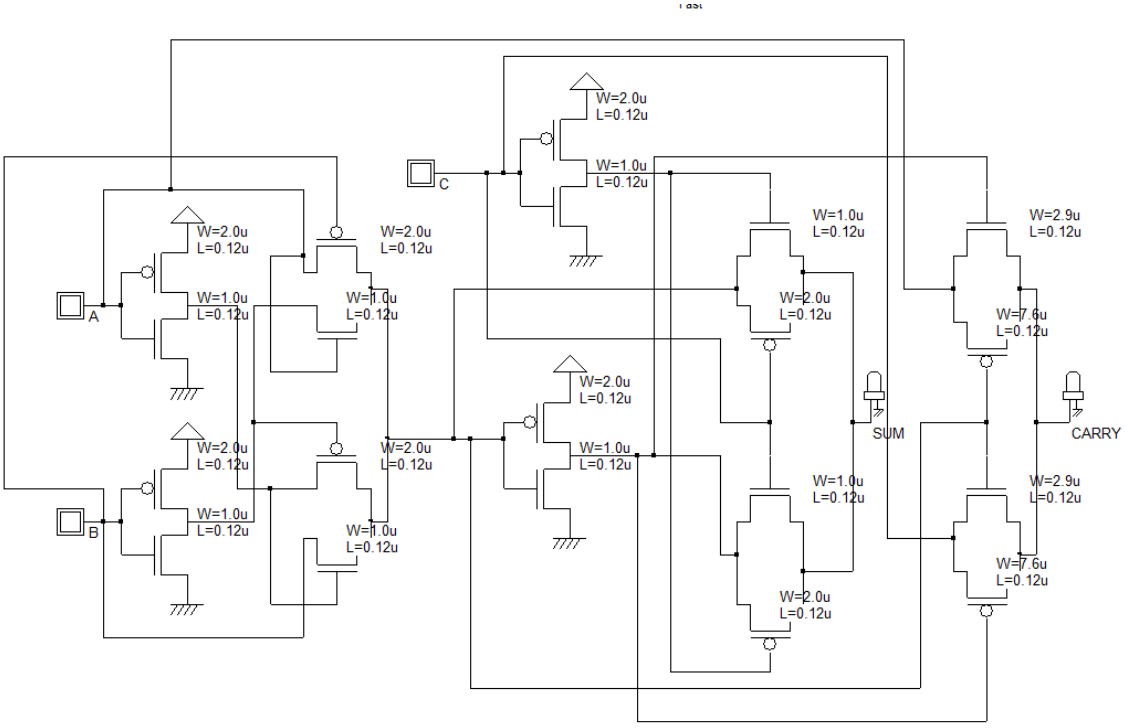


Fig .1. Centralized Full adder

4.2 CENTRALIZED FULL ADDER WAVEFORM

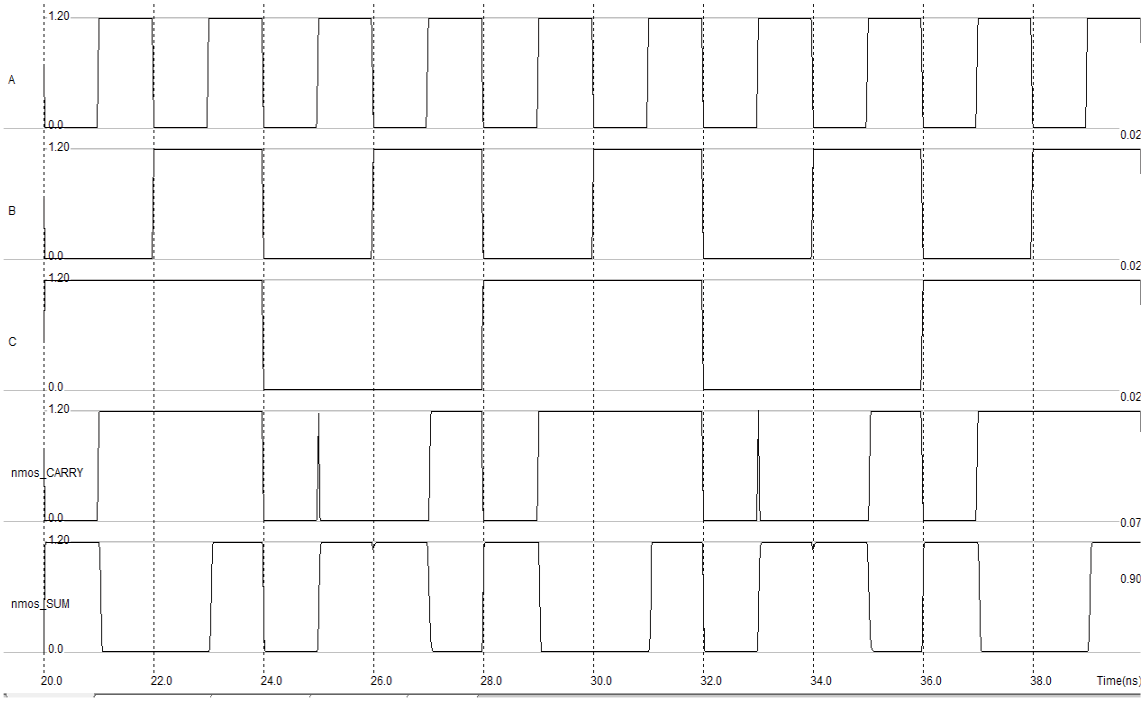


Fig .2. Centralized Full adder waveform

4.3 XOR-XOR BASED FULL ADDER SCHEMATIC

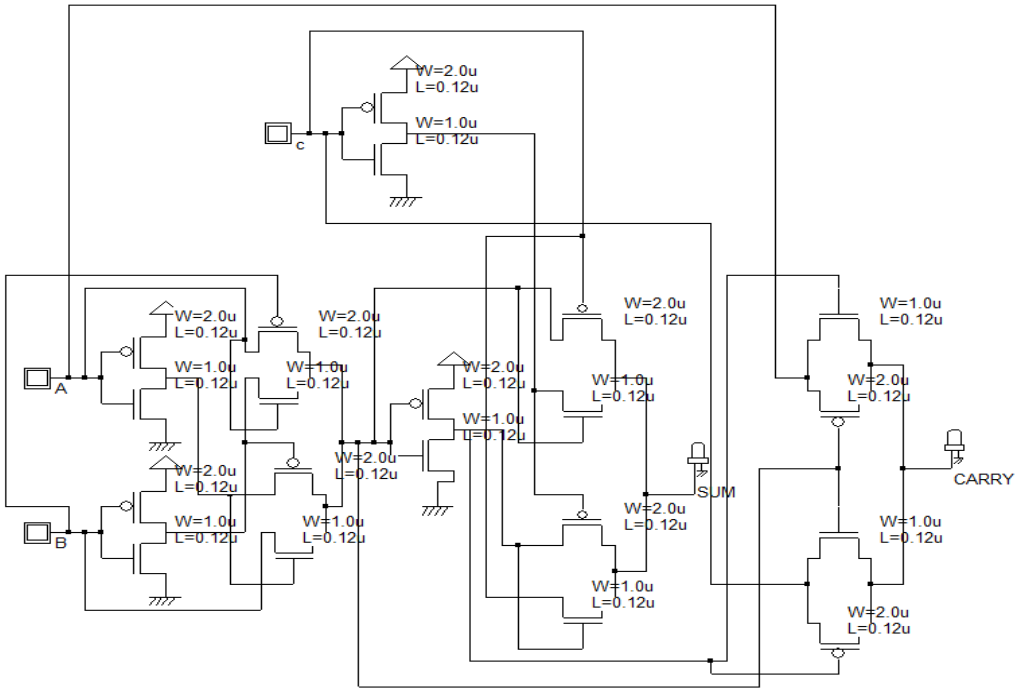


Fig .3. XOR-XOR Based Full adder

4.4 XOR-XOR BASED FULL ADDER WAVEFORM

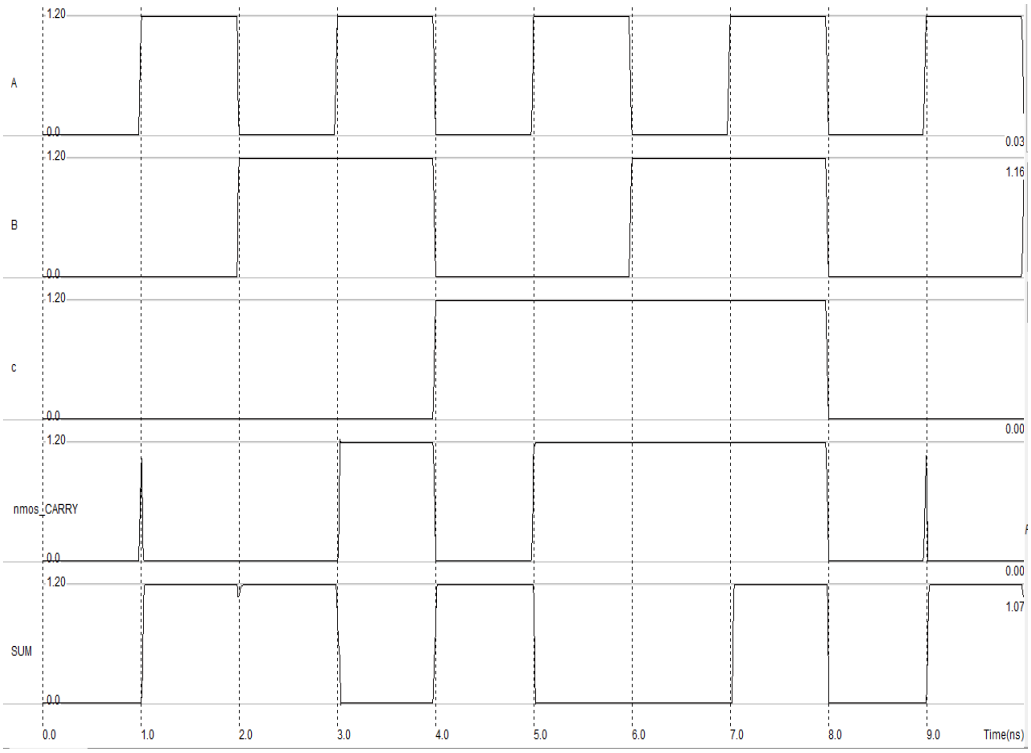


Fig .4. XOR-XOR based Full adder wavefor

4.5 XNOR-XNOR BASED FULL ADDER SCHEMATIC

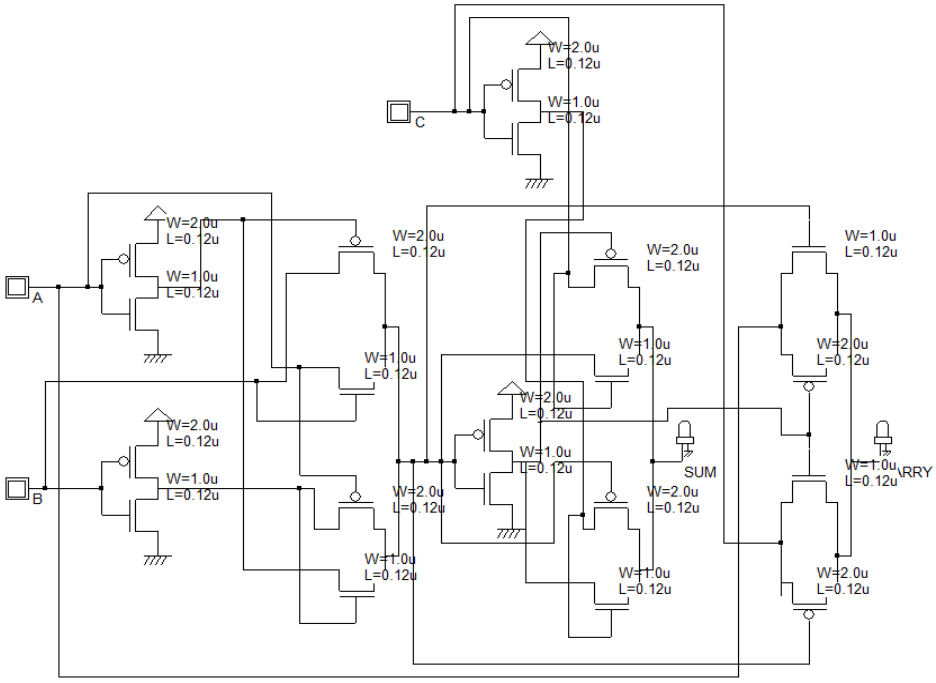


Fig .5. Xor-Xor Based Full adder

4.6 XNOR-XNOR BASED FULL ADDER WAVEFORM

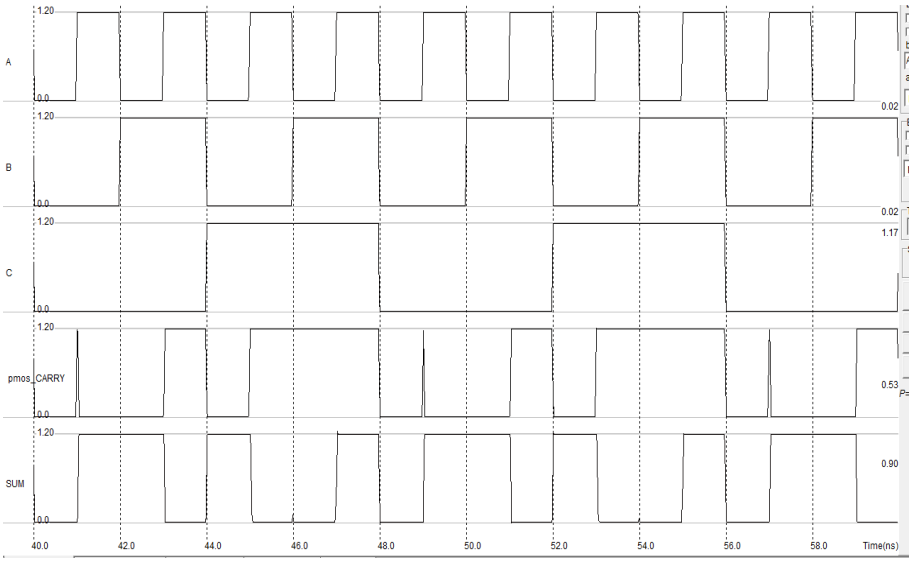
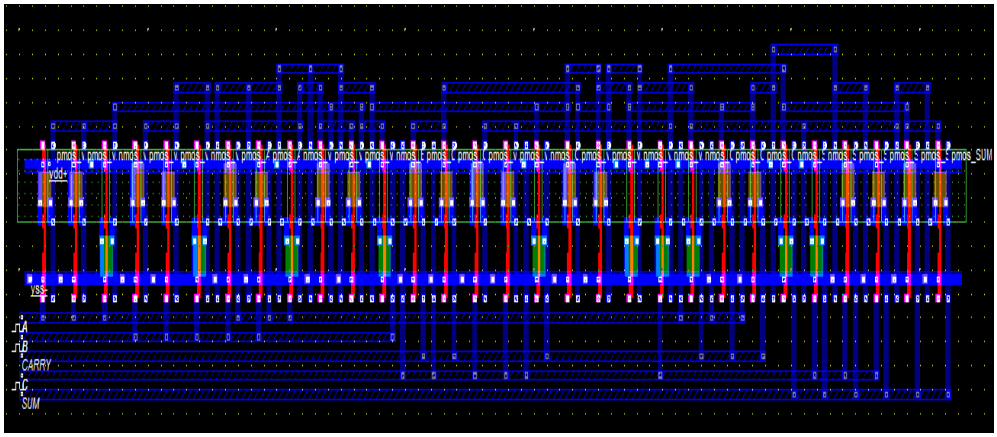


Fig.6. Xnor-Xnor based Full adder waveform

V. FULL ADDER LAYOUTS

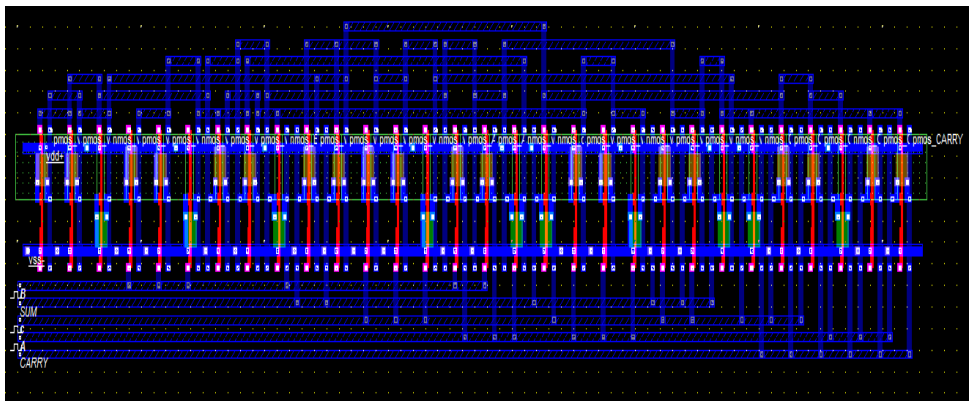
The area of these three full adder designs are calculted by designing the layout in Microwind 3.1.The verilog file which is generated by DSCH is compiled in microwind to get the Layout design.The technology used used for the layout is CMOS 0.12µm-6 Metal[16].

5.1 CENTRALIZED FULL ADDER LAYOUT



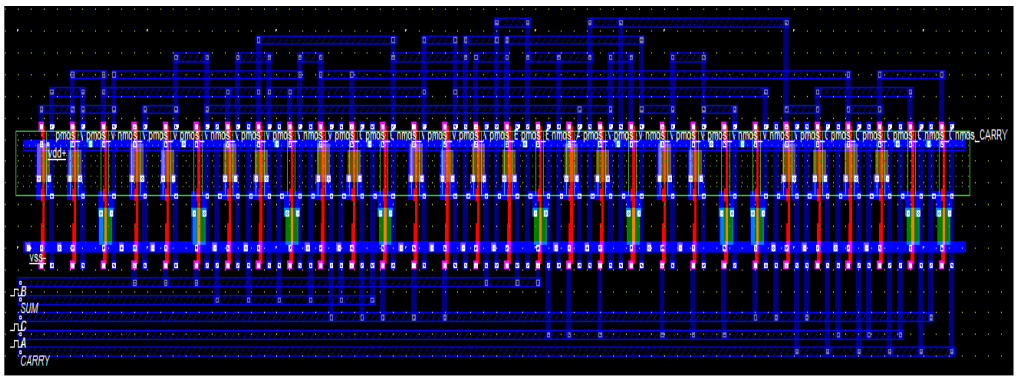
Width: 44.3µm (738 lambda)
Height: 8.9µm (148 lambda)
Surf area: 393.2µm^2

5.2 XOR-XOR BASED FULL ADDER LAYOUT



Width: 44.3µm (738 lambda)
Height: 9.4µm (156 lambda)
Surf area: 414.5µm^2

5.3 XNOR-XNOR BASED FULL ADDER LAYOUT



Width: 44.3µm (738 lambda)
Height: 9.4µm (156 lambda)
Surf area: 414.5µm^2

VI. SIMULATION RESULTS

The Performance of these three circuit is evaluted based on their Area, Power dissipation, Delay.All the simulations are performed using DSCH2.7 and Microwind 3.1.All the results are measured using the MOS Model Emprical Level 3 having different supply voltages like 0.8V, 1.20V, 1.80V and the operating Tempreture is 27°C.In the Emprical Level 3 the threshhold voltage is 0.4V, Gate oxide thickness 3nm and Lateral diffusion into channel is 0.01µm.In the simulation steps first of all design the Schematic of given circuit in DSCH2.7, After this make verilog file of this schematic circuit,then open the microwind 3.1 tool and compile this verilog file and genrate the layout and then simulate this layout to get the various parameters which are given below[16].
Table I shows the simulation results for 1-bit Full adders Performance comparison, regarding power dissipation, Propagation delay and PDP.All the full adders were supplied with differrent voltages(0.8V, 1.2V and 1.8V) and the maximum frequency for the inputs was 50MHz.

TABLE I : Simulation Results of Full Adders

Full Adder Scheme	AREA in	Supply Voltage(V)	Avg Power Diss. in µW	Propagation Delay in ps	PDP in µW.ps
CENTRALIZED	393.2µm2	0.8	6.803	89	605.4
		1.2	16.5	37	610.5
		1.8	47.543	23	1092.5
XOR-XOR BASED	414.5µm2	0.8	6.844	71	485.9
		1.2	16.734	32	534.4
		1.8	48.222	20	964
XNOR-XNOR BASED	414.5µm2	0.8	6.772	74	501.1
		1.2	16.951	33	559.3
		1.8	49.280	22	1084.16

From the results in Table –I we can state the following:

- The Power Dissipation increses with the increase of supply voltage.The table shows that there is a less power dissipation in the Centralized full adder than the other two approaches with the given supply voltages.
- With regards of speed,it can be seen that propagation delay of the Xor based type full adder design is less than the other designs. So, the speed of Xor based adder is more as compared to other designs.
- On regards of the implementation area obtained from the Layouts, it can be seen that the Centralized full adder require the smallest area as compared to other two approaches.which can also be considered as one of the factors for presenting lower delay and power consumption.
- The power delay product(PDP) coloums confirms the energy effeciency for the full adders built using these three logic circuits.From the results we can say that PDP is less in Xor-Xor based logic circuit.

VII. FUTURE WORK

In Recent years several variants of different logic styles have been proposed to implement 1-bit full adders. In this paper we have proposed the three designs of 1-bit full adders with different logic styles like Double Pass Transistor logic, which gives good performance on the basis of Area, Power dissipation, Propagation delay and Power delay product with different supply voltages. In these three designs full adders comprises of Xor, Xnor gates and multiplexers. Many types of logic design provide flexibility to work on CMOS area to overall performance of the circuit. Likewise we have used DPL logic; designer may use other logic to design the Xor and Xnor gates like CPL, SR-CPL to get better results of Power dissipation with less number of gates. Designers can be further design the Multipliers like array multiplier and tree multiplier using these three types of full adders. Moreover, a

slight improvement in area, power dissipation, and propagation delay and power delay product can create huge impact on the overall performance. As different application can be generated using this different modules, designers should take a good look at the power consumption at different input voltage. Another important concern for designing circuits is delay. Decrease of delay and low input voltage might have an impact on the speed of overall circuits. Due to this reason delay is another area where designer can work in future. Designer may use the Tanner Tool(S-edit, T-Spice) [17] for Schematic designs and Simulation or designers may use Microwind Tool to design Layouts of schematics and to calculate the area.

VIII. CONCLUSION

An alternative internal logic structure for designing full-adder cells was introduced. In order to demonstrate its advantages, three full-adders were built. They were designed with a DSCH & Micro wind 3.1 with 120nm CMOS technology, and were simulated and compared against Power dissipation, Propagation delay, and Area & Power delay Product (PDP).The simulation shows the power savings are more in case of Centralized full adder; also centralized full adders are area efficient. But with respect to the delay and Power delay product the Xor-Xor based full adders are more reliable. So if we want the more speed of the circuit we can use Xor-Xor based circuit for full adder. The power-supply voltage for the proposed full-adders can be lowered down to 0.8 V, maintaining proper functionality.

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