AN INVERTED SINE PWM SCHEME FOR NEW ELEVEN LEVEL INVERTER TOPOLOGY

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ABSTRACT

This paper demonstrates reduced harmonic distortion can be achieved for a new topology of multilevel inverters with Inverted sine PWM. The new topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter, and can be extended to any number of levels. The modes of operation are outlined for 5-level inverter, as similar modes will be realized for higher levels. Simulation of different number of levels of the proposed inverter topology, this paper focuses on PD based inverted sine PWM technique for a eleven-level inverter. ISPWM has a better spectral quality and a higher fundamental voltage compared to the triangular based PWM Simulation of different number of levels of the proposed inverter topology along with corroborative experimental results are presented

KEYWORDS: *Multilevel Inverter, harmonic elimination Inverted sine PWM, THD.*

I. INTRODUCTION

Multilevel inverter is an effective and practical solution for increasing power demand and reducing harmonics of AC waveforms. Function of a multilevel inverter is to synthesize a desired voltage wave shape from several levels of DC voltages. As the number of levels increase, the synthesized staircase output waveform has more steps, approaching the desired sinusoidal waveform. They are of special interest in the distributed energy sources area because several batteries, fuel cell and solar cell can be connected through multilevel inverter to feed a load [1].

The principal function of multilevel inverters is to synthesize a desired ac voltage from several separate dc sources, which may be obtained from batteries, fuel cells, or solar cells [2]. The desired output voltage waveform can be synthesized from the multiple voltage levels with less distortion, less switching frequency, higher efficiency, and lower voltage devices. With an increasing number of dc sources, the inverter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency switching scheme. While many different multilevel inverter topologies have been proposed, the two most common topologies are the cascaded H-bridge inverter and its derivatives [3], and the diode-clamped inverter [4]. The main advantage of both topologies is that the rating of the switching devices is highly reduced to the rating of each cell. However, they have the drawback of the required large number of switching devices which equals $2(k\text{-}1)$ where k is the number of levels. This number is quite high and may increase the circuit complexity, and reduce its reliability and efficiency. Cascaded H-bridge inverter has a modularized layout and the problem of the dc link voltage unbalancing does not occur, thus easily expanded to multilevel. Diode-clamped inverter needs only one dc-bus and the voltage levels are produced by several capacitors in series that divide the dc bus voltage into a set of capacitor voltages. Balancing of the capacitors is very complicated especially at large number of levels. Moreover, three-phase version of this topology is difficult to implement due to the neutral-point balancing problems

The performance of the modulation control schemes for the multilevel inverter can be divided into two categories fundamental switching frequency and high switching frequency PWM. The high frequency PWM is classified as multilevel carrier-based PWM and multilevel space vector PWM [5]. The most popular and simple high frequency switching scheme for MLI is the Multi-Carrier PWM (MCPWM). It can be categorized into two groups: Carrier Disposition (CD) methods and Phase Shifted (PS) methods [6]. Among the carrier disposition methods, Phase Disposition (PD) PWM technique is normally employed for MLI as the carriers need minimal amounts of alteration since they are all in phase with each other [7]. This paper focuses on PD based inverted sine PWM technique for a eleven-level inverter. ISPWM has a better spectral quality and a higher fundamental voltage compared to the triangular based PWM.

II. MULTILEVEL INVERTER NEW TOPOLOGY

In order to reduce the overall number of switching devices in conventional multilevel inverter topologies, a new topology has been proposed. The circuit configuration of the new 5 -level inverter is shown in Fig.1. It has four main switches in H-bridge configuration Q1~Q4, and four auxiliary switches Q5, Q6, Q7 and Q8. The number of dc sources (*two*) is kept unchanged as in similar 5-level conventional cascaded H-bridge multilevel inverter. Like other conventional multilevel inverter topologies, the proposed topology can be extended to any required number of levels. The inverter output voltage, load current, and gating signals are shown in Fig.2. The inverter can operate in three different modes according to the polarity of the load voltage and current. As these modes will be repeated irrespective of the number of the inverter levels, and for the sake of simplicity, the modes of operation will be illustrated for 5-level inverter, these modes are:

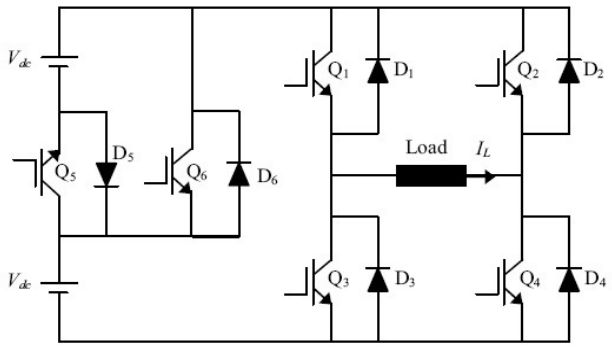


Fig 1 : The 5-level inverter of the new topology

Powering Mode

This occurs when both the load current and voltage have the same polarity. In the positive half cycle, when the output voltage is *Vdc*, the current pass comprises; the lower supply, D6, Q1, load, Q4, and back to the lower supply. When the output voltage is *2Vdc*, current pass is; the lower source, Q5, the upper source, Q1, load, Q4, and back to the lower source. In the negative half cycle, Q1 and Q4 are replaced by Q2 and Q3 respectively.

Free-Wheeling Mode

Free-wheeling modes exist when one of the main witches is turned-off while the load current needs to continue its pass due to load inductance. This is achieved with the help of the anti-parallel diodes of the switches, and the load circuit is disconnected from the source terminals. In this mode, the positive half cycle current pass comprises; Q1, load, and D2 or Q4, load, and D3, while in the negative half cycle the current pass includes Q3, load, and D4 or Q2, load, and D1.

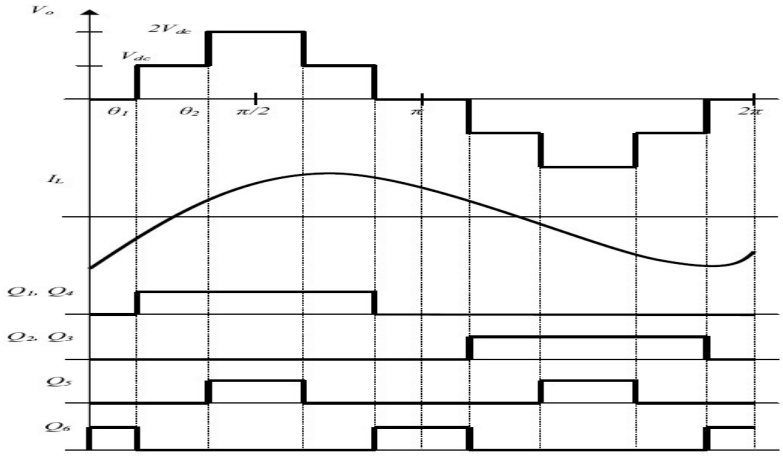


Fig 2 : Waveforms of the proposed 5-level inverter

Regenerating Mode

In this mode, part of the energy stored in the load inductance is returned back to the source. This happens during the intervals when the load current is negative during the positive half cycle and vice-versa, where the output voltage is zero. The positive current pass comprises; load, D2, Q6, the lower source, and D3, while the negative current pass comprises; load, D1, Q6, the lower source, and D4.
A generalized circuit configuration of the new topology is shown in Fig.5. The proposed topology has the advantage of the reduced number of power switching devices, but on the expense of the high rating of the main four switches. Therefore, it is recommended for medium power applications.

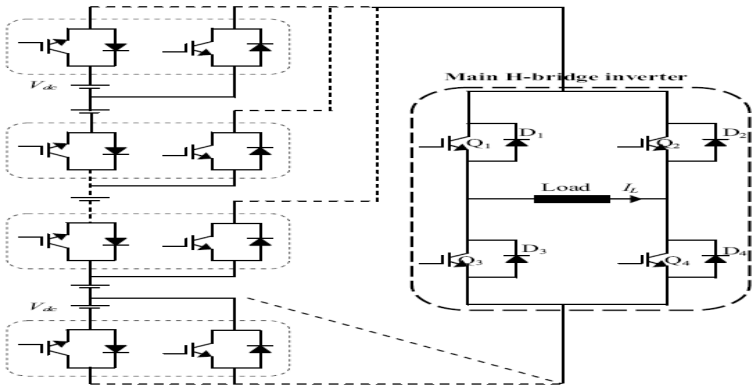


Fig 3 : Generalized multilevel inverter configuration of the new topology

The percentage reduction in the number of power switches compared to conventional H-bridge multilevel inverter is shown in Table 1.

Table 1: Percentage reduction in switching devices

	Number of Switches			
Inverter Type	5- level	7- level	9- level	11- level
Cascaded H Bridge	8	12	16	20
Proposed Topology	6	8	10	12
% Reduction	25 %	33.3%	37.5%	40%

III. MATHEMATICAL METHOD OF SWITCHING

In order to verify the ability of the proposed multilevel inverter topology to synthesize an output voltage with a desired amplitude and better harmonic spectrum, programmed PWM technique is applied to determine the required switching angles. It has been proved that in order to control the fundamental output voltage and eliminate n harmonics, therefore n+1 equation is needed. Therefore, 11-level inverter, for example, can provide the control of the fundamental component beside the ability to eliminate or control the amplitudes of two harmonics, not necessarily to be consecutive. The method of elimination will be presented for 11-level inverter such that the solution for three angles is achieved.

The Fourier series expansion of the output voltage waveform using fundamental frequency switching scheme shown in Fig.2 is as follows:

$$V(\omega t) = \left(\frac{4VDC}{\pi}\right) \Sigma \left[\cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_s)\right] \sin(n\omega t) \quad \text{where } n = 1, 3, 5, 7,.. \qquad (1)$$

The conducting angles θ_1, θ_2, θ_3,…, θ_s can be chosen such that the voltage total harmonic distortion is a minimum. Normally, these angles are chosen so as to cancel the predominant lower frequency harmonics [8], [9]. For the 11-level case in Fig. 2,the 5th, 7th, 11th, and 13th harmonics can be eliminated with the appropriate choice of the conducting angles The switching angles can be found by solving the following equations

$$\left.\begin{aligned}
&\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4)) + \cos(\theta_5) = 5m_a \\
&\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4)) + \cos(5\theta_5) = 0 \\
&\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4)) + \cos(7\theta_5) = 0 \\
&\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) = 0 \\
&\cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4)) + \cos(\theta_5) = 0
\end{aligned}\right\} \qquad (2)$$

Where m=V1/(4Vdc/π), and the modulation index ma is given by ma=m/s, where $0 \leq m_a \leq 1$

One approach to solving the set of nonlinear transcendental equations (2), is to use an iterative method such as the Newton-Raphson method [10]. In contrast to iterative methods, the approach here is based on solving polynomial equations using the theory of resultants which produces all possible solutions [11]. The set of nonlinear transcendental equations can be solved by an iterative method such as the Newton–Raphson method. For example, using a modulation index of 0.9 obtains

$$\theta_1 = 6.57^\circ, \theta_2 = 18.94^\circ, \theta_3 = 27.18^\circ, \theta_4 = 45.15^\circ, \theta_5 = 62.24^\circ.$$

This means that, if the inverter output is symmetrically switched during the positive half cycle of the fundamental voltage to $+V_{dc}$ at 6.57 , $+2V_{dc}$ at 18.94 , $+3V_{dc}$ at 27.18 , $+4V_{dc}$ at 45.14 , and $+5V_{dc}$ at 62.24 , and similarly in the negative half cycle to $-V_{dc}$ at 186.57 , $-2V_{dc}$ at 198.94 , $-3V_{dc}$ at 207.18 , $-4V_{dc}$ at 225.14 , $-5V_{dc}$ and at 242.24 , the output voltage of the 11-level inverter will not contain the 5th, 7th, 11th, and 13th harmonic components.

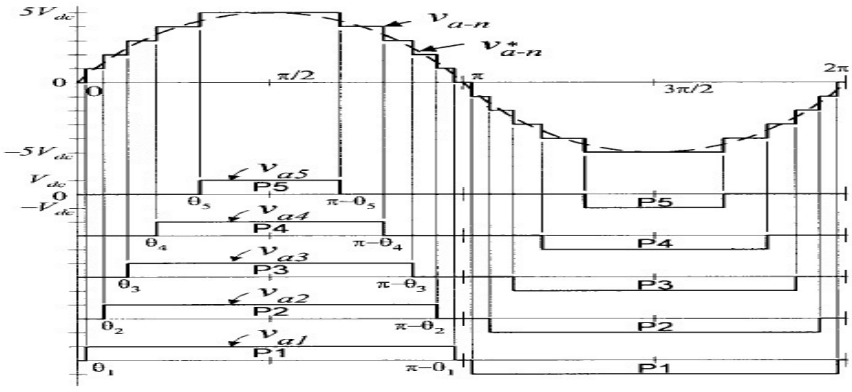


Fig 4: Waveforms and switching method of the 11-level cascade inverter

IV. INVERTED SINE PWM TECHNIQUE FOR MLI

The inverted sine carrier PWM (ISPWM) method uses the conventional sinusoidal reference signal and an inverted sine carrier. The control strategy uses the same reference (synchronized sinusoidal signal) as the conventional SPWM while the carrier triangle is a modified one. The control scheme uses an inverted (high frequency) sine carrier that helps to maximize the output voltage for a given modulation index [12-15]. In the gating pulse generation of the proposed ISCPWM scheme, the triangular carrier waveform of SPWM is replaced by an inverted sine waveform. In Fig.5 shows the pulse generation circuit for a single phase of the multilevel inverter in which a sine wave (modulating signal) of fundamental frequency is compared with high frequency phase disposed inverted sine carrier waves. For an 'm' level inverter, (m-1) carrier waves are required. The pulses are generated when the amplitude of the modulating signal is greater than that of the carrier signal. The proposed control strategy has a better spectral quality and a higher fundamental output voltage without any pulse dropping.

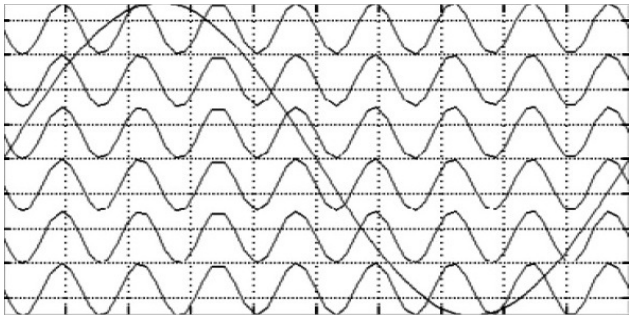


Fig 5: Carrier and Reference waveforms for ISPWM technique

The advantages of ISPWM method are it has a better spectral quality and a higher fundamental component compared to the conventional sinusoidal PWM (SPWM) without any pulse dropping. The ISCPWM strategy enhances the fundamental output voltage particularly at lower modulation index ranges□□There is a reduction in the total harmonic distortion (THD) and switching losses To increase the fundamental amplitude in the sinusoidal pulse-width modulation the only way is by increasing the modulation index beyond 1 which is called over modulation. Over modulation causes the output voltage to contain many lower order harmonics and also makes the fundamental component vs. modulation index relation non-linear. Inverted sine pulse width modulation technique replaces over modulation [16].The appreciable improvement in the total harmonic distortion in the lower range of modulation index attracts drive applications where low speed operation is required. ISPWM technique causes marginal increase in the lower order harmonics, but except third harmonic all other harmonics are in acceptable level. But for three phase applications the heightened third harmonics need not be bothered [17-20].

V. SIMULATION RESULTS

The feasibility of the proposed approach is verified using computer simulations. A model of the eleven-level inverter is constructed in MATLAB-Simulink. **A** new strategy with reduced number of switches is employed. For cascaded H Bridge 11 level inverter requires 20 switches 6 to get eleven level output voltage and with the proposed topology requires 12 switches. The new topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter. The Proposed topology reducing the harmonics using Inverted Sine PWM model PD technique is used for generating the pulses is shown in fig. 6. For the gate pulse generation the proposed requires carriers as sine as shown in fig 7 and the comparison of both carrier and reference signal as shown in fig.8, results pulses generation and hence it control the inverter The generated output pulses from the Inverse Sine PWM block as shown in the Fig.6 and those pulses generated are in eight numbers which is required to drive the devices in to ON state with the aid of Inverted Sine PWM converter blocks

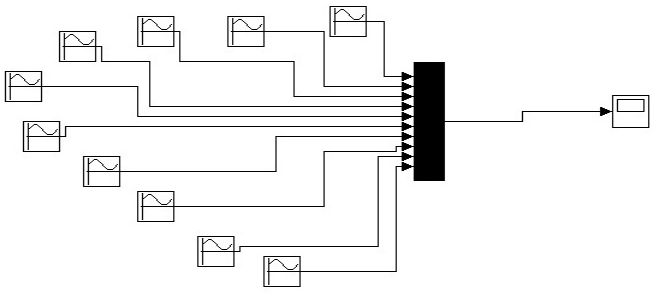


Fig: 6 Inverted Sine PWM signal generation

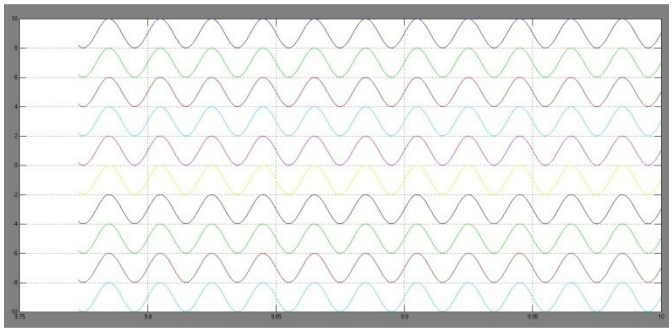


Fig: 7 Carrier Signal

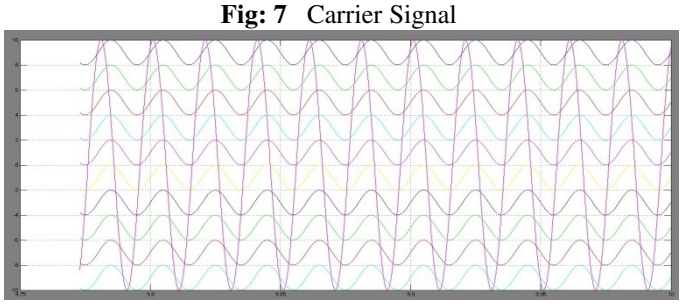


Fig: 8 Carrier and Reference signals

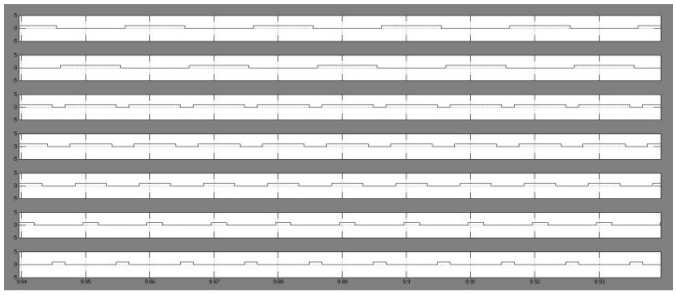


Fig: 9 Generated Gate pulses

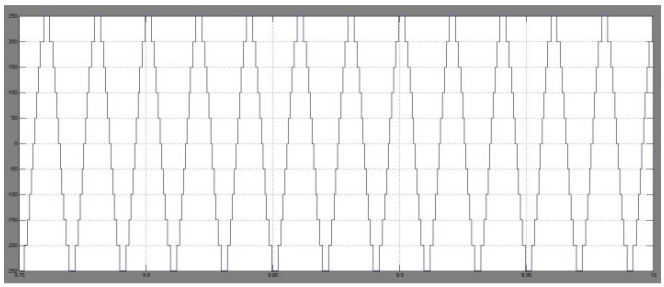
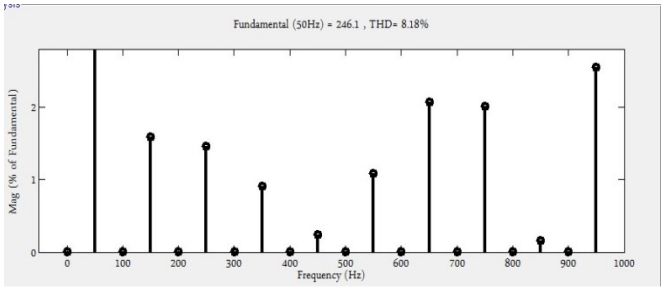


Fig. 10 Output Voltage of Eleven Level Inverter



Fig, 11 Harmonic spectrum of the simulated output

The switching patterns adopted are applied for the proposed topology and switches to generate seven output voltage levels at 0.9 modulation index and the switching pattern are shown in the Fig.9 Simulation results for 7-level inverter at Vdc=50Vs, ma=0.9 where s=5 and corresponding output voltages for proposed eleven level inverter are shown in Fig 10 The proposed topology has the advantage of its reduced number switches and harmonics are reduced with THD value of 8.18 at 246.1V is achieved. For proposed harmonic spectrum of the simulation system is as shown in the fig.11, which shows the results are well within the specified limits of IEEE standards. The results of both output voltage and FFT analysis are verified by simulating the main circuit using MATLAB

VI. CONCLUSION

A new family of multilevel inverters has been presented and built in MATLAB-Simulink. It has the advantage of its reduced number of switching switches compared to conventional similar inverters. However, a Inverted Sine PWM is implemented for generation of pulses and based on the theory of resultant has been applied for harmonic elimination of the new topology. The Inverse Sine PWM strategy reduces the THD and this strategy enhances the fundamental output voltage. When Modulation Index is equal to 1 by adopting Inverted Sine PWM strategy the THD value is reduced to 8.18. Those schemes confirmed by simulation results. This proposed prototype can be extended to m-level inverter. Other PWM methods and techniques are also expected to be successively applied to the proposed topology. The simulation results and experimental results show that the algorithm can be effectively used to eliminate specific higher order harmonics of the new topology and results in a dramatic decrease in the output voltage THD

VII. FUTURE WORK

- The proposed topology focused on the Inverter Sine PWM method and this method can be applied to different voltage levels, other modulation techniques and similarly other PWM techniques can be applied.
- Also if the comparison is done from an economical point of view, it gives a better picture in construction in reduction in circuit complexity, requiring a less number of power switches in industrial application
- Another interesting topic that can be studied in the modeling and control of multilevel inverters in FACTS devices application, HVDC transmission lines and large wind turbine applications

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