# DESIGN OF FIRST ORDER AND SECOND ORDER SIGMA DELTA ANALOG TO DIGITAL CONVERTER

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***ABSTRACT***

*This paper presents the design of a first order and second order single bit Sigma-Delta Analog-to-Digital Converter (ADC) which is realized using CMOS technology. In this paper, a first Order and Second order Sigma-Delta ADC is designed which accepts an input signal of frequency 1 KHz, an OSR of128, and 256 KHz sampling frequency .It is implemented in a standard 90nm CMOS technology. The ADC operates at 0.5V reference voltage. The Design and Simulation of the Modulator is done using H-spice. This paper firstly elaborates Summer, Integrator, Comparator, D-Latch and DACwhich is integrated together to form Sigma Delta Modulator. Op-amp which is a key componentused in the design, has the open loop voltage gain of 80.5db, Phase Margin of 66 Degree, output resistance of 122.5KΩ, and power dissipation of 0.806 mW. Finally, a first order and second order single bit Sigma Delta ADC is implemented using ±2.5 power supply and simulation results are plotted using H-Spice .After the modulator is designed, the output pulse train of the modulator is transferred from H-spice to MatlabWorkspace [1].The Power Spectral density of both the Modulators are plotted andfinally the decimationis done using CIC filter[4].*

***KEYWORDS:*** *Op-amp, FirstOrder Modulator, Second Order Sigma Delta Modulator, CIC Filter, PSD.*

## I. INTRODUCTION

A sigma–delta modulator is one method for providing the front end to an analog to digital converter. When an analog signal is digitized, quantization error is introduced into the frequency spectrum. The sigma–delta's function is to push the quantization error that is near the signal into a higher frequency band near the sampling frequency. After this is done the signal can be low pass filtered and the original signal can be restored in a digitized form .The sigma–delta modulator with first order and second order noise shaping characteristics is designed . The block diagram of the first order and second order loop is shown in Figure1 and 2.

In the sigma–delta modulator, the difference between the analog input signal and the output of the DAC is the output of the Summer. Thisdifference is given as aninput to the Integrator. The integrator integrates over each clock period. The clock is at a much higher frequency than the input sinusoid, causing the sine wave to be approximately flat over the clock period. The integration of the pulse difference is linear over one clock period. The output of the integrator represents an accumulation of the error term between the input and the DAC output [3].

This integral then digitized by a clocked quantizer, and the quantizer output is the output of the sigma–delta modulator. In the feedback path, the DAC shifts the logic level so that the feedback term matches the logic level of the input; making the difference equally weighted. The transient output of the sigma–delta modulator is a pulse density modulated signal that represents the input sine wave. This waveform is more dense with digital ones when the signal represented is high and less dense when the waveform is low.The three main

performance measures of an ADC are its resolution (usually number of bits), its speed (how many conversions it does per second), and its power consumption, where customarily it is desired that the first two of these be maximized and the third minimized [6].
A second order sigma-delta modulator can be derived by placing two integrators in series as shown in Figure 2. The operation of the second order modulator blocks is similar to that of the first order modulator except that the integration is performed twice on the data.

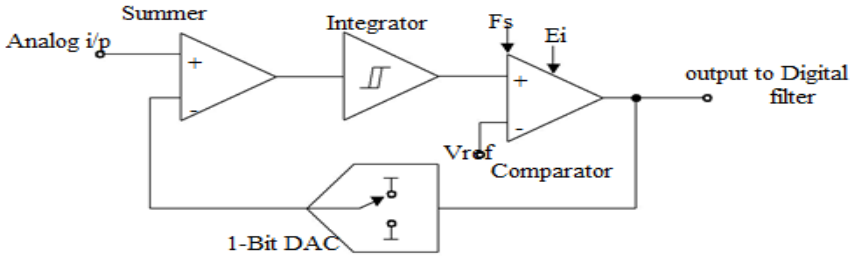


**Fig 1:** Block diagram of 1st order sigma-delta modulator

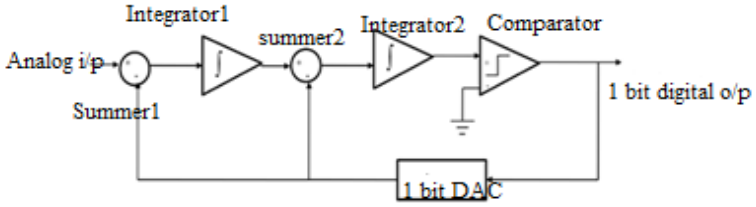


**Fig 2:** Block diagram of 2nd order sigma-delta modulator

### 1.1 Decimator Overview

Decimation is a technique used to reduce the number of samples in a discrete-time signal .The process of decimation is used in a sigma-delta converter to eliminate redundant data at the output [4]. In practice, this usually implies low pass filtering a signal and then down sampling to decrease its effective sampling rate. The function of the digital filter in a sigma-delta ADC is to attenuate the out of band quantization noise and signal components that are pushed out to the higher frequencies by modulator.
Section 2 of this paper provides a brief description of the system and analysis of op-amp used in the design.Section3 provides the detail about design of sub-circuit in H-spice.Section4 shows the simulation and Decimation of the Modulator output that is transferred from H-spice to Matlab Workspace.Section5 lists the analysis of the result with section 6 concluding the paper.

### 1.2 Methodology

In this present work, the aim is focused on designing a first and second order sigma Delta ADC.The methodology can be divided into three major parts: Study of related Areas, modeling of the modulator in H-spice,modeling the decimated output and simulating the Power Spectral Density in Matlab.

## II. SYSTEM DESIGN AND SIMULATION

At each stage, we get different output. First we add up the original signal and negative adjusted pulse output of D Flip-flop, after passing through a DAC. Then, we integrate the difference of this stage, and quantize the result. We get result of 0 and 1 output signal representing a sinusoidal waveform. We get more 0/1 oscillation in the center of input range, more 1 when input is high and more 0 when input is low.

**PerformanceAnalysis of Op-amp:**

Open-loop gain-80.5dB

Phase Margin 66degree

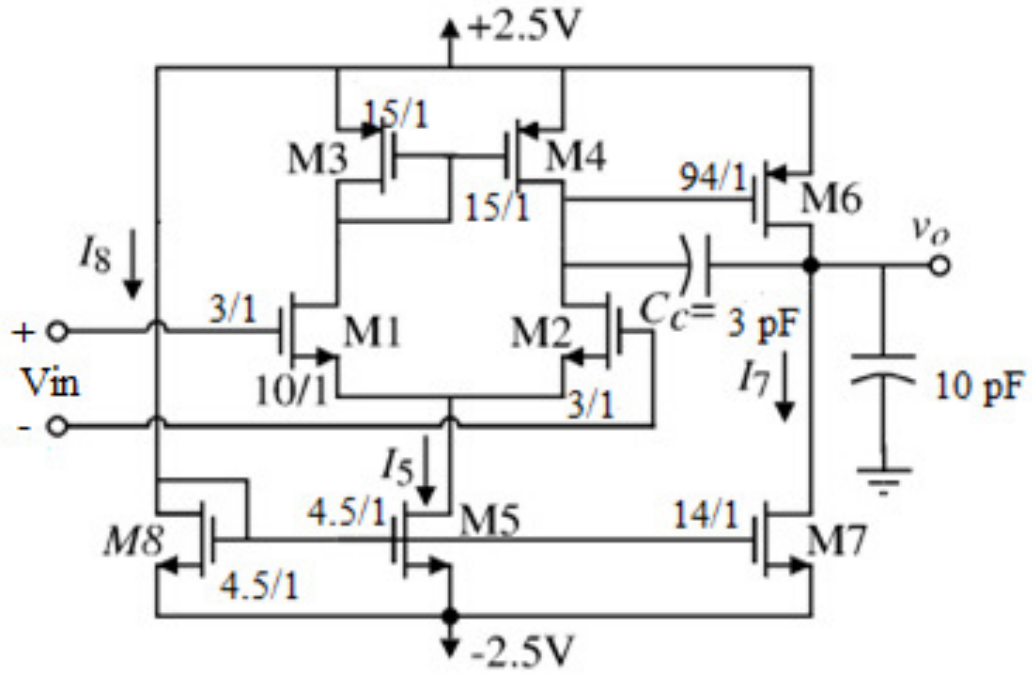


**Fig 3:** Design Of Two Stage Op-amp

The operational amplifier that the integrator uses must have high gain to effectively carry out a smooth integration, as well as a large enough bandwidth to support the high frequency square waves that it will be integrating[5]. The amplifier used is shown in Figure 3.

## III. DESIGN OF SUB CIRCUITS

The whole system consists of a summer, an integrator, a comparator, D Latch and DAC, which were designed and simulated in H-spice. Each component is discussed below with its simulation verification.

### 3.1 Summer

The summer was simulated using H-Spice, and was found to function correctly. The simulation results for the summer are shown below. The first simulation test on the summer was done using a DC voltage of 1V as an input at the positive terminal, and a sine wave with amplitude of 1V and centered at 2.5V as an input to negative terminal. The simulation result for the summer is shown in Figure 4.The second simulation at the Summer was done taking sine wave at both the inputs as shown in figure 5.

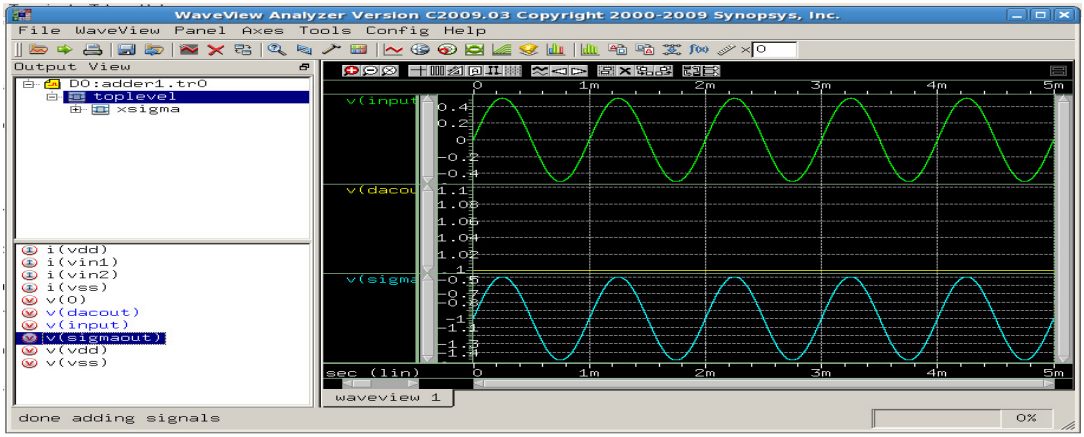


**Fig 4:**Output of Summer for a DC voltage of 1V and a sine wave of 0.5V

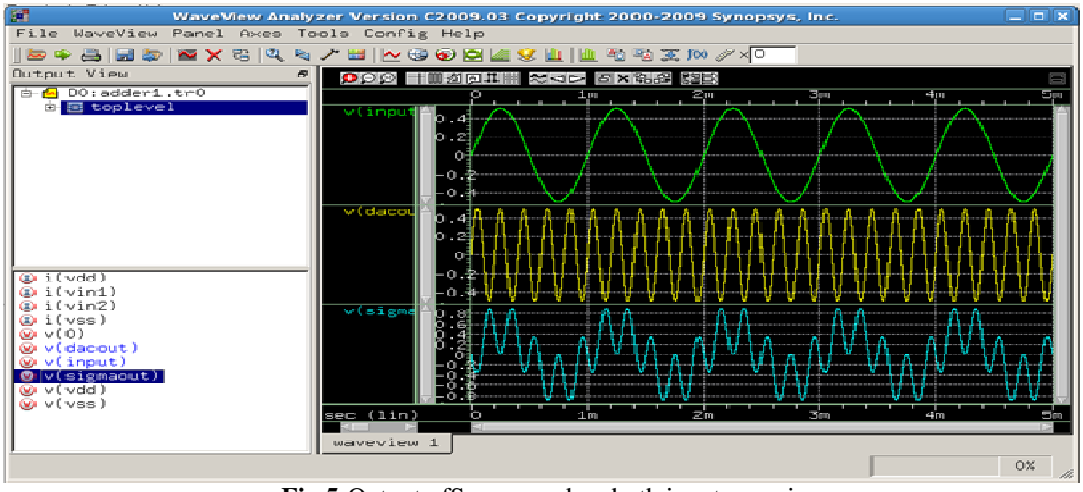


**Fig 5:**Output ofSummer when both inputs are sine wave.

## 3.2Integrator

The loop gain for this circuit is not crucial, but it is necessary that the gain of the integrator is small enough so that the device does not saturate or run into the positive or negative rails. To achieve a gain of one, the integrator gain factor T/RC is formed from time domain analysis, and set to one.The integrator used a capacitance of 1n to make its working robust. It was tested using a pulse input. The simulation results are shown in Figure 6below. The integrator is able to handle the input pulse and integrates it to a fairly clean triangular wave.

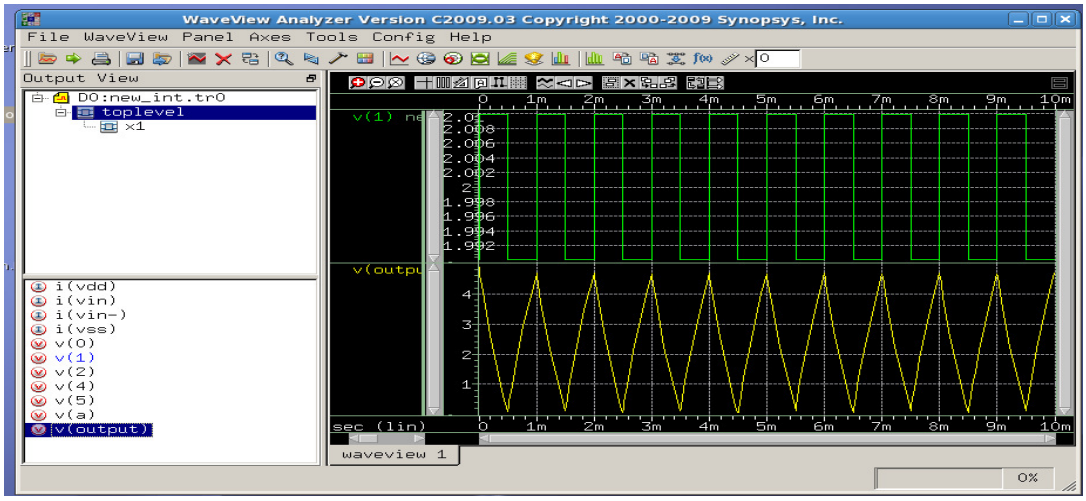


**Figure 6:** Output ofIntegrator fora pulse input

### 3.3Comparator

The comparator simulations are relatively simple to perform. The comparator is set up so the threshold is 0 volts. This was done by grounding the inverting input. When a sine wave is input to the circuit, the comparator switches from positive rail to negative rail. The propagation delay of the comparator is found to be 5ns.

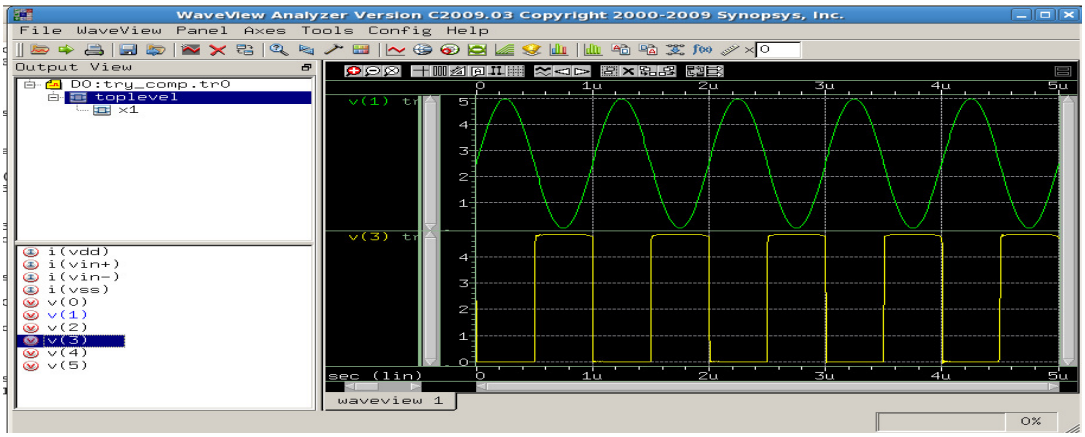


**Fig.7:** Simulation of Comparator

### 3.4 Latch Simulations

To test the D flip–flop, the input signal used was a square wave with a frequency less than that of the clock. To verify the correct operation of the Latch, the input, output and clock signal were analyzed. The Latch was found to work properly because the input was passed on the rising edge of the clock and held while the clock was high and did not passon any other clock transitions.

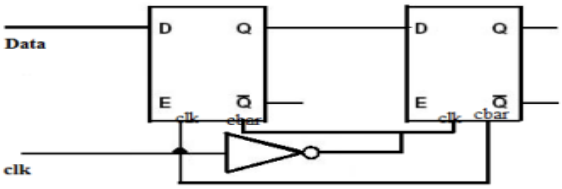


**Figure 8a:** Block Diagram of D-Latch

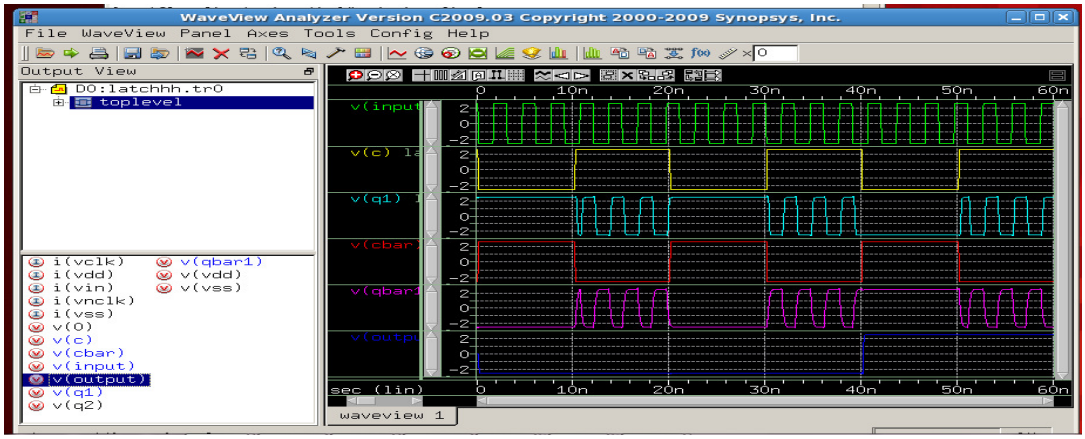


**Fig 8b:** Simulationof D-Latch

### 3.5 Modulator Simulation in H-Spice

When all the components were combined together the complete system simulation gave the desired result. The simulation result for sine wave is shown below. Thewaveform shows the output of each stage in the complete system simulation, starting with the input, followed by integrator output, comparator output, and DAC output and finally Latch output (which is the same as the system output).

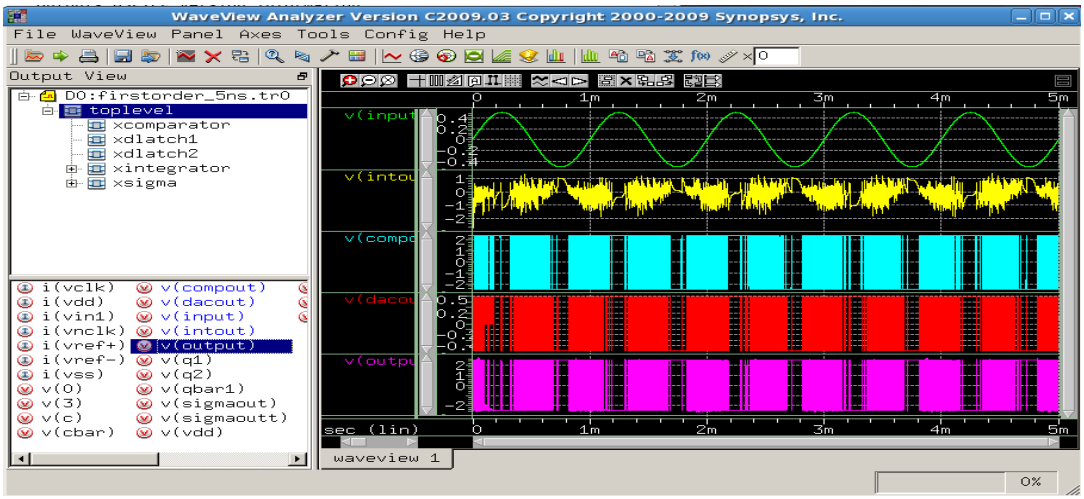


**Fig 9:**Step by Step Performance of First Order Modulator

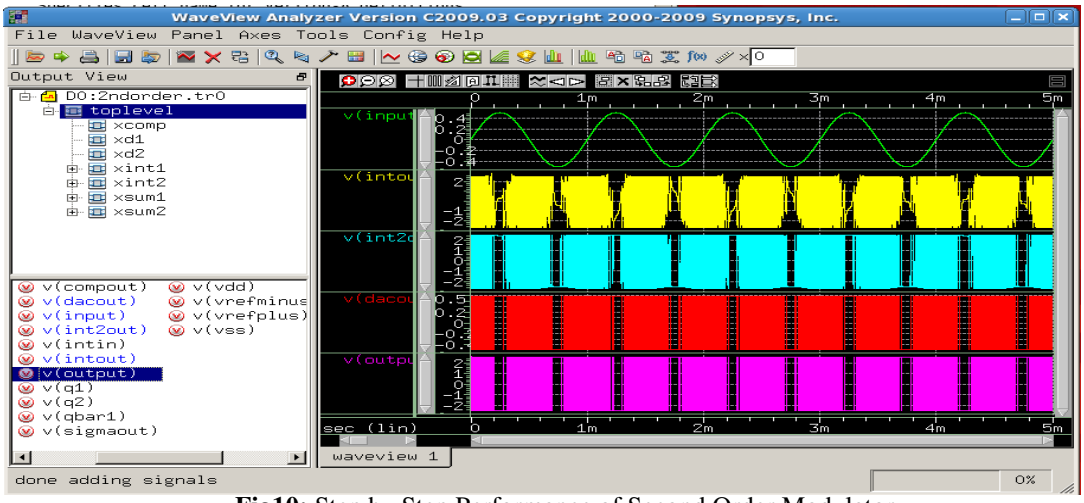


**Fig10:** Step by Step Performance of Second Order Modulator

## IV. MATLAB SIMULATION

For Further processing, the output of First order and Second Modulator is transferred from H-Spice to Matlab Workspacefor Plotting its Power Spectral Density Spectrum and finding the SNR.

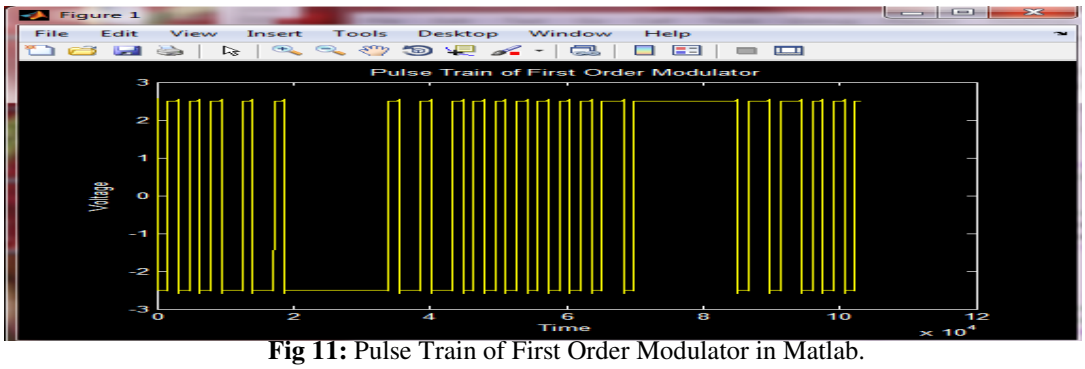


**Fig 11:** Pulse Train of First Order Modulator in Matlab.


**Fig 12:** Decimated Output of First Order Modulator.

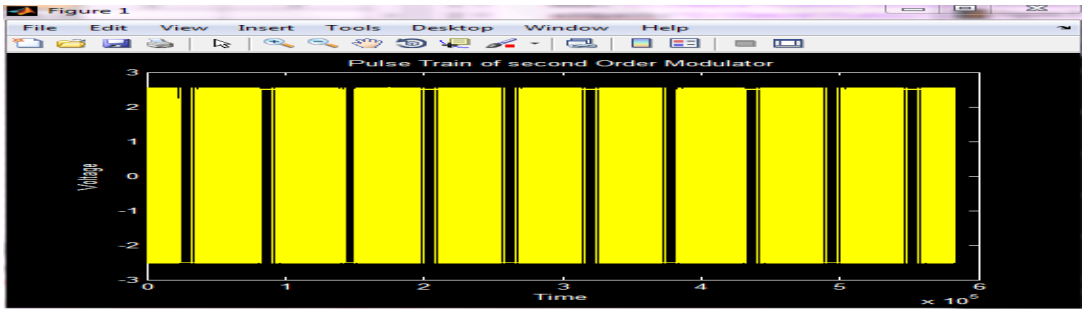


**Fig 13**: Pulse Train of Second Order Modulator in Matlab.

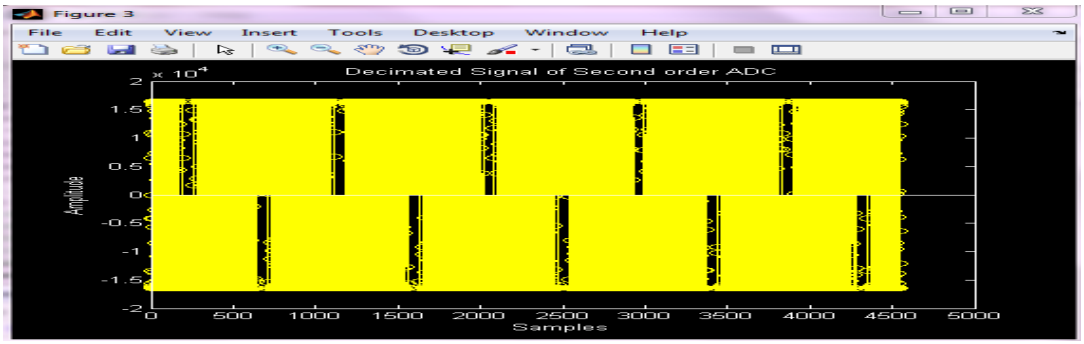


**Fig 14:** Decimated Output of Second Order Modulator.

Power Spectral Density of the Modulator output is plottedby taking its FFT and using the HanningWindow. It is found that the SNR of Second order is higher than the SNR of first order.

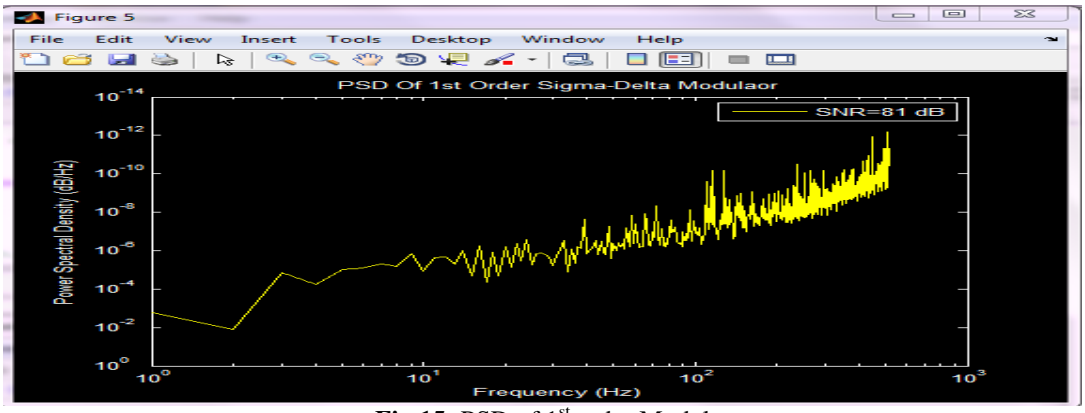


**Fig 15:** PSD of 1st order Modulator

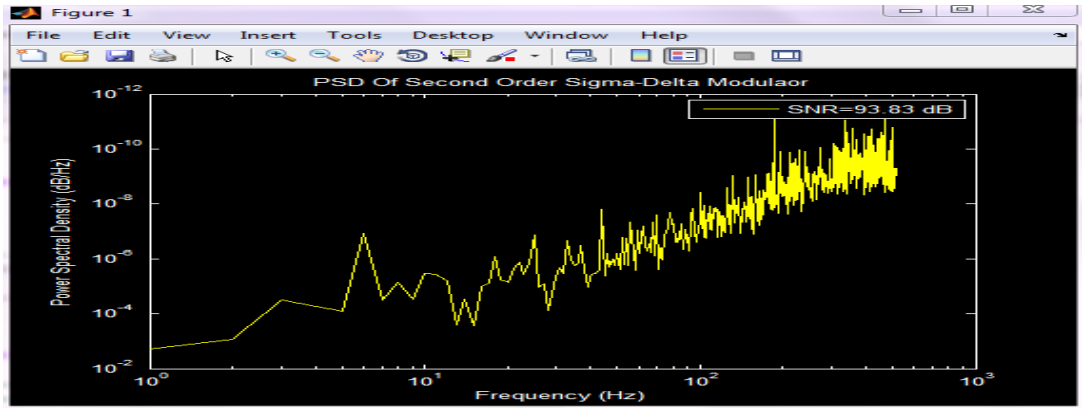


**Fig 16:** PSD of 2nd order Modulator

## V. ANALYSIS OF RESULTS

### Performance Summary

**Table 1:** Performance Summary

| **Parameters** | **Value** |
|---|---|
| Supply Voltages | 2.5V |
| Sampling Frequency | 256 KHz |
| Signal Bandwidth | 1Khz |
| Full Scale Input Signal | 1 $V_{p-p}$differential |
| Open Loop Gain of Op-amp | 80.5 dB |
| Propagation Delay Of Comparator | 5 ns |
| Capacitor Value of Integrator | 1nF |
| SNR of first Order Modulator | 81dB |
| SNR of Second Order Modulator | 93.83dB |
| ENOB of first Order Modulator | 13.16 bits |
| ENOB of second Order Modulator | 15.29 bits |
| In-band noise in 1st Order Modulator | 7.71 μ$V_{rms}$ |
| In-band noise in 2nd Order Modulator | .025 μ$V_{rms}$ |
| Oversampling Ratio | 128 |
| Dynamic Range of 1st Order Modulator | 99 dB |
| Dynamic Range of 2nd Order Modulator | 140 dB |

Delta-sigma modulation is a technique that i) combines filtering and oversampling to perform analog-to-digital conversion.ii)The noise from a low resolution quantizer is shaped away from the signal band prior to being removed by filtering.iii) Performance of a modulator is determined by taking the spectrum of a sequence of output bits generated from time-domain simulation of the modulator. (iv)It is characterized with some of the usual ADC performance measures such as DR and SNR.

## VI. CONCLUSION

This project primarily aims to demonstrate the design of First order and second ordersigma-delta ADCtoadapttomultiplecommunicationsstandards.The simulated parameter for first and second Order Modulators using an integrator of capacitance 1nF and a Comparator with a propagation delay of 5 nsecare shown below.

**Table 2:** Simulated Parametric Value

| Parameter | First Order Modulator | Second Order Modulator |
|---|---|---|
| SNR | 81dB | 93.83 dB |
| ENOB | 13 bits | 15bits |
| DR | 99 dB | 140 dB |

### 6.1 Future Work:

The area which will be of interestis optimizing the power distribution among the various blocks: (1) continuous-time analog filter preceding the ADC, (2) the ADC, and (3) the digital filter following the ADC should be explored.

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**AuthorBiography**

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