SCALABLE PARALLEL COUNTER ARCHITECTURE BASED ON STATE LOOK-AHEAD LOGIC

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ABSTRACT

This paper presents a high- speed and wide-range parallel counter that achieves high operating frequencies through a pipeline partitioning methodology (a counting path and state look-ahead path), using only three simple repeated module types: an initial module generates anticipated counting states for higher significant bit modules through the state look-ahead path , simple D-type flip-flops, and 2-bit counters. The state look-ahead path prepares the counting path's next counter state prior to the clock edge such that clock edge triggers all modules simultaneously, thus concurrently updating the count state with a uniform delay at all counting path modules/stages with respect to the clock edge. The structure is scalable to arbitrary N-bit counter widths using only the three modules types and no fan-in or fan-out increase. The proposed architecture is verified by verilog HDL in ModelSim.

KEYWORDS-*Architecture design, parallel design, pipeline counter design.*

I. INTRODUCTION

Counters are widely considered as essential building blocks for a variety of circuit operations [1],[3] such as programmable frequency dividers, shifters, code generators, memory select management, and various arithmetic operations. Since, many applications are comprised of these fundamental operations; much research focuses on efficient counter architecture design. Counter architecture design methodologies explore tradeoffs between operating frequency, power consumption, area requirements, and target application specialization. Early design methodologies improved counter operating frequency by partitioning large counters into multiple smaller counting modules, such that modules of higher significance(containing higher significant bits) were enabled when all bits in modules of lower significance(containing lower significant bits) saturate. Initializations and propagation delays such as register load time, AND logic chain decoding, and the half incrementer component delays in half adders dictated operating frequency.

To reduce high counter power consumption Alioto et al. [2] presented a low power counter design with a relatively high operating frequency. Alioto's design was based on cascading an analog block ,these analog blocks were structured using MOS current-mode logic to represent an analog divider stage such that each counting stage's (module's) input frequency was halved compared to the previous counting stage (module). Hoppe at el.[5] improved counter frequency by incorporating a 2-bit Johnson counter [7] into the initial counting module in a partitioned counter architecture. However the increase in operating frequency was offset by reduced counting capability. Kakarauntas et al. [6] used a carry look-ahead circuit [4] to replace the carry chain. The carry look-ahead used a prescaler technique with systolic 4-bit counter modules with the cost of an extra detector circuit. The detector circuit detected the assertion of lower order bits to enable counting in the higher order bits. To further improve the operating frequency, Kakarauntas's design used DFFs between systolic counter modules but the large counter widths incurred an additional three input logic gate delay. Based on the survey an efficient counter architecture is designed.

The main contributions of the proposed parallel counter are as follows:

1) A single clock input triggers all counting modules simultaneously, resulting in an operating frequency independent of counter width. The total critical path delay is uniform at all counting stages and is equal to the combination of the access time of a 2-bit counting module, a single three input AND gate delay, and the DFF setup-hold time.
2) Parallel counter architecture enables high flexibility and reusability, and thus enables short design time for wide counter applications. The architecture is composed of three basic module types separated by DFFs in a pipelined organization. These three modules type are placed in a highly repetitious structure in both the counting path and the state look-ahead paths, which limits localized connections to only three signals.
3) The counter output is in radix-2 representation so the count value can be read on-the-fly with no additional logic decoding.
4) Proposed counter has no latency.

II. PROPOSED PARALLEL COUNTER ARCHITECTURE

2.1 Implemented Architecture

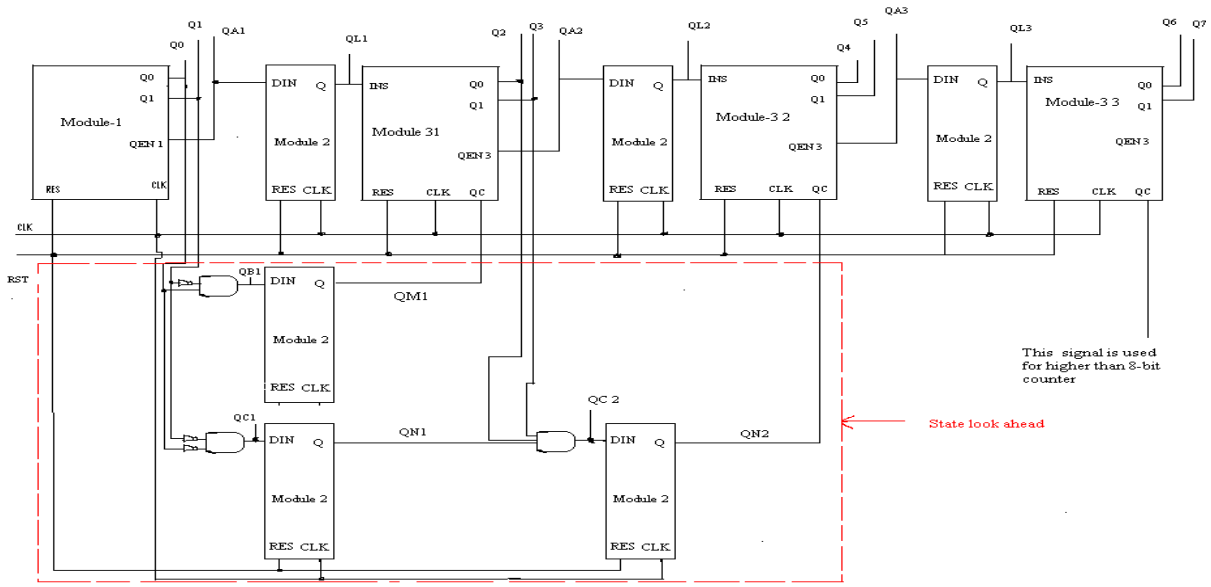

Figure 1. Proposed 8-bit parallel counter

Figure 1 is a proposed parallel counter architecture for 8-bit counter. The main structure consists of the state look-ahead path and the counting path. The counter is partitioned into uniform 2-bit synchronous up counting modules.

The counting path's counting logic controls counting operations and the state look-ahead logic anticipates future states and thus prepares the counting for these future states. Figure 1 shows the three module types (module-1, module-2 and module-3s, where s=123, etc.) used to construct both paths. Module-1 and module-3 are exclusive to the counting path and each module represents two counter bits. Module-2 is a conventional positive edge triggered DFF and is present in both paths. In the counting path, each module-3s's serves two main purposes. The first purpose is to generate all counter bits associated with their ordered position and the second purpose is to enable (in conjunction with stimulus from the state look ahead path) future states in subsequent module-3s's in conjunction with stimulus from the state look- ahead path.

2.2 Architecture Functionality of Module-1

Module -1 is a standard parallel synchronous binary 2-bit counter, which is responsible for low order bit counting and generating future states for all modules-3s's by pipelining the enable for these future states through the state look-ahead path. Hardware schematic and state diagram is shown in Figure 2.

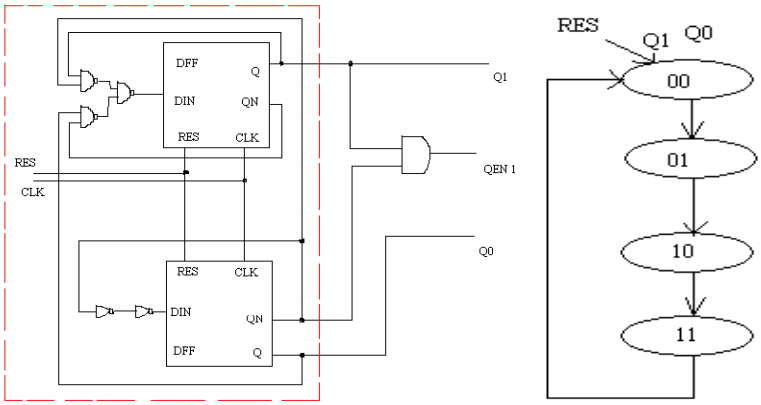

Figure 2. Hardware schematic and state diagram for module-1

2.3 Architecture Functionality of Module-3S

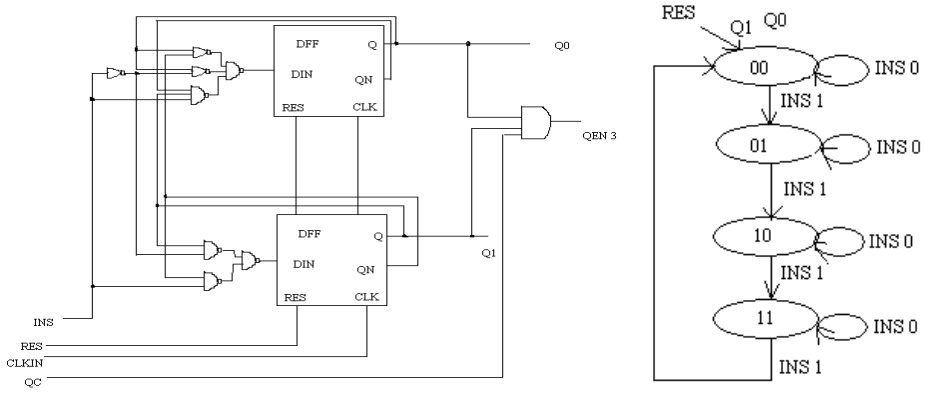

Figure 3. Hardware schematic and state diagram for module-3S.

Figure 3 shown above is hardware schematic and state diagram of Module-3S. Module-3S is a parallel synchronous binary 2-bit counter whose count is enabled by INS. INS connects to the Q output of the preceding module-2. QEN3 connects to the subsequent module2's DIN input and provides the one – cycle look ahead mechanism.

2.4 Generalized Parallel Counter Architecture

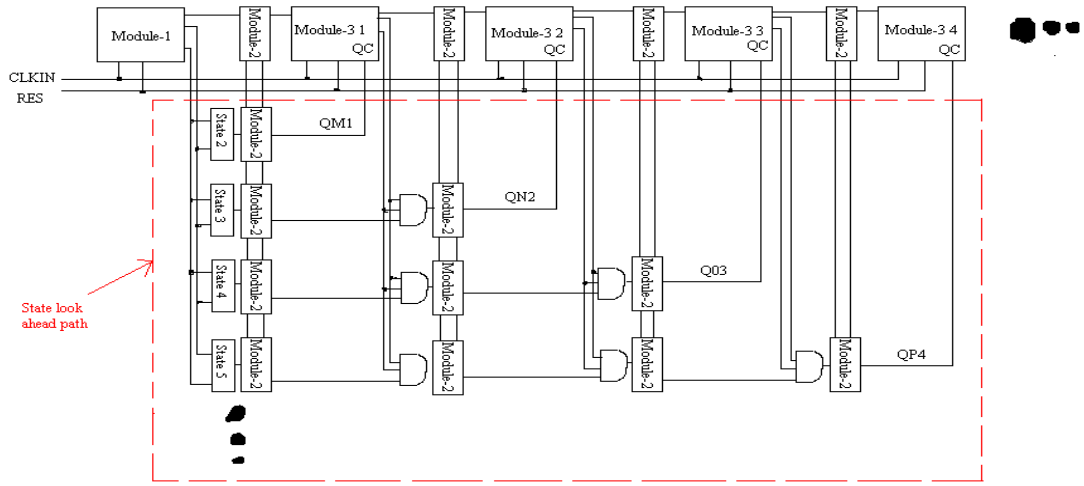

Figure 4. Generalized N-bit parallel counters

Figure 4 depicts a generalized N-bit counter topology, revealing state look ahead path details.Modules-2s in the state look-ahead logic are responsible for propagating (pipelining) the overflow detection to the appropriate module-3S. Early overflow is initiated by the module -1 through the left most column of decoders (state-2, state-3 etc.).

III. SIMULATION RESULTS

A Testbench is developed using Verilog which verifies the functionality of the proposed counter and it is simulated using ModelSim simulator which is shown in Figure 5. Simulation result of 8-bit counter shows that a similar sequence repeats through the remaining clock cycles due to the counter state anticipation by pipelining early overflow detection. These mechanisms enable all modules to maintain the same gate delay regardless of counter width.

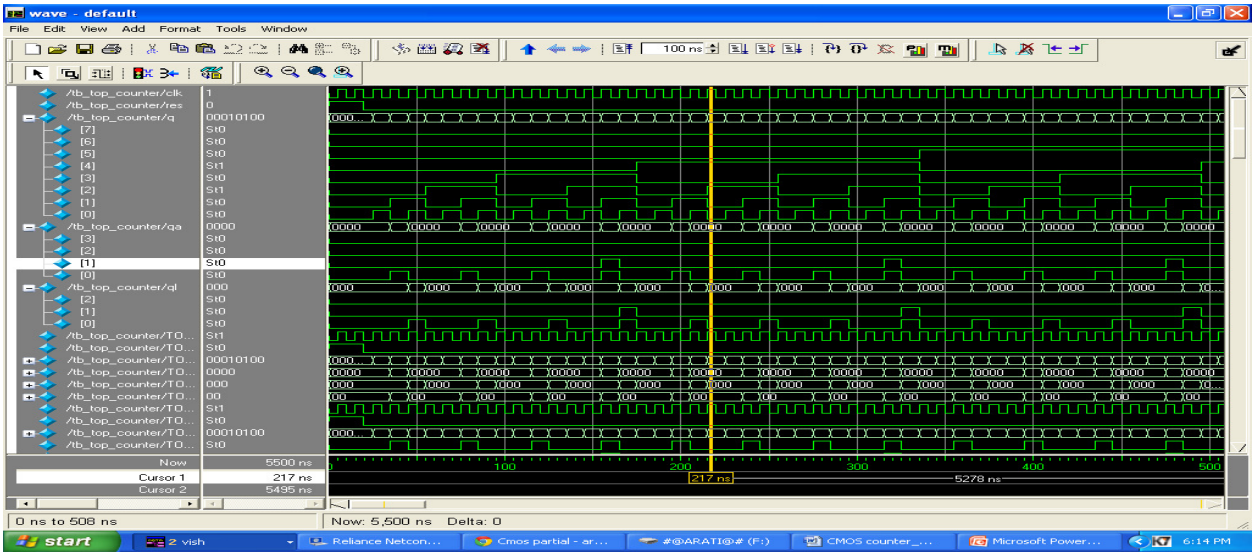

Figure 5. Simulated 8- bit proposed counter

IV. SYNTHESIS RESULTS

Using Xilinx ISE 8.2i synthesis is done and analyzed which is shown in Figure 6. The synthesis report shows the number of flip-flops and IOBs (input-output blocks) used is very less. Also gives the parameters enhanced like operating frequency, power dissipation, gate delay & net delay.

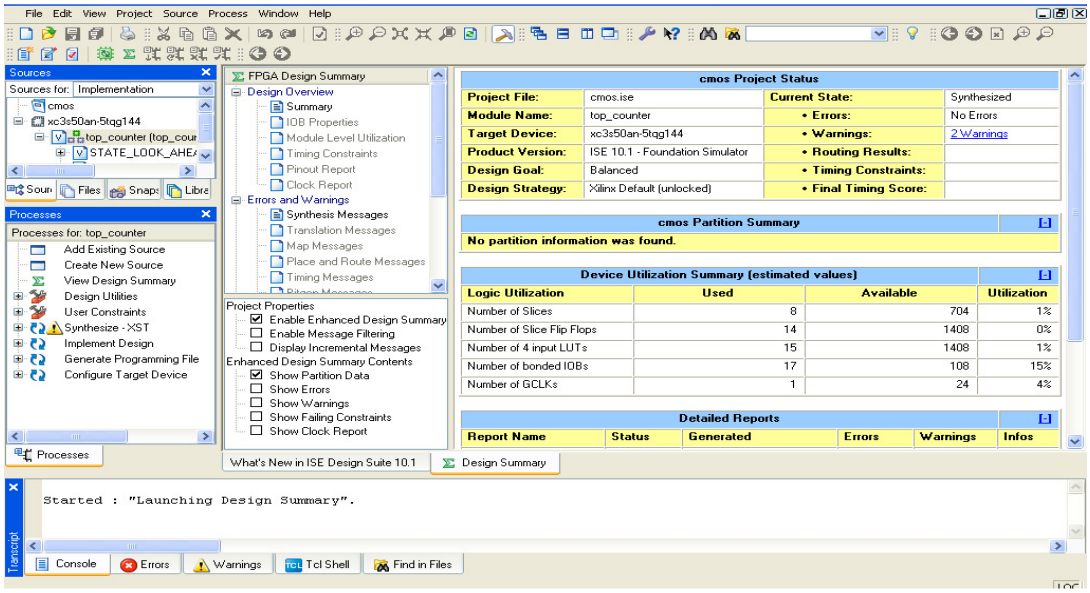

Figure 6. Synthesis report of 8- bit proposed counter

V. RESULTS COMPARISON

Table 1 clearly shows that implemented method has given the best performance metrics compared to existing. The implemented counter has increased the frequency about 55% more than the previous design. Also the delay and power dissipation get reduced.

Table 1: Comparison of proposed design with existing design

	Existing counter	Proposed counter
Operating frequency	215.564 MHZ	387.597 MHZ
Delay [Gate delay+Net delay]	6.982 ns	6.173 ns
Power	36 mW	19 mW

VI. CONCLUSION AND FUTURE WORKS

This paper presented a scalable high-speed parallel counter using CMOS gate logic components. This counter design logic is comprised of mainly 2-bit counting modules and three input AND gates. Counter's structure main features are pipelined and state look ahead path logic whose interoperation activates all modules concurrently at the system's clock edge, thus provides all counter state values at the exact time without rippling effects. In addition, this structure avoids using along chain detector circuit typically required for large counter widths. To make the architecture compatible, efficient CMOS transistors should be used and interconnection nets can be reduce using efficient logic design along with lesser number of AND gate to get low chain delay and hence the latency can be reduce.

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