INVERTED SINE PULSE WIDTH MODULATED THREE-PHASE CASCADED MULTILEVEL INVERTER

R.Seyezhai
Associate Professor, Department of EEE, SSN College of Engineering, Chennai, India

ABSTRACT

MultiLevel Inverter (MLI) has been recognized as an attractive topology for high voltage DC-AC conversion. This paper addresses an Inverted Sine PWM (ISPWM) technique to control the seven-level asymmetric cascaded multilevel inverter. The proposed switching technique enhances the fundamental component of the output voltage and generates lower total harmonic distortion in comparison with the conventional triangular based multicarrier PWM techniques. A detailed study of the proposed modulation technique is carried out through MATLAB /SIMULINK. Gating signals are generated using FPGA Spartan processor. A prototype of three-phase asymmetric cascaded MLI is developed to verify the theoretical results.

KEYWORDS: *Asymmetric Multilevel Inverter, THD, Inverted sine PWM.*

I. INTRODUCTION

Multilevel inverter is an effective and practical solution for increasing power demand and reducing harmonics of AC waveforms. Function of a multilevel inverter is to synthesize a desired voltage wave shape from several levels of DC voltages. As the number of levels increase, the synthesized staircase output waveform has more steps, approaching the desired sinusoidal waveform. They are of special interest in the distributed energy sources area because several batteries, fuel cell and solar cell can be connected through multilevel inverter to feed a load [1]. This paper presents a seven-level asymmetric cascaded multilevel inverter suited for renewable energy applications. The advantages of this topology are better output quality, lower switching dissipation, lesser number of sources and higher efficiency. The performance of multilevel inverter (such as switching loss and harmonics) is mainly decided by its modulation strategies. The modulation control schemes for the multilevel inverter can be divided into two categories fundamental switching frequency and high switching frequency PWM. Further, the high frequency PWM is classified as multilevel carrier-based PWM and multilevel space vector PWM [2]. The most popular and simple high frequency switching scheme for MLI is the Multi-Carrier PWM (MCPWM). It can be categorized into two groups: Carrier Disposition (CD) methods and Phase Shifted (PS) methods [3]. Among the carrier disposition methods, Phase Disposition (PD) PWM technique is normally employed for MLI as the carriers need minimal amounts of alteration since they are all in phase with each other [4]. This paper focuses on PD based inverted sine PWM technique for a seven-level inverter. ISPWM has a better spectral quality and a higher fundamental voltage compared to the triangular based PWM. The performance of asymmetric MLI with the proposed modulation strategy is studied through simulation studies for linear loads. A comparative evaluation between hybrid modulation and the conventional PDPWM method is also presented in terms of output voltage quality, power circuitry complexity, Total Harmonic Distortion (THD). A seven-level asymmetric MLI prototype has been developed to verify the simulation results.
Section-2 discusses about the three-phase asymmetric cascaded multilevel inverter with reduced number of switches. Section -3 describes the proposed inverted sine pulse width modulation technique

highlighting its advantages compared to the conventional triangular based carrier. Section -4 discusses the simulation results for the proposed PWM technique and the results are compared with the conventional PWM .Section-5 provides the details about the prototype of the asymmetric multilevel inverter and the validation of simulation results.

II. ASYMMETRIC CASCADED MULTILEVEL INVERTER

The cascaded multilevel inverter with separate DC sources can fit many of the needs of all electric vehicles because it can use on board batteries or fuel cells to generate a nearly sinusoidal voltage waveform to drive the main vehicle traction motor. Normally, each phase of a three-phase cascaded multilevel inverter requires "n" DC sources for 2n+1 level [5]. For many applications, multiple DC sources are required demanding long cables and this could lead to voltage unbalance among the DC sources [6]. With an aim to reduce the number of DC sources required for the cascaded multilevel inverter, this paper focuses on an asymmetric topology which uses only two DC sources to generate seven-level output. The proposed topology consists of two H-bridges as shown in Fig.1. By appropriately opening and closing the switches of H_1, the output voltage V_1 can be made equal to - $V_{dc,}$ 0, + $V_{dc.}$ Similarly the output voltage V_2 of the second bridge H_2 can be made equal to - $0.5V_{dc}$, 0 , $0.5V_{dc}$ .Therefore, the output voltage of the MLI have the values of -1.5 V_{dc}, $-V_{dc}$, $-0.5V_{dc}$, 0, $0.5V_{dc}$, V_{dc} and $1.5V_{dc}$ as shown in Fig.2.

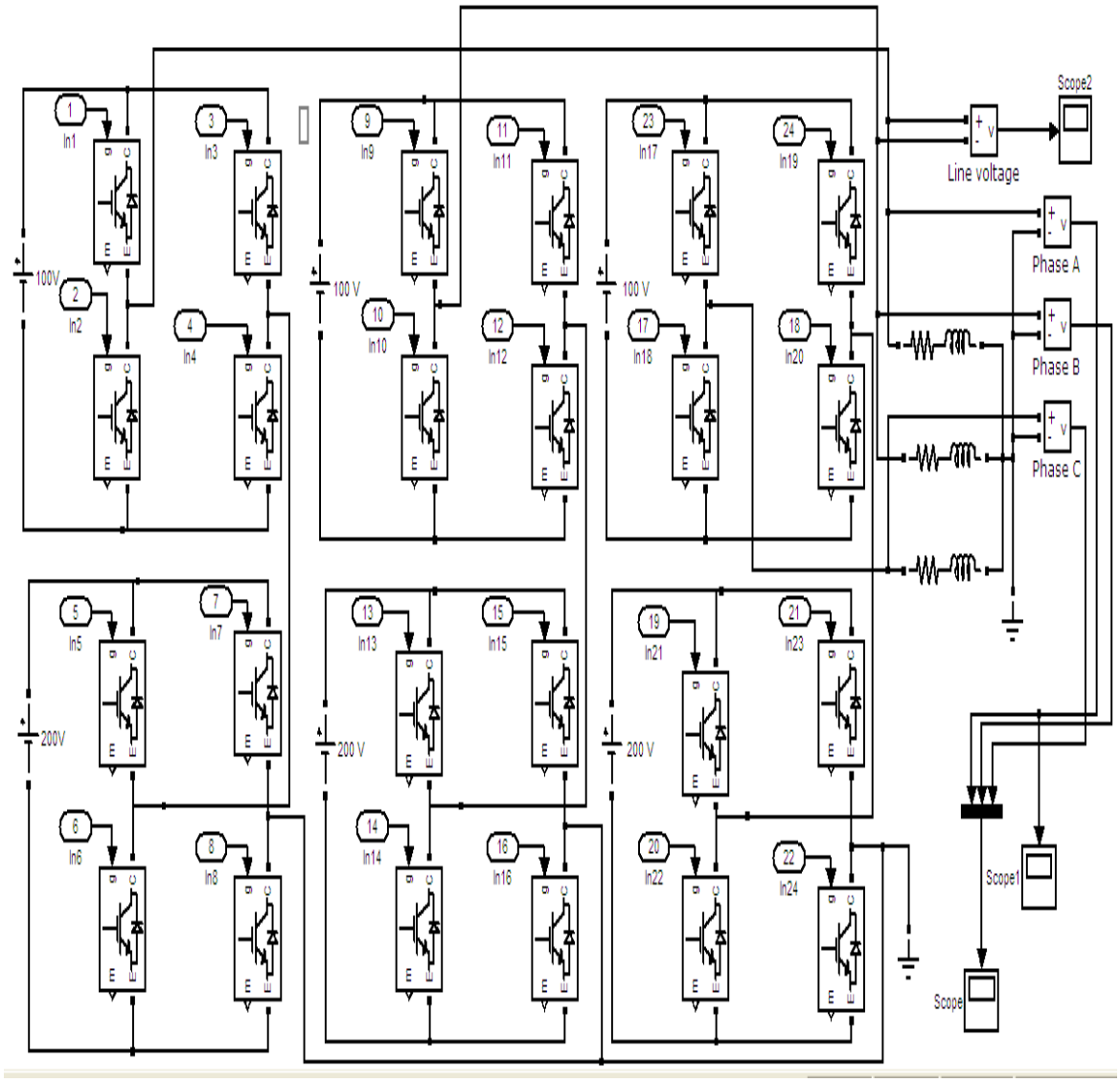

Fig.1 Three-phase Asymmetric cascaded multilevel inverter

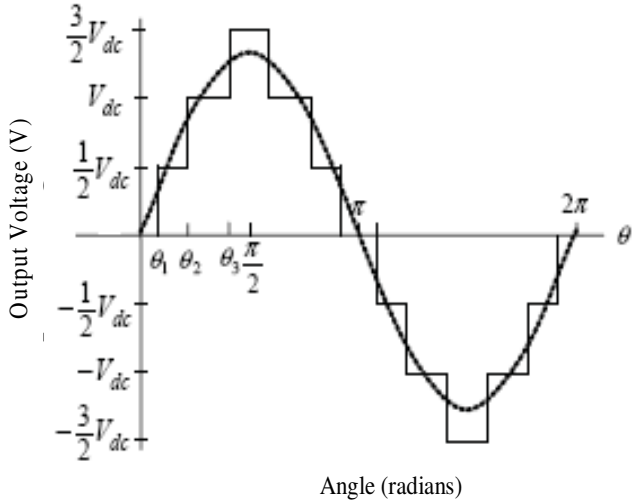

Fig .2 Seven –level equal step phase voltage waveform

III. INVERTED SINE PWM TECHNIQUE FOR MLI

The inverted sine carrier PWM (ISPWM) method uses the conventional sinusoidal reference signal and an inverted sine carrier. The control strategy uses the same reference (synchronized sinusoidal signal) as the conventional SPWM while the carrier triangle is a modified one. The control scheme uses an inverted (high frequency) sine carrier that helps to maximize the output voltage for a given modulation index [7-10]. In the gating pulse generation of the proposed ISCPWM scheme, the triangular carrier waveform of SPWM is replaced by an inverted sine waveform. In Fig.3 shows the pulse generation circuit for a single phase of the multilevel inverter in which a sine wave (modulating signal) of fundamental frequency is compared with high frequency phase disposed inverted sine carrier waves. For an 'm' level inverter, (m-1) carrier waves are required. The pulses are generated when the amplitude of the modulating signal is greater than that of the carrier signal.
The proposed control strategy has a better spectral quality and a higher fundamental output voltage without any pulse dropping.

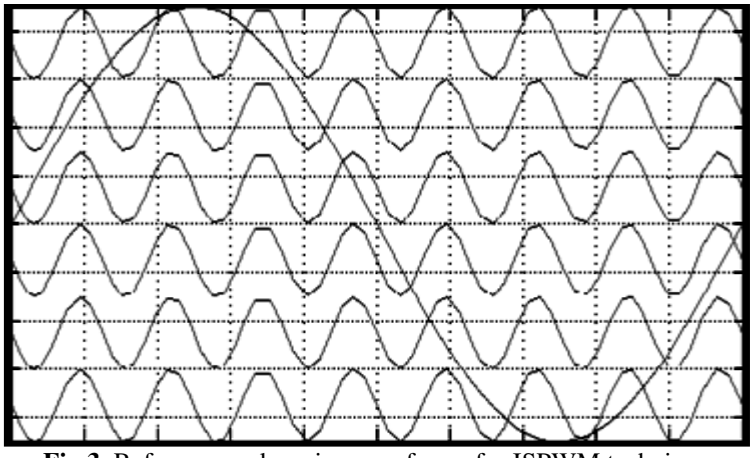

Fig.3. Reference and carrier waveforms for ISPWM technique

The advantages of ISPWM method are:

- It has a better spectral quality and a higher fundamental component compared to the conventional sinusoidal PWM (SPWM) without any pulse dropping.
- The ISCPWM strategy enhances the fundamental output voltage particularly at lower modulation index ranges

- There is a reduction in the total harmonic distortion (THD) and switching losses.
- To increase the fundamental amplitude in the sinusoidal pulse-width modulation the only way is by increasing the modulation index beyond 1 which is called over modulation. Over modulation causes the output voltage to contain many lower order harmonics and also makes the fundamental component vs. modulation index relation non-linear. Inverted sine pulse - width modulation technique replaces over modulation [11].
- The appreciable improvement in the total harmonic distortion in the lower range of modulation index attracts drive applications where low speed operation is required.

ISPWM technique causes marginal increase in the lower order harmonics, but except third harmonic all other harmonics are in acceptable level. But for three phase applications the heightened third harmonics need not be bothered [12-15]. The pulses generated using inverted sine pulse-width modulation technique is shown in Fig.4 which is used to trigger the IGBTs in a sequential manner such that the desired output is obtained.

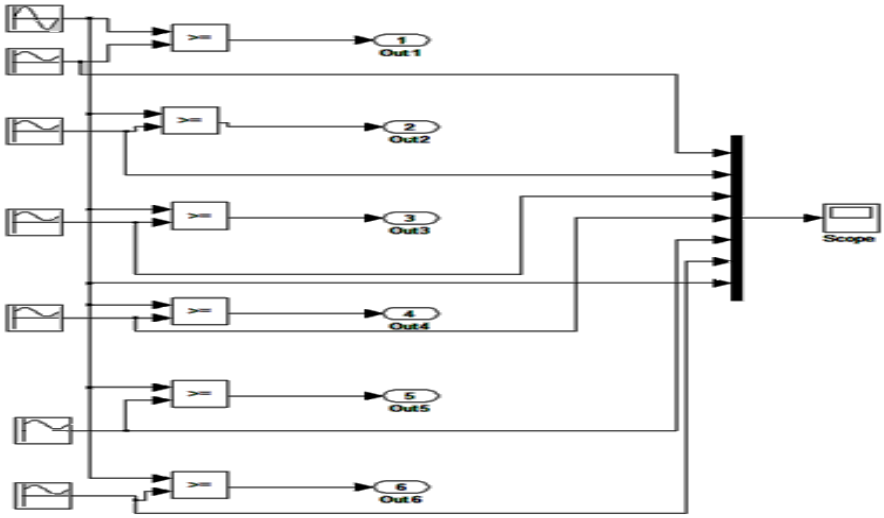

Fig. 4 Pulse generation circuit for ISPWM

The gating signals for a single phase asymmetric MLI using ISPWM is shown in Fig.5.

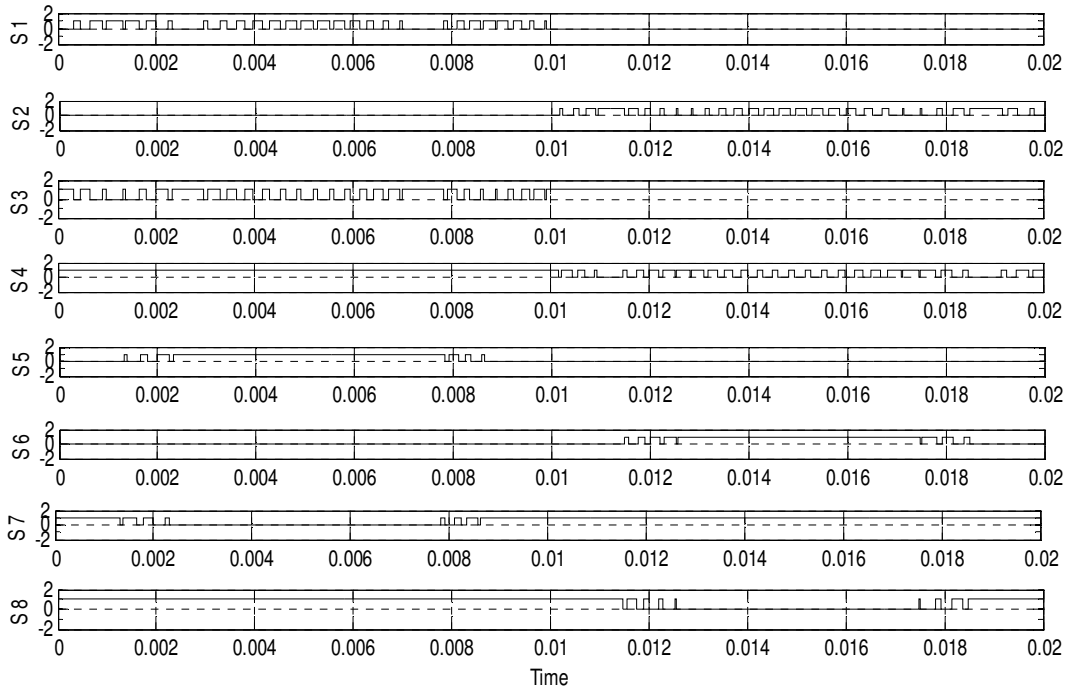

Fig.5 Pulse pattern for asymmetric MLI employing ISPWM

IV. SIMULATION RESULTS

The performance evaluation [16-17] of an inverted sine pulse-width modulated for three-phase asymmetric cascaded multilevel inverter is done using MATLAB and the phase voltage for the three phases is shown in Fig.6

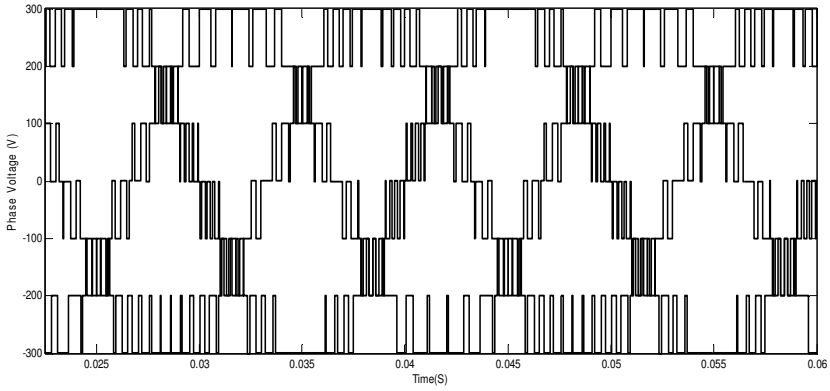

Fig.6 Phase Voltage waveform for asymmetric MLI using ISPWM

The line- line voltage waveform is shown in Fig.7

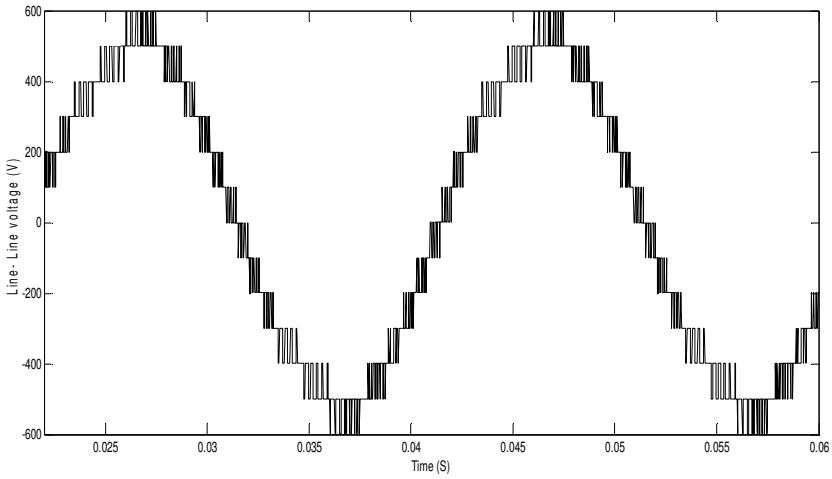

Fig.7 Line-line voltage waveform of Asymmetric cascaded MLI (ISPWM)

The line- line current waveform for asymmetric cascaded MLI is shown in Fig.8

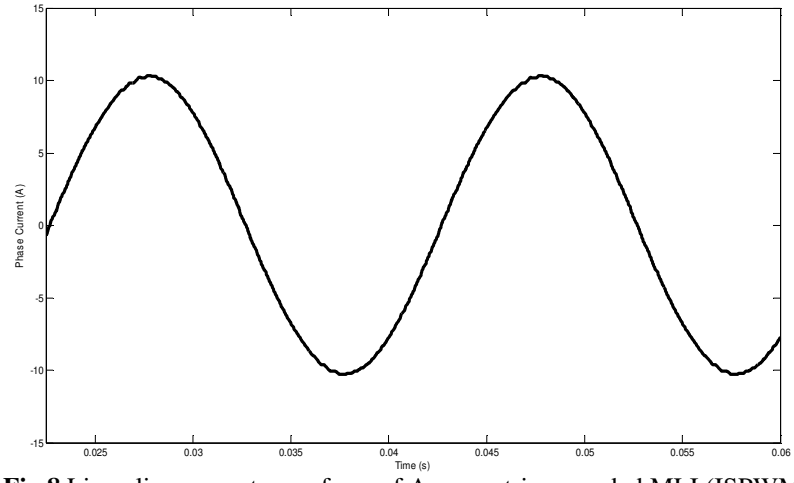

Fig.8 Line –line current waveform of Asymmetric cascaded MLI (ISPWM)

FFT spectrum for the load voltage waveform of MLI using ISPWM technique is shown in Fig.9

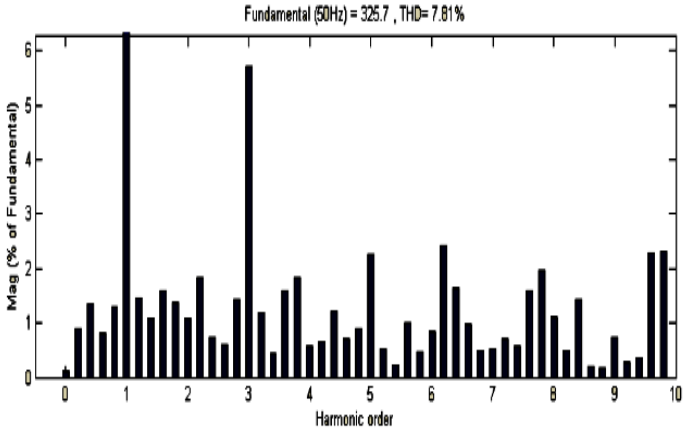

Fig.9 FFT spectrum of load voltage of MLI (F_{opt} = 3950Hz)

The FFT spectrum for the load current waveform is shown in Fig.10

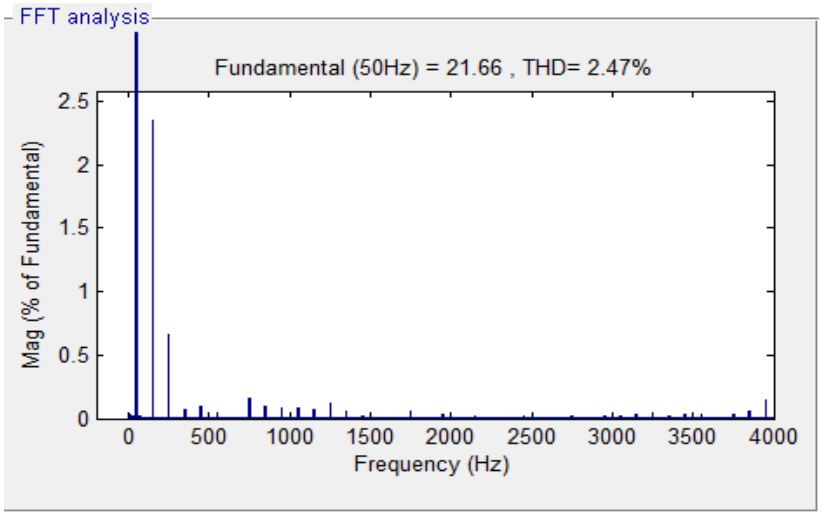

Fig.10 FFT Spectrum for the load current of MLI

The fundamental component of voltage [18-19] increases with increase in switching frequency and is higher for inverted sine carrier compared to the conventional triangular carrier which is shown in Fig.11.

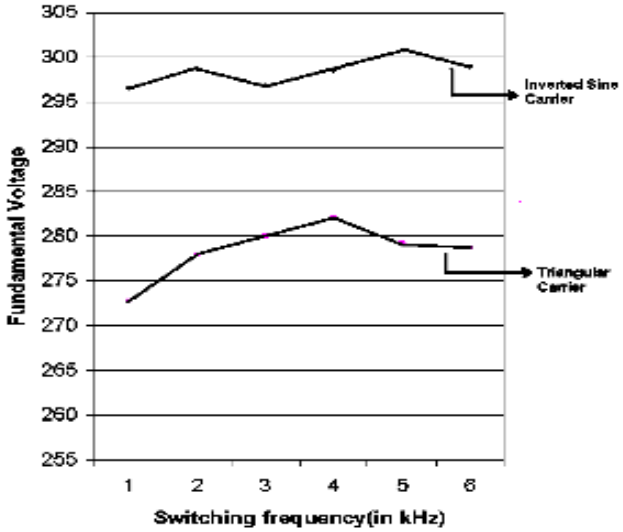

Fig.11 Fundamental voltage Vs Switching frequency

From the above results, it is observed that ISPWM gives an enhanced fundamental voltage and reduced total harmonic distortion.

V. EXPERIMENTAL RESULTS

To experimentally validate the asymmetric cascaded H-bridge multilevel inverter using the proposed modulation, a prototype of three-phase seven-level inverter has been built using FSBB20CH60 smart power module (SMP) as the switching devices shown in Fig.1.The SMP uses IGBT as the power device and it provides optimized circuit protection and drive matched to low loss IGBT. Hardware can be divided into the following sections: a Xilinx Spartan board, 7- level MLI setup (optocoupler, driver & power circuit) and load configuration. Xilinx Spartan 3-A DSP trainer is employed to generate the pulses required to trigger the IGBTs. The PWM pins AE3 to AF8 are used to generate the gating pulses of the respective devices. Transformers, Bridge Rectifiers and Voltage Regulators are used to form 12V DC supply for opto-couplers. Optocoupler consists of LED and a phototransistor. When an electrical signal is applied to the input of the opto-isolator, its LED lights, its light sensor then activates, and a corresponding electrical signal is generated at the output. The experimental setup for the asymmetric MLI is shown in Fig.12.

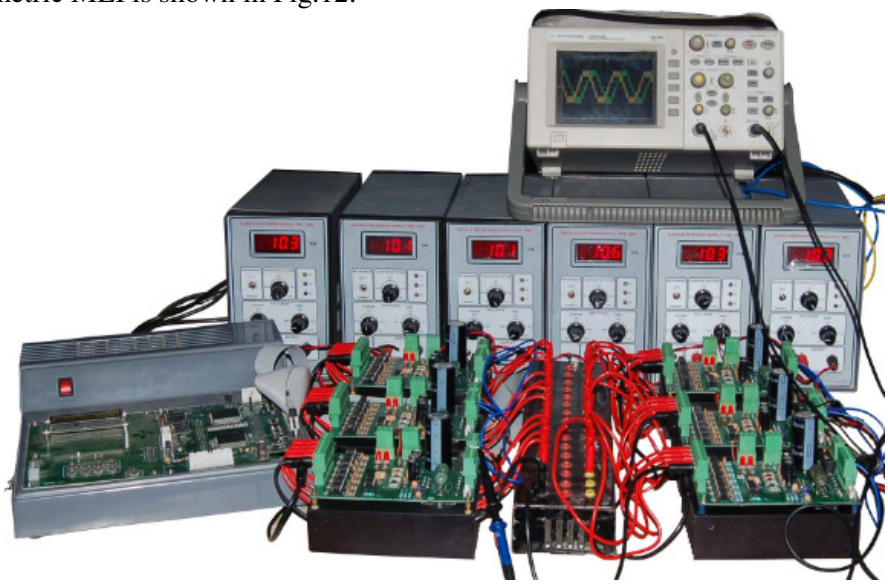

Fig.12 Photograph of the prototype of 3-phase asymmetric MLI

The experimental phase voltage waveforms is shown in Fig.13

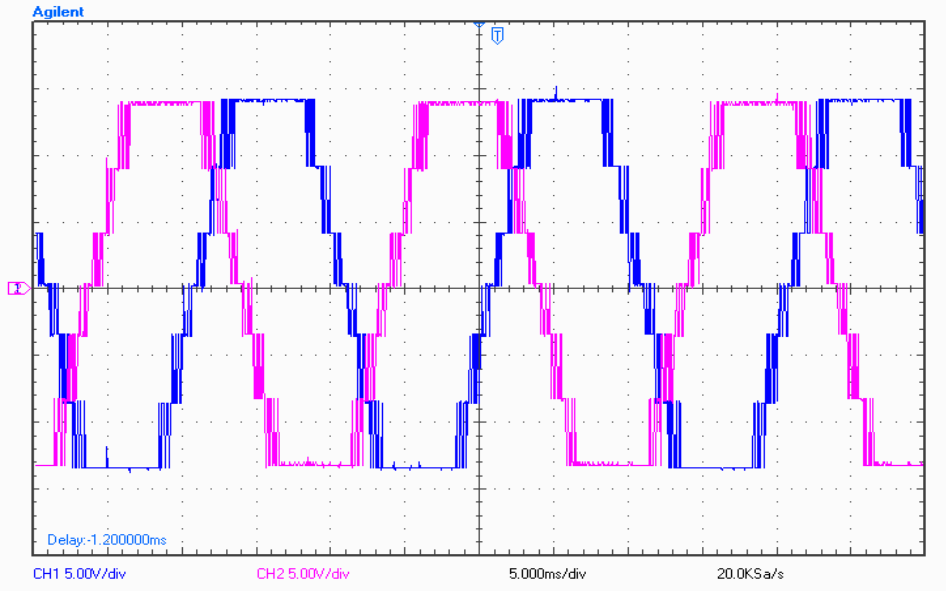

Fig.13 Experimental phase voltage waveform for 3-phase asymmetric cascaded MLI

The experimental line –line voltage waveform for MLI employing ISPWM technique is shown in Fig.14.

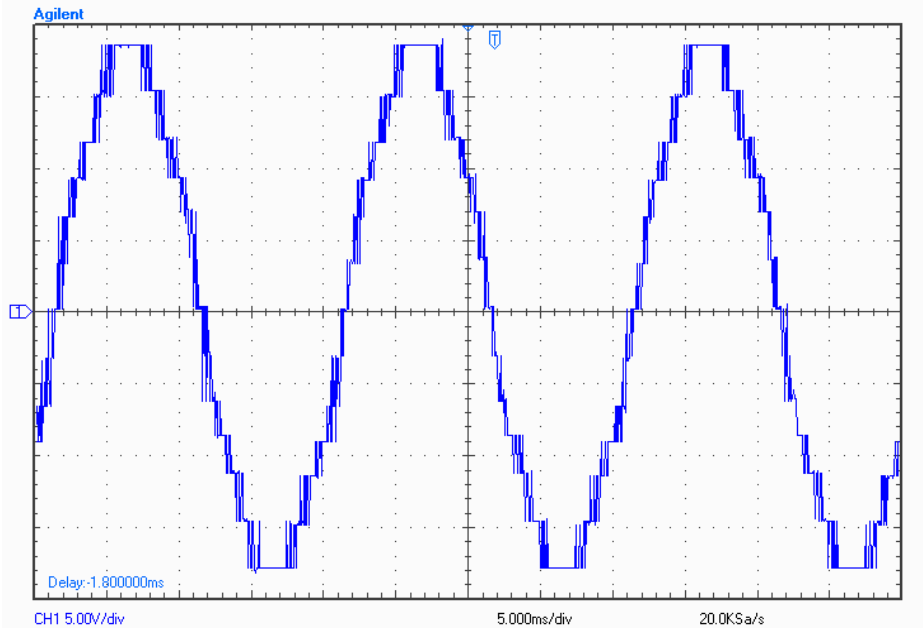

Fig.14 Experimental phase voltage waveform for 3-phase asymmetric cascaded MLI

VI. CONCLUSIONS

A three-phase asymmetric cascaded multilevel inverter employing inverted sine PWM technique has been investigated. From the simulation and experimental results, it is observed that ISPWM technique provides an enhanced fundamental voltage and reduced THD compared to the conventional triangular based PWM. Line-line voltage waveform of the proposed MLI topology produces 13-level which greatly reduces the harmonics in the output waveform. Asymmetric MLI Topology uses reduced number of DC sources thus decreasing the complexity and the cost of the circuit. This can be important in the high power quality cascaded multilevel inverters which require several voltage sources and knowledge of the DC voltage levels. By increasing the number of steps, waveform approaches the desired sinusoidal shape and THD is reduced. The proposed modulation strategy can be applied to multilevel inverter powered by fuel cells in place of DC sources and it has a greater scope in applications involving electrical vehicles and distributed generation.

REFERENCES

[1]. Fang Zheng Peng, Jih-Sheng Lai, and Rodriguez, J. "Multilevel inverters: a survey of topologies, controls, and applications", Industrial Electronics, IEEE Transactions, Vol. 49, issue:4, pp. 724-738, Aug 2002.

[2]. B.L.Mathur and R.Seyezhai ''Harmonic Evaluation of Multicarrier PWM Techniques for Cascaded Multilevel Inverter''. International Conference on Electrical Engineering Applications ICEEA 2008, Algeria.

[3]. M.Calais, L. J. Borle and V.G. Agelidis, "Analysis of Multicarrier PWM Methods for a Single-phase Five Level Inverter", in Proc. 32nd IEEE Power Electronics Specialists Conference,PESC'01,July 2001,pp 1351-1356.

[4]. Radan,, A.H.Shahirinia, and M Falahi, "Evaluation of Carrier-Based PWM Methods for Multi-level Inverters", in Proc. IEEE International Symposium on Industrial Electronics, ISIE 2007, pp. 389-394, 2007.

[5]. S. Mariethoz, and A.C. Rufer, "Design and control of asymmetrical multi-level inverters," in Proc. IEEE 28th Annual Conference, IECON 02, Vol. 1, pp. 840-845, 2002.

[6]. D. Zhong, , L.M Tolbert, J.N. Chaissson, and B.Ozpineci, "A Cascaded Multilevel Inverter Using a Single DC Source", in Proc. Applied Power Electronics Conference and Exposition, Vol. 2, pp. 426-430, 2006.

[7]. P.Dananjayan, S.Jeevananthan, R.Nandhakumar ‘‘Inverted Sine Carrier for Fundamental Fortification in PWM Inverters and FPGA Based Implementations’’. Serbian Journal of Electrical Engineering, Vol. 4, No. 2, pp. 171-187, November 2007.
[8]. R. Seyezhai and B.L.Mathur, “Implementation and control of Variable Frequency ISPWM Method for an Asymmetric Multilevel Inverter”, European Journal of Scientific Research, Vol. 39, Issue 4, 2010, pp. 558-568.
[9]. R. Seyezhai and B.L.Mathur, “Performance Evaluation of Inverted Sine PWM Techniques for an Asymmetric Multilevel Inverter”, Journal of Theoretical and Applied Information Technology, Vol. 2, No. 2, 2009, pp. 91-98.
[10]. M.G.H. Aghdam, , S.H. Fathi, and B. Gharehpetian, “A Novel Carrier based PWM Method for THD reduction in Asymmetric Multilevel Inverter”, in Proc. International Conference on Renewable Energies and Power Quality, 2008, pp. 105-110.
[11]. Z.D.Far, , A. Radan, and M.D. Far, “Introduction and Evaluation of novel multi-level carrier based PWM strategies using a generalized algorithm”, in Proc. European Conference on Power Electronics and Applications, EPE’07, pp. 1-10, 2007.
[12]. L.M Tolbert, and T.G. Habetler, “Novel multilevel inverter Carrier based PWM Methods”, in Proc. IEEE IAS 1998 Annual Meeting, St.Louis, Missouri, pp. 1424-1431, 1998.
[13]. S. Yuvarajan and A. Khoei, “A Novel PWM for Harmonic Reduction and its Application to AC-DC Converters”, IETE Journal of Research, Vol. 48, No. 2, pp. 85-92, 2002.
[14]. S. Yuvarajan and Abdullah Khoei, “A novel PWM for harmonic reduction and its application to ac-dc converters,” IETE Journal of Research, Vol. 48, No. 2, March-April 2002.
[15]. D. Quek and S. Yuvarajan, "A novel PWM scheme for harmonic reduction in power converters," Proc. of International conference on Power Electronics and Drive systems, Singapore, February 1995.
[16]. N. A. Azli and Y.C. Choong, “Analysis on the performance of a Three- phase Cascaded H-Bridge Multilevel inverter”, in Proc. First International Conference on Power and Energy PECON 2006, Malaysia, pp. 405-410, 2006.
[17]. M.G.H.Aghdam, S.H.Fathi and B.Gharehpetian, “Analysis of multicarrier PWM methods for asymmetric multilevel inverter”, in Proc. 3rd IEEE Conference on Industrial Electronics and Applications, ICIEA’08, pp. 2057- 2062, 2008.
[18]. H.Keivani, M.R.Askari, F.Kavahnia, Aghdam, A. Mohammadi, "Novel multicarrier PWM method for a three- phase cascaded H-bridge multilevel inverter", in Proc. 41st International Universities Power Engineering Conference, UPEC 2006, 6- 8 September 2006, Vol .2, pp- 593 – 597.
[19]. Radan, A. H. Shahirinia, M. Falahi, “Evaluation of Carrier- Based PWM Methods for Multi-level Inverters” in Proc. IEEE International Symposium on Industrial Electronics,ISIE07, June 2007,pp.389-394.

ACKNOWLEDGEMENT

The authors wish to express her gratitude to the management of SSN Institutions, Chennai, India and Vi Microsystems, Chennai for providing the laboratory and computational facilities to carry out this work.

AUTHOR PROFILE

R. Seyezhai obtained her B.E. Electronics & Communication Engineering) from Noorul Islam College of Engineering, Nagercoil in 1996 and her M.E in Power Electronics & Drives from Shanmugha College of Engineering, Thanjavur in 1998 and PhD from Anna University, Chennai. She has been working in the teaching field for about 13 Years. She has published several papers in International Journals and International Conferences in the area of Power Electronics & Drives. Her areas of interest include SiC Power Devices, Multilevel Inverters, Modeling of fuel cells, Design of Interleaved Boost Converter, Multiport DC-DC Converter and control techniques for DC-DC Converter.