

# A ZIGZAG-DELTA PHASE-SHIFTING TRANSFORMER AND THREE-LEG VSC BASED DSTATCOM FOR POWER QUALITY IMPROVEMENT

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## ABSTRACT

*In this paper, a new three-phase four-wire distribution static compensator (DSTATCOM) based on a Phase-Shifting transformer (PST) and a three-leg voltage source converter (VSC) is proposed for power quality improvement. The Zigzag Phase-Shifting transformer mitigates the circulating power flows in interconnected utilities and the three-leg VSC compensates harmonic current, reactive power and balances the load. The principle of PST is to take harmonics generated from separate sources, shift one source of harmonics 180° with respect to the other and then combine them together; this will result in cancellation. This type of transformer has patented built-in electromagnetic technology designed to remove high neutral current and the most harmful harmonics from the 3<sup>rd</sup> through 21<sup>st</sup>. The interesting aspect of such phase shifters is that despite their low MVA capacity, by controlling the phase shift, they exercise a significant real-power control. The insulated gate bipolar transistor (IGBT) based VSC is supported by a capacitor and is controlled for the required compensation of the load current. The dc bus voltage of the VSC is regulated during varying load conditions. The performance of the three-phase four-wire DSTATCOM is validated using MATLAB software with its Simulink and power system blockset toolboxes.*

**KEYWORDS:** *Distribution Static Compensator (DSTATCOM), Neutral Current Compensation, Power Quality Improvement, Phase-Shifting Transformer (PST), Voltage Source Converter (VSC)*

## I. INTRODUCTION

Three-phase four-wire distribution systems are facing severe power quality problems such as poor voltage regulation, high reactive power and harmonics current burden, load unbalancing, excessive neutral current, etc. Three-phase four-wire distribution systems are used in commercial buildings, office buildings, hospitals, etc. Most of the loads in these locations are nonlinear loads and are mostly unbalanced loads in the distribution system. This creates excessive neutral current both of fundamental and harmonic frequency, and the neutral conductor gets overloaded. The voltage regulation is also poor in the distribution system due to the unplanned expansion and the installation of different types of loads in the existing distribution system. In order to control the power quality problems, many standards are proposed, such as the IEEE-519 standard [6].

There are mitigation techniques for power quality problems in the distribution system and the group of devices is known by the generic name of custom power devices (CPDs) [1]. The distribution static compensator (DSTATCOM) is a shunt-connected CPD capable of compensating power quality problems in the load current. Some of the topologies of DSTATCOM for three-phase four-wire

system for the mitigation of neutral current along with power quality compensation in the source current are four-leg voltage source converter (VSC), three single-phase VSCs, three-leg VSC with split capacitors [3], three-leg VSC with zigzag transformer [7]-[9] and three-leg VSC with neutral terminal at the positive or negative of dc bus [10]. The voltage regulation in the distribution feeder is improved by installing a shunt compensator [11]. There are many control schemes reported in the literature for control of shunt active compensators such as instantaneous reactive power theory, power balance theory, synchronous reference frame theory, symmetrical components based, etc. [12], [13]. The synchronous reference frame theory [12] is used for the control of the proposed DSTATCOM. In this paper, a new topology of DSTATCOM is proposed for a three-phase four-wire distribution system, which is based on three-leg VSC and a Zigzag Phase-Shifting transformer (PST). Harmonic cancellation is performed with harmonic cancelling transformers also known as phase-shifting transformers. A harmonic cancelling transformer is a relatively new power quality product for mitigating harmonic problems in electrical distribution systems. This type of transformer has patented built-in electromagnetic technology designed to remove high neutral current and the most harmful harmonics from the 3<sup>rd</sup> through 21<sup>st</sup>. The technique used in these transformers is call "low zero phase sequencing and phase shifting". These transformers can be used to treat existing harmonics in buildings or facilities. This same application can be designed into new construction to prevent future harmonics problems. The insulated gate bipolar transistor (IGBT) based VSC is self-supported with a dc bus capacitor and is controlled for the required compensation of the load current.

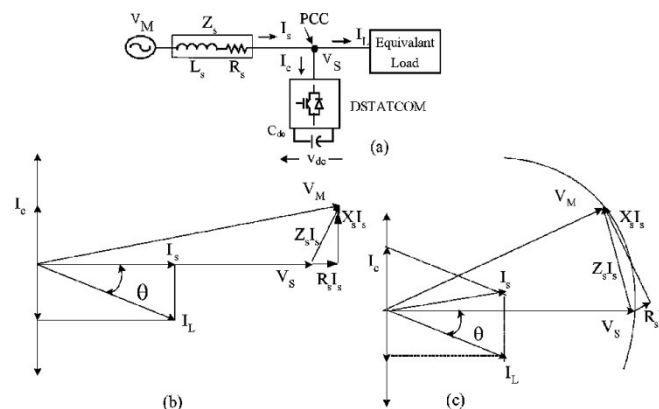


Fig. 1. (a) Single-line diagram of DSTATCOM system. (b) Phasor diagram for UPF operation. (c) ZVR operation.

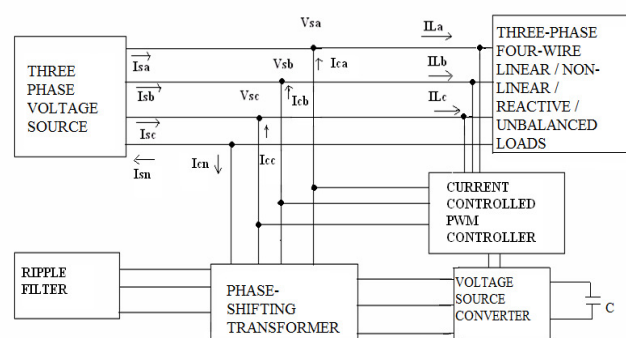


Fig. 2. Block diagram of the proposed three-leg VSC with Phase-Shifting transformer based DSTATCOM connected in distribution system.

The DSTATCOM is designed and simulated using MATLAB software with its Simulink and power system blockset (PSB) toolboxes for power factor correction and voltage regulation along with neutral current compensation, harmonic elimination, and load balancing with linear loads as well as nonlinear loads.

## II. SYSTEM CONFIGURATION AND DESIGN

Fig. 1(a) shows the single-line diagram of the shunt-connected DSTATCOM based distribution system. The dc capacitor connected at the dc bus of the converter acts as an energy buffer and establishes a dc voltage for the normal operation of the DSTATCOM system. The DSTATCOM can be operated for reactive power compensation for power factor correction or voltage regulation. Fig. 1(b) shows the phasor diagram for the unity power factor operation. The DSTATCOM injects a current  $I_C$  such that the source current is only  $I_S$ , and this is in-phase with voltage. The voltage regulation operation of DSTATCOM is depicted in the phasor diagram of Fig. 1(b). The DSTATCOM injects a current  $I_C$  such that the voltage at the load ( $V_S$ ) is equal to the source voltage ( $V_M$ ).

The proposed DSTATCOM consists of a three-leg VSC and a Phase-Shifting transformer is shown in Fig. 2, where the Phase-Shifting transformer is connected in Zigzag – delta configuration. The Zigzag Phase-Shifting Transformer block implements a three-phase transformer with a primary winding connected in a zigzag configuration and a configurable secondary winding. The model uses three single-phase, three-winding transformers. The primary winding connects the windings 1 and 2 of the single-phase transformers in a zigzag configuration. The secondary winding connects the windings 3 of the single-phase transformers in delta configuration.

A three-leg VSC is used as an active shunt compensator along with a Phase-shifting transformer, as shown in Fig.2, and this topology has six IGBTs, three ac inductors, and one dc capacitor. The required compensation to be provided by the DSTATCOM decides the rating of the VSC components. The VSC is designed for compensating a reactive power of 12 kvar, as decided from the load details. The selection of interfacing inductor, dc capacitor, and the ripple filter are given in the following sections.

### 2.1. DC Capacitor Voltage

The minimum dc bus voltage of VSC of DSTATCOM should be greater than twice the peak of the phase voltage of the system [17]. The dc bus voltage is calculated as

$$V_{dc} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3}m} \quad (1)$$

where  $m$  is the modulation index and is considered as 1, and  $V_{LL}$  is the ac line output voltage of DSTATCOM. Thus,  $V_{dc}$  is obtained as 677.69 V for  $V_{LL}$  of 415 V and is selected as 700 V.

### 2.2. DC Bus Capacitor

The value of dc capacitor ( $C_{dc}$ ) of VSC depends on the instantaneous energy available to the DSTATCOM during transients [17]. The principle of energy conservation is applied as

$$\frac{1}{2}C_{dc} \left[ (V_{dc}^2) - (V_{dc1}^2) \right] = 3V(\alpha I)t \quad (2)$$

where  $V_{dc}$  is the reference dc voltage and  $V_{dc1}$  is the minimum voltage level of dc bus,  $\alpha$  is the overloading factor,  $V$  is the phase voltage,  $I$  is the phase current, and  $t$  is the time by which the dc bus voltage is to be recovered.

Considering the minimum voltage level of the dc bus,  $V_{dc1} = 690$  V,  $V_{dc} = 700$  V,  $V = 239.60$  V,  $I = 27.82$  A,  $t = 350$   $\mu$ s,  $\alpha = 1.2$ , the calculated value of  $C_{dc}$  is 2600  $\mu$ F and is selected as 3000  $\mu$ F.

### 2.3. AC Inductor

The selection of the ac inductance ( $L_f$ ) of VSC depends on the current ripple  $i_{cr,p-p}$ , switching frequency  $f_s$ , dc bus voltage ( $V_{dc}$ ), and  $L_f$  is given as [17]

$$L_f = \frac{\sqrt{3}m V_{dc}}{12\alpha f_s i_{cr(p-p)}} \quad (3)$$

where  $m$  is the modulation index and  $\alpha$  is the overload factor. Considering,  $i_{cr,p-p} = 5\%$ ,  $f_s = 10$  kHz,  $m = 1$ ,  $V_{dc} = 700$  V,  $\alpha = 1.2$ , the  $L_f$  value is calculated to be 2.44 mH.

### 2.4. Ripple Filter

A low-pass first-order filter tuned at half the switching frequency is used to filter the high-frequency noise from the voltage at the PCC. Considering a low impedance of  $8.1 \Omega$  for the harmonic voltage at a frequency of 5 kHz, the ripple filter capacitor is designed as  $C_f = 5 \mu\text{F}$ . A series resistance ( $R_f$ ) of  $5 \Omega$  is included in series with the capacitor ( $C_f$ ). The impedance is found to be  $637 \Omega$  at fundamental frequency, which is sufficiently large, and hence, the ripple filter draws negligible fundamental current.

### 2.5. Design of the Phase-Shifting Transformer

A basic three-phase Zigzag-delta transformer consists of a Zigzag-connected primary and a delta-connected secondary. The zigzag part is accomplished by winding half of the primary turns of one phase of the transformer on one leg of the three-phase transformer, with the other half of the primary turns on an adjacent phase. The schematic diagram of the basic Zigzag-delta transformer is shown in fig.3 (a) below:

From the figure 3(a) we can see that A and A' are wound on the same leg similarly B and B' are so wound as well as C and C'. In operation, the harmonics current flow from the harmonics generating loads into the transformer primary windings. With all triplen-harmonics current are in phase with each other, by vector analysis, the positive and negative flux interaction in the zigzag is "cancelling" these triplen-harmonics. Hence there is reduced harmonics current flowing back into the primary and system.

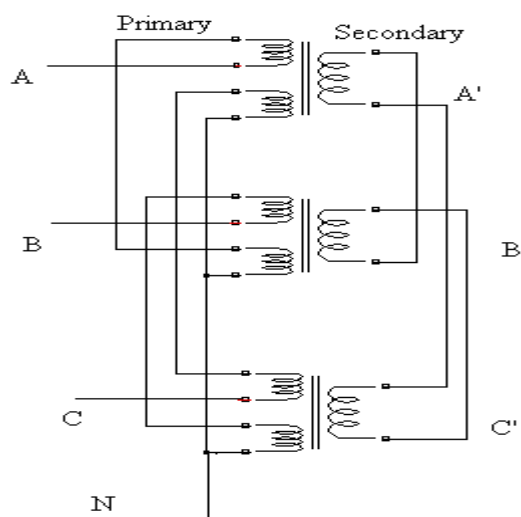


Fig. 3. (a) Zigzag-Delta Transformer Connection.

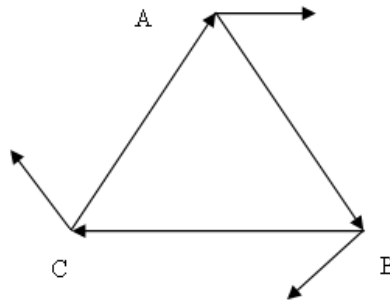


Fig. 3. (b) Phasor diagram.

Delta connected secondary winding transformer will force the triplen harmonics to circulate at its secondary winding and eliminated balanced triplen harmonics. From the phasor diagram Fig. 1(b), it can be found that the voltage across the transformer's winding is  $\frac{1}{\sqrt{3}}$  of the phase voltage of the three-phase four-wire distribution power system.

### III. CONTROL OF DSTATCOM

The control approaches available for the generation of reference source currents for the control of VSC of DSTATCOM for three-phase four-wire system are instantaneous reactive power theory (IRPT), synchronous reference frame theory (SRFT), unity power factor (UPF) based, instantaneous symmetrical components based, etc. [12], [13]. The SRFT is used in this investigation for the control of the DSTATCOM. A block diagram of the control scheme is shown in Fig. 4. The load currents ( $i_{La}$ ,  $i_{Lb}$ ,  $i_{Lc}$ ), the PCC voltages ( $V_{Sa}$ ,  $V_{Sb}$ ,  $V_{Sc}$ ), and dc bus voltage ( $V_{dc}$ ) of DSTATCOM are sensed as feedback signals. The load currents from the a-b-c frame are first converted to the  $\alpha$ - $\beta$ -0 frame and then to the d-q-0 frame using

$$\begin{bmatrix} \dot{i}_{Lq} \\ \dot{i}_{Ld} \\ \dot{i}_{L0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos \theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin \theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} \dot{i}_{La} \\ \dot{i}_{Lb} \\ \dot{i}_{Lc} \end{bmatrix} \quad (4)$$

where  $\cos \theta$  and  $\sin \theta$  are obtained using a three-phase phase-locked loop (PLL). A PLL signal is obtained from terminal voltages for generation of fundamental unit vectors [18] for conversion of sensed currents to the d-q-0 reference frame. The SRF controller extracts dc quantities by a low-pass filter, and hence, the non-dc quantities (harmonics) are separated from the reference signal. The d-axis and q-axis currents consist of fundamental and harmonic components as

$$\dot{i}_{Ld} = \dot{i}_{d\ dc} + \dot{i}_{d\ ac} \quad (5)$$

$$\dot{i}_{Lq} = \dot{i}_{q\ dc} + \dot{i}_{q\ ac} \quad (6)$$

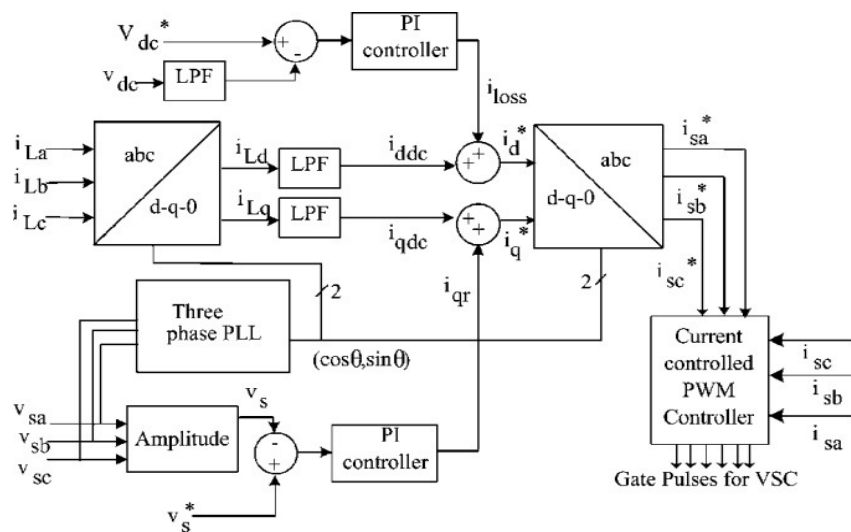


Fig. 4. Control algorithm for the three-leg-VSC-based DSTATCOM in a three-phase four-wire system.

### 3.1. UPF Operation of DSTATCOM

The control strategy for reactive power compensation for UPF operation considers that the source must deliver the mean value of the direct-axis component of the load current along with the active power component current for maintaining the dc bus and meeting the losses ( $i_{loss}$ ) in DSTATCOM. The output of the proportional-integral (PI) controller at the dc bus voltage of DSTATCOM is considered as the current ( $i_{loss}$ ) for meeting its losses

$$\dot{\mathbf{i}}_{loss(n)} = \dot{\mathbf{i}}_{loss(n-1)} + \mathbf{K}_{pd} (V_{dc(n)} - V_{dc(n-1)}) + \mathbf{K}_{id} V_{dc(n)} \quad (7)$$

where  $V_{de(n)} = V_{dc}^* - V_{dc(n)}$  is the error between the reference ( $V_{dc}^*$ ) sensed ( $V_{dc}$ ) dc voltages at the nth sampling instant.  $K_{pd}$  and  $K_{id}$  are the proportional and integral gains of the dc bus voltage PI controller. The reference source current is therefore

$$\dot{\mathbf{i}}_d^* = \dot{\mathbf{i}}_{d\ dc} + \dot{\mathbf{i}}_{loss} \quad (8)$$

The reference source current must be in phase with the voltage at the PCC but with no zero-sequence component. It is therefore obtained by the following reverse Park's transformation with  $i_d^*$  as in (12) and  $i_q^*$  and  $i_0^*$  as zero

$$\begin{bmatrix} \dot{\mathbf{i}}_a^* \\ \dot{\mathbf{i}}_b^* \\ \dot{\mathbf{i}}_c^* \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta & 1 \\ \cos(\theta - \frac{2\pi}{3}) & \sin(\theta - \frac{2\pi}{3}) & 1 \\ \cos(\theta + \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} \dot{\mathbf{i}}_d^* \\ \dot{\mathbf{i}}_q^* \\ \dot{\mathbf{i}}_0^* \end{bmatrix} \quad (9)$$

### 3.2. Zero-Voltage Regulation (ZVR) Operation of DSTATCOM

The compensating strategy for ZVR operation considers that the source must deliver the same direct-axis component  $i_d^*$ , as mentioned in (12) along with the sum of quadrature-axis current ( $i_{q\ dc}$ ) and the component obtained from the PI controller ( $i_{qr}$ ) used for regulating the voltage at PCC. The amplitude of ac terminal voltage ( $V_s$ ) at the PCC is controlled to its reference voltage ( $V_s^*$ ) using the PI

controller. The output of PI controller is considered as the reactive component of current ( $i_{qr}$ ) for zero-voltage regulation of ac voltage at PCC. The amplitude of ac voltage ( $V_s$ ) at PCC is calculated from the ac voltages ( $V_{sa}$ ,  $V_{sb}$ ,  $V_{sc}$ ) as

$$V_s = (2/3)^{1/2} (V_{sa}^2 + V_{sb}^2 + V_{sc}^2)^{1/2} \tag{10}$$

Then, a PI controller is used to regulate this voltage to a reference value as

$$i_{qr(n)} = i_{qr(n-1)} + K_{pq} (V_{te(n)} - V_{te(n-1)}) + K_{iq} V_{te(n)} \tag{11}$$

where  $V_{te(n)} = V_s^* - V_{S(n)}$  denotes the error between reference ( $V_s^*$ ) and actual ( $V_{S(n)}$ ) terminal voltage amplitudes at the  $n^{\text{th}}$  sampling instant.  $K_{pq}$  and  $K_{iq}$  are the proportional and integral gains of the dc bus voltage PI controller. The reference source quadrature-axis current is

$$i_q^* = i_{qdc} + i_{qr} \tag{12}$$

The reference source current is obtained by reverse Park's transformation using (13) with  $i_d^*$  as in (12) and  $i_q^*$  as in (16) and  $i_0^*$  as zero.

### 3.3. Computation of Controller Gains

The gains of the controllers are obtained using the Ziegler-Nichols step response technique [19]. A step input of amplitude (U) is applied and the output response of the dc bus voltage is obtained for the open-loop system. The maximum gradient (G) and the point at which the line of maximum gradient crosses the time axis (T) are computed. The gains of the controller are computed using the following equations:

$$K_p = \left| \frac{1.2U}{GT} \right| \tag{13}$$

$$K_i = \left| \frac{0.6U}{GT^2} \right| \tag{14}$$

The gain values for both the PI controllers are computed.

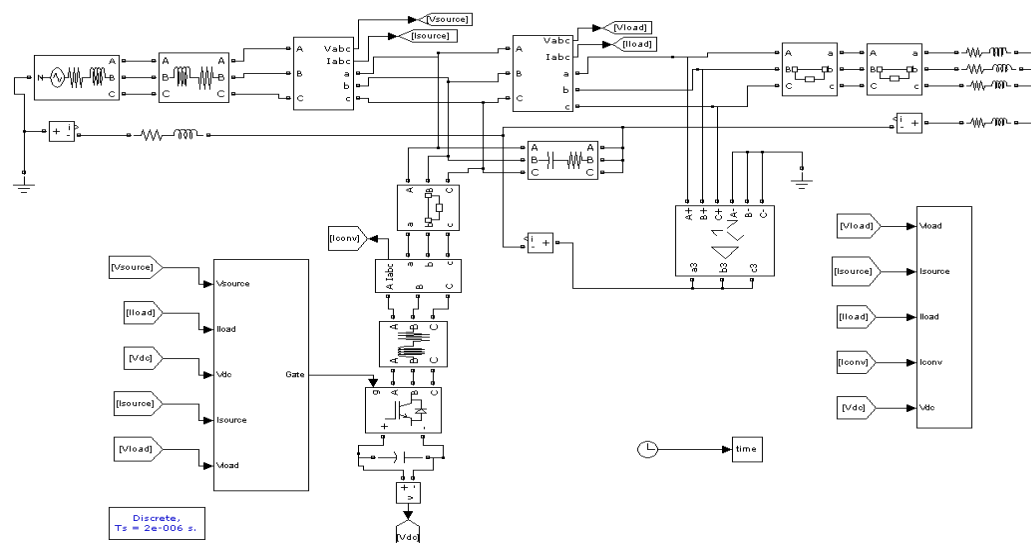


Fig. 5. MATLAB model of the Zigzag-delta configuration of the Phase-Shifting transformer and the three-leg

VSC based DSTATCOM connected system.

### 3.4. Current-Controlled Pulse Width Modulation (PWM) Generator

In a current controller, the sensed and reference source currents are compared and a proportional controller is used for amplifying current error in each phase before comparing with a triangular carrier signal to generate the gating signals for six IGBT switches of VSC of DSTATCOM.

## IV. MODELING AND SIMULATION

The three-leg VSC and the Phase-Shifting Transformer based DSTATCOM connected to a three-phase four-wire system is modeled and simulated using the MATLAB with its Simulink and PSBs. The ripple filter is connected to the DSTATCOM for filtering the ripple in the PCC voltage. The MATLAB-based model of the three-phase four-wire DSTATCOM is shown in the Fig.5. The Phase-Shifting transformer in parallel to the load, the three-phase source, and the shunt-connected three-leg Voltage Source Converter are connected as shown in the Fig.5. The available model of Zigzag Phase-Shifting transformer is used for modeling the Zigzag-delta configuration of the Phase-Shifting transformer.

The control algorithm for the DSTATCOM is also modeled in MATLAB. The reference source currents are derived from the sensed PCC voltages ( $V_{sa}$ ,  $V_{sb}$ ,  $V_{sc}$ ), load currents ( $i_{La}$ ,  $i_{Lb}$ ,  $i_{Lc}$ ) and the dc bus voltage of DSTATCOM ( $V_{dc}$ ). A PWM current controller is used over the reference and sensed source currents to generate the gating signals for the IGBTs of the VSC of the DSTATCOM.

## V. RESULTS AND DISCUSSION

The performance of the Phase-Shifting Transformer and three-leg-VSC based three-phase four-wire DSTATCOM is demonstrated for power flow control, power factor correction and voltage regulation along with harmonic reduction, load balancing, and neutral current compensation. The developed model is analyzed under linear load the results are discussed shortly.

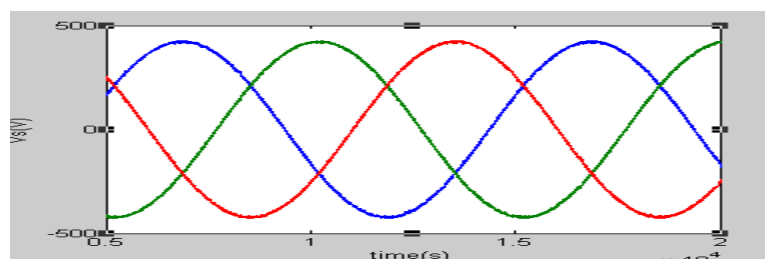


Fig. 6.(a) PCC Voltage (V)

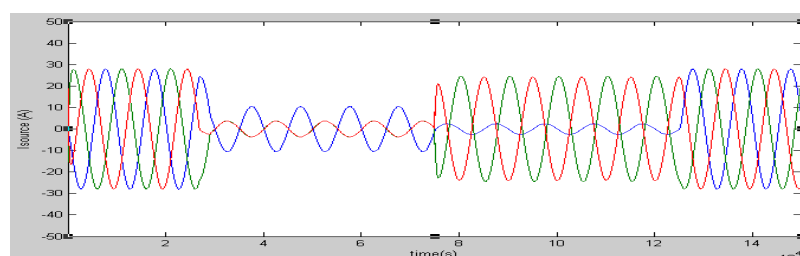


Fig. 6.(b) Source current (A)



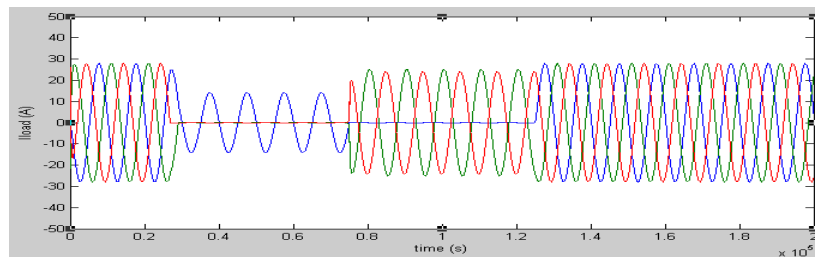


Fig. 6.(c) Load current (A)

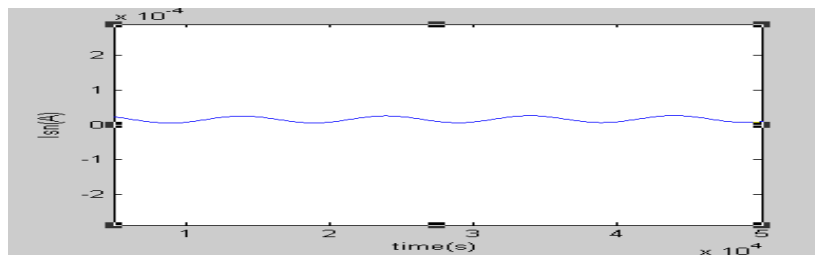


Fig. 6.(d) Source-neutral current (A)

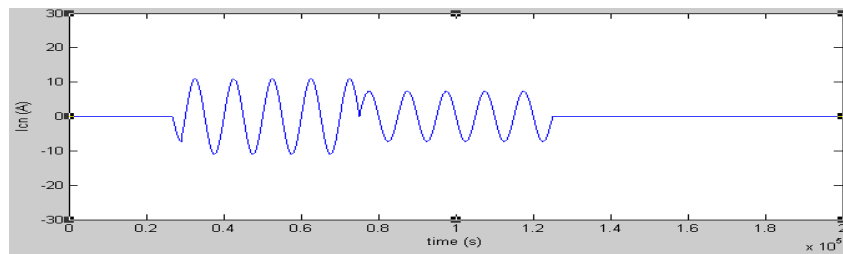


Fig. 6.(e) Compensator-neutral current (A)

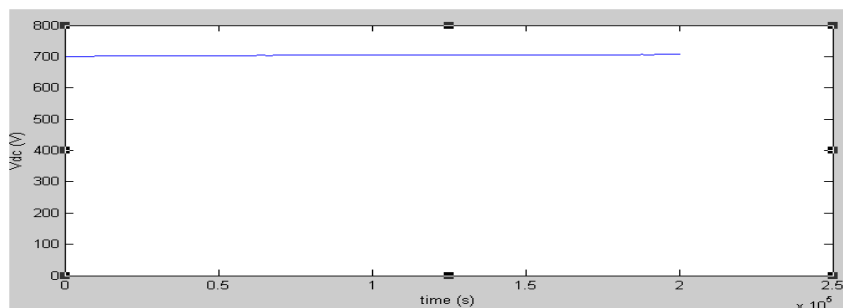


Fig. 6.(f) DC Bus Voltage (V)

### 5.1. Performance of DSTATCOM with linear load for Neutral Current Compensation, Load Balancing, UPF Operation and Zero-Voltage Regulation Operation

The dynamic performance of the DSTATCOM under linear lagging power factor unbalanced load condition is shown in Fig. 6. At 0.6 s, the load is changed to two-phase load and to single-phase load at 0.7 s. These loads are applied again at 0.8 and 0.9 s, respectively. The PCC voltages ( $V_s$ ), source currents ( $i_s$ ), load currents ( $i_L$ ), compensator currents ( $i_c$ ), source-neutral current ( $i_{sn}$ ), load-neutral current ( $i_{Ln}$ ), compensator-neutral current ( $i_{cn}$ ), dc bus voltage ( $V_{dc}$ ), and amplitude of voltage ( $V_s$ ) at PCC are also depicted in Fig. 6. The source-neutral current is observed as nearly zero, and this verifies the proper compensation. The reactive power is compensated for power factor correction, and the source currents are balanced and sinusoidal. It is also observed that the dc bus voltage of DSTATCOM is able to maintain close to the reference value under all disturbances. Its total harmonic

distortion is low. The amplitude of PCC voltage is maintained at the reference value under various load disturbances, which shows the ZVR mode of operation of DSTATCOM.

## 5.2. Experimental Demonstration of the Performance of Zigzag Phase-Shifting Transformer

The proposed topology of DSTATCOM consists of combined operation of three-leg VSC and a Zigzag Phase-Shifting transformer. As the performance of a three-leg VSC and a zig-zag transformer is studied in [9], the Zigzag-delta configuration of the Phase-Shifting transformer is analyzed for the compensation of neutral current. A prototype of the Zigzag-delta configuration of the Phase-Shifting transformer is developed in the laboratory and the neutral current compensation technique is tested for linear and nonlinear loads. The Phase-Shifting transformer is tested for neutral current compensation under unbalanced linear loads and balanced/unbalanced nonlinear loads. When the load is nonlinear and balanced, the load-neutral current is observed to be mainly triplen harmonics current, and this is compensated using the Phase-Shifting transformer.

## VI. COMPARISON WITH OTHER TECHNIQUES

A three-leg single-phase-VSC-based DSTATCOM [3] requires a total of 12 semiconductor devices, and hence, is not attractive, and the three-leg VSC with split capacitors [3] has the disadvantage of difficulty in maintaining equal dc voltage at two series-connected capacitors. The four-leg-VSC-based DSTATCOM [3] is considered as superior considering the number of switches, complexity, cost, etc. The proposed three-phase-four-wire DSTATCOM is based on a three-leg VSC and a Phase-Shifting transformer. A three-leg VSC with zig-zag and delta configuration of Phase-Shifting transformer has the advantage of using a passive device for neutral current compensation, reduced number of switches, use of readily available three-leg VSC, etc. It is observed that the KVA rating of the PST is less compared to the T-connected transformer. Similarly, comparison with the four-leg converter shows that the number of switches are reduced in the proposed configuration, thus reducing the complexity and cost of the system. The total harmonic distortion of the Zigzag-delta configuration of the Phase-Shifting transformer is less compared to any other techniques. The advantage of the PST is that their low MVA capacity and it improves the stability of the power system. The T-connected transformer requires two single-phase transformers, whereas the zig-zag transformer reported in [9] has three single-phase transformers with a turn's ratio of 1:1. A star/delta transformer is also reported [20] for neutral current compensation and the kVA rating required is higher compared to Phase-Shifting transformer. Table I shows the rating comparison of the three transformer techniques for a given neutral current of 10 A. But the disadvantage of the proposed topology is that it requires the protection of PST.

**Table 1.** Comparison of Rating of Transformer Connections.

Transformer	Winding Voltage (V)	Winding Current (A)	KVA	Total KVA
T-connected	240/120/120	10	2.4	4.48
	208/208		2.08	
Star/Delta	240/240	10	2.4	7.2
Zigzag Phase-Shifting	120/120	10	1.4	4.2

## VII. CONCLUSION

The performance of a new topology of three-phase four-wire DSTATCOM consisting of three-leg VSC with a PST has been demonstrated for reactive power compensation, harmonic elimination, load balancing and mitigating circulating power flows in interconnected utilities. The voltage regulation and power factor correction modes of operation of the DSTATCOM have been observed and are as

expected. The PST improves the transient stability of a power system. It is also observed that the Phase-Shifting transformer helps in damping low frequency power oscillations. The dc bus voltage of the DSTATCOM has been regulated to the reference dc bus voltage under varying loads. The total kilovolt-amperes rating of the PST is lower than the T-connected transformer for reactive power compensation. The PST has verified that it is effective in compensating the reactive power, zero sequence fundamental and harmonic currents. We found that harmonic mitigation techniques using Zigzag-delta transformers are a viable choice for mitigating rich triplen harmonics in four-wire electrical distribution system. As comparison made in term of costs, Zigzag-delta Phase-Shifting transformers show that low cost as to compare with active filter and other types of harmonic mitigation. The proposed approach is much simpler, cheaper and reliable compared to approaches using active filters. The costs comparison with active filter as shown below:

Active Filter – RM1750/kVA

Transformer – RM 300/kVA

Zigzag-delta Phase-Shifting transformers are also significantly reduced neutral current flowing back to the system almost up to 90%.

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