DESIGN OF A SQUAT POWER OPERATIONAL AMPLIFIER BY FOLDED CASCADE ARCHITECTURE

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ABSTRACT

The objective of this paper is to implement the full custom design of low voltage and low power operational amplifier which operates at high frequency, which is applicable for the Micro Electronics and Telecommunications. In order to design the low power operational amplifier, certain compensation techniques are used. At the input side, transconductance removal technique was used by using the complimentary differential pair. At the output side, to achieve high swing output, class AB output stage was used. The operational amplifier is used to implement the ADC circuit. This paper will briefly outline the performance of operational amplifier operating at lower supply voltages. In this paper each individual parameter is measured. Simulations of the entire paper are implemented in CADENCE software.

KEYWORDS: *AC-DC Response, Gain, Bandwidth, Slew Rate..*

I. INTRODUCTION

Operational amplifier, which has become one of the most versatile and important building blocks in analog circuit design. There are two operational amplifiers developed. Operational Tran conductance amplifiers (unbuffered) have the output resistance typically very high. The other one is the buffered amplifiers (voltage operational amplifier) typically low output resistance. Operational amplifiers are amplifiers (control sources) that have high forward gain so that when negative feedback is applied, the closed loop transfer function is practically independent of the gain of operational amplifier. This principle has been exploited to develop many useful analog circuits and systems. The primary requirement of an operational amplifier is to have an open loop gain that is sufficiently large to implement the negative feedback concept. The figure shows the block diagram that represents the important aspects of an operational amplifier. CMOS operational amplifiers are very similar in architecture to their bipolar counter parts.Improvements in processing have pushed scaling of device dimensions persistently over the past years. The main drive behind this trend is the resulting reduction in IC production cost since more components on a chip are possible. In addition to device scaling, the increase in the portable electronics market is also encouraging low voltage and low power circuitry since this would reduce battery size and weight and enable longer battery life time

II. OP-AMP SPECIFICATIONS

The key criterion of this paper is to operate with +1.2V power supply and achieve large signal to noise ratio while maintaining ≤2mW power consumption, ≤10ns settling time, and reasonable gain. The table shows the full detailed specifications. The operational amplifier drives the capacitive load of 5pF.

Table 1: Op-Amp Parameters

Performance parameter	Design goal
Swing(>20% inc. gain)	Close to rails
Total power	Low
0.1%Settling Time	<100ns
Slew rate	>200V/µs
Gain(DC)	>(70db)
Phase margin	45 to 60
Unity gain frequency	>110MHz
CMRR	Max
PSRR+	Max

2.1. Input Stage

To keep the signal-to-noise ratio as large as possible particularly in non-inverting op amp circuits, the common mode input voltage should be kept as wide as possible. This can be accomplished by placing N-type and P-type input pairs in parallel. By placing two complementary differential pairs in parallel, it is possible to obtain a rail-to-rail input stage. The NMOS pair is in conduction for high input common-mode voltages while the PMOS pair is in conduction for low input common mode voltages and the both differential pairs can operate together for middle values of the input common-mode voltage. In this case, the total trans-conductance of the input stage is not constant It is also possible to obtain a constant trans-conductance; for low-input common-mode voltages only the PMOS pair is active, where for high ones only the NMOS pair is in conduction. For middle values, both pairs are "ON," but each with reduced contribution (exactly the half in the "crossing point" condition). The constant- operation with low supply voltages is achieved by designing input transistors with large aspect ratios operating in weak inversion Since the input transistors are in weak inversion, the input transconductance is the same for low and high-input common-mode voltages. For "middle" values of common-mode input voltages, a reduced value of current flows in both the input pairs which is exactly half of the value compared to low and high common inputs. Consequently, the input transconductance is always the same. The input stage mainly comprises of the CMOS complementary stage which consists of an N-differential pair and a P-differential pair to keep the signal-to-noise ratio as large as possible. The current bias transistors are used to keep the current flowing in the differential stage is constant. A much more serious drawback though is the variation of the input stage transconductance, g_m with the common-mode input voltage. So that one to three mirrors have been used with the transistors operating in strong inversion, reducing the variation to about 15%, using a 1.8-V minimum supply voltage.

2.2. Output Stage

When designing a low power Operational amplifier, the output stage becomes the fundamental block because it significantly affects the final features of the whole circuit such as power dissipation, linearity and bandwidth. The performance of output stages is measured in terms of dissipation (or efficiency), output swing, drive capability, and linearity. Efficiency generally depends on the bias current, which, being a trade-off between power dissipation and bandwidth, must be properly controlled. Moreover, the output swing is maximized by adopting push-pull topologies while the drive capability is guaranteed by an appropriate choice of the aspect ratio of the final transistors. As a consequence, linearity, which strictly depends on the above parameters, is often sacrificed and its final value is determined by the topology adopted. It consists of a push-pull pair, M_N and M_P, and a driver circuit made up of transistors M1-M6 and two current generators, I_B. The stage exhibits high linearity provided that the driver structure is symmetrical that is, transistors MiA and MiB must have the same aspect ratio.

III. ANALYSIS OF VARIOUS PARAMETERS

3.1. Input Stage

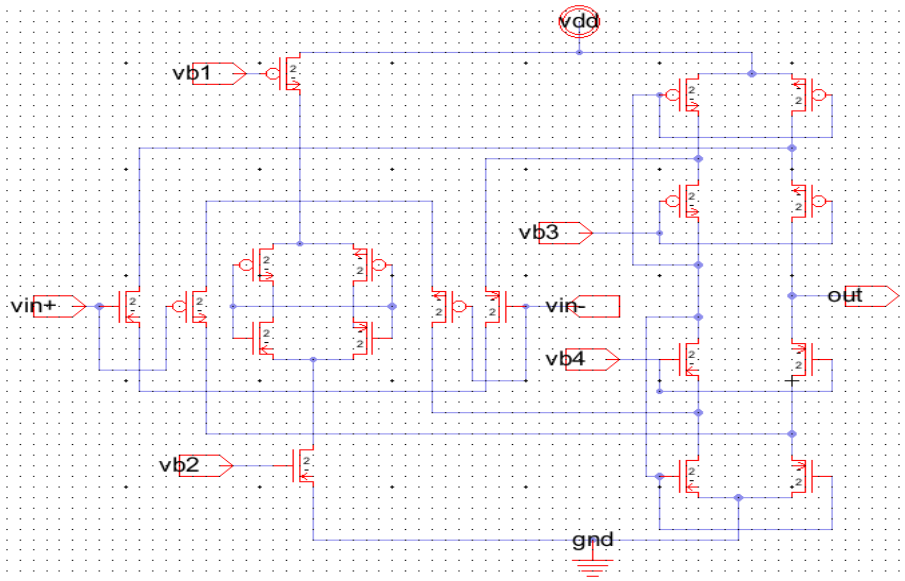

Fig 1: Input Stage Schematic

Table 2: W/L ratios of Input stage transistors

Name of the Transistor	W/L Ratio's (µm/ µm)	M
M1, M2	72/1	1
M3, M4	181/1	1
M5	361/1	1
M6	145/1	1
M7, M8	542/1	1
M9, M10	217/1	1
M11, M12	551/1	1
M13, M14	734/1	1
M15, M16	289/1	1
M17, M18	361/1	1

3.2 Output Stage

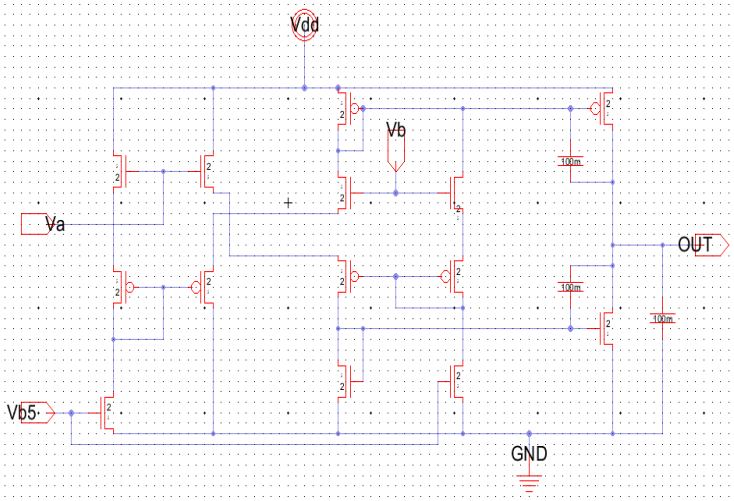

Fig 2: Output Stage Schematic

Table 3: W/L ratios of Output stage transistors

Name of the Transistor	W/L Ratio's (µm/ µm)	M
MN	127/1	2
MP	322/1	2
M4A, M4B	26/1	1
M1A, M1B	42/1	1
M2A, M2B	127/1	1
M3A,M3B	9/1	1
M5	9/1	1
M6	22/1	1

3.3 Complete Operational Amplifier:

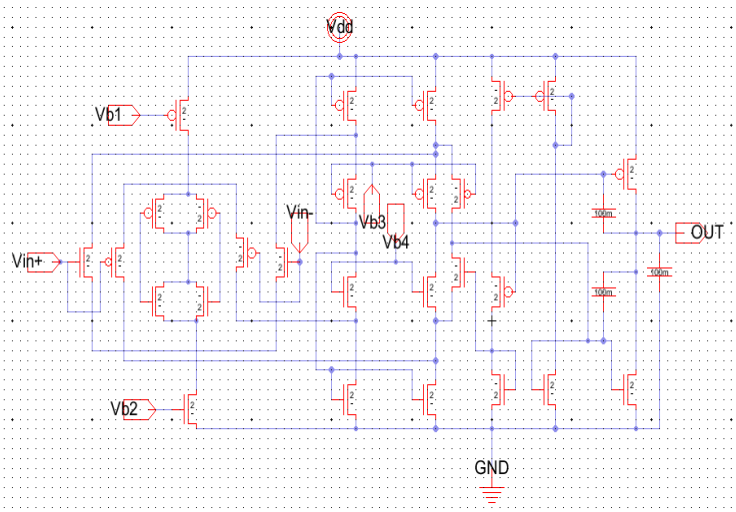

Fig 3: Complete Operational Amplifier Schematic

Table 4: W/L ratios of Complete Op-Amp transistors

Name of the Transistor	W/L Ratio's(µm/ µm)	M
M1, M2	72/1	1
M3, M4	181/1	1
M5	361/1	1
M6	145/1	1
M7, M8	542/1	1
M9, M10	217/1	1
M11, M12	551/1	1
M13	734/1	1
M14, M19	367/1	1
M15	289/1	1
M16, M20	195/1	1
M17, M18	361/1	1
M21,M22,M23	15/1	1
M24	6/1	1
M25	0.3/1	1
M26	322/1	2

M27	127/1	2

3.4 AC Response

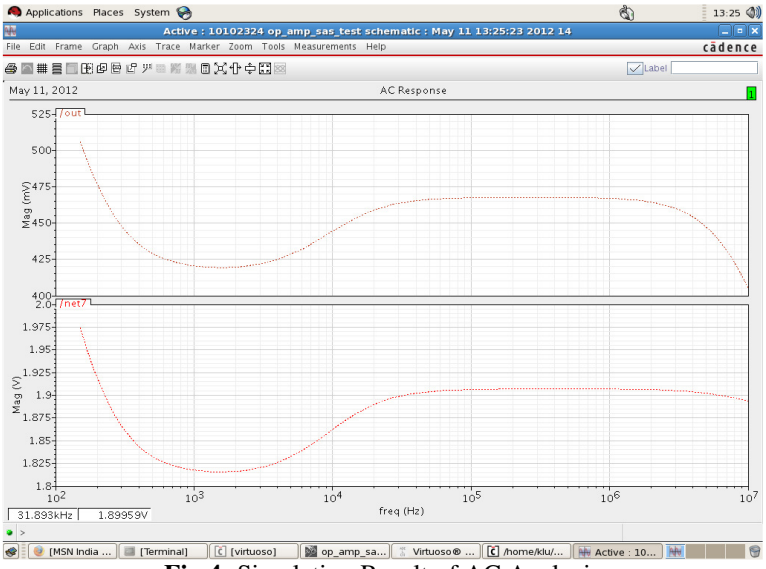

Fig 4: Simulation Result of AC Analysis

3.5 DC Response

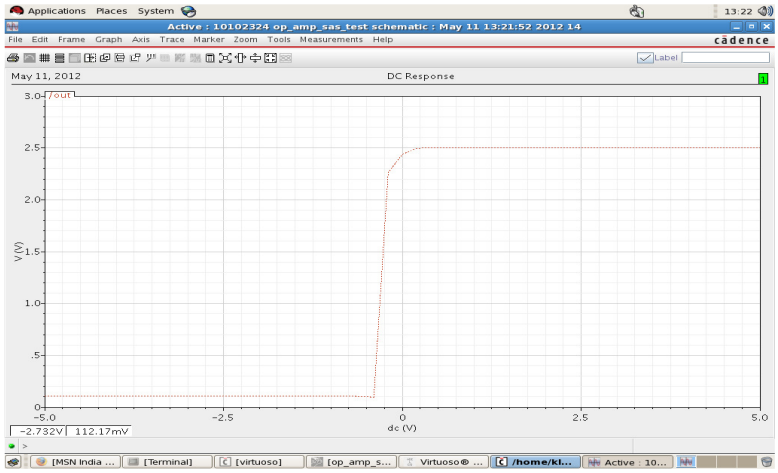

Fig 5: Simulation Result of DC Analysis

3.6 Gain Margin

Reciprocal of the open loop voltage gain at the frequency where he open loop phase shift first reaches -180^0

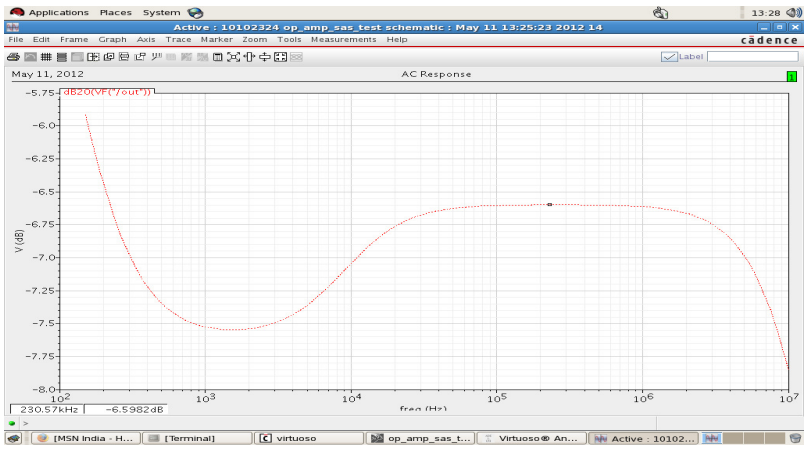

Fig 6: Simulation Result of Gain

3.7 Bandwidth

The range of frequencies with in which the gain is ± 0.1 dB of the nominal value. An ideal operational amplifier has an infinite frequency response and can amplify any frequency signal from DC to the highest AC frequencies so it is therefore assumed to have an infinite bandwidth. With real op-amps, the bandwidth is limited by the Gain-Bandwidth product (GB), which is equal to the frequency where the amplifiers gain becomes unity.

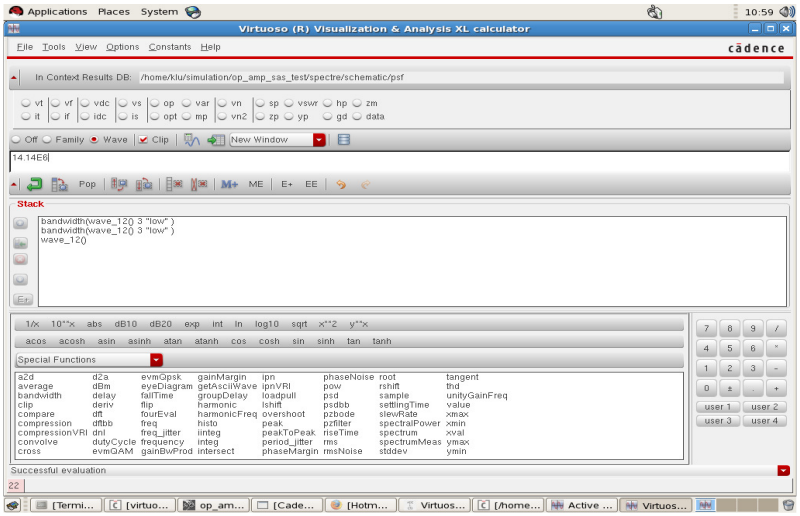

Fig 7: Simulation Result of Bandwidth

3.8 Gain Bandwidth Product

GBW defines the gain behaviour of op-amp with frequency. It is constant for voltage-feedback amplifiers. It does not have much meaning for current-feedback amplifiers because there is not a linear relationship between gain and bandwidth.

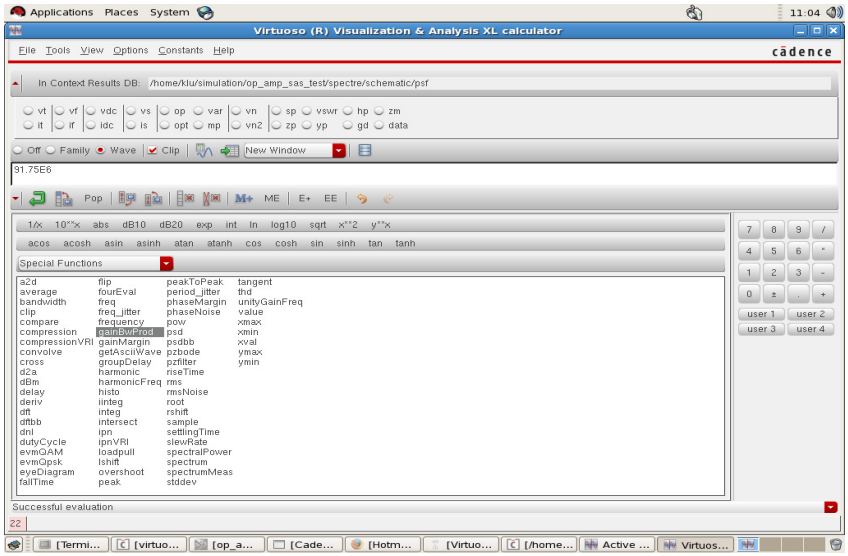

Fig 8: Simulation Result of Gain Bandwidth Product

3.9 Phase Margin

It is a measure to find the stability of the amplifier. It is the phase difference between open loop gain and -180^0 when open loop gain is at unity

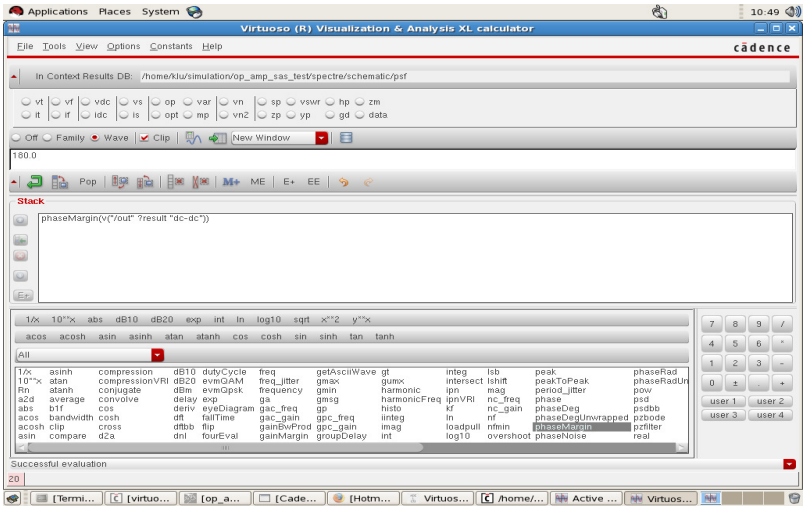

Fig 9: Simulation Result of Phase Margin

3.10 Settling Time

The settling time is the time it takes for the signal to settle within a certain wanted range. With a step change at the input, the time required for the output voltage to settle within the specified error band of the final value

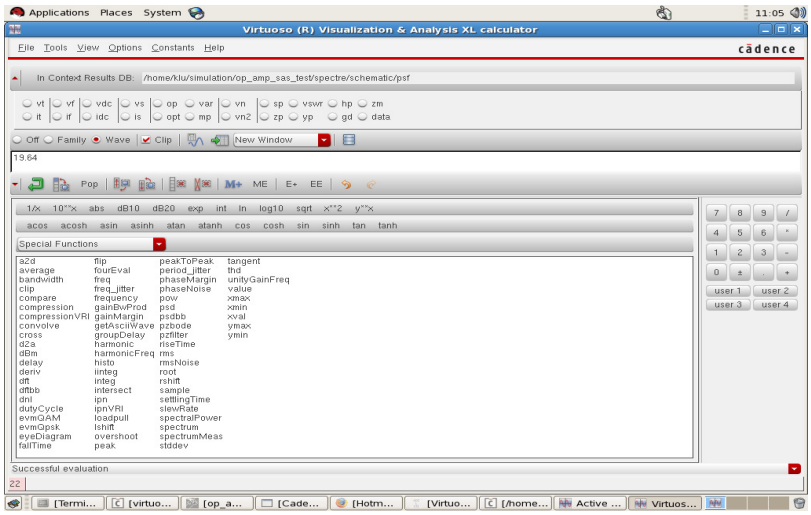

Fig 10: Simulation Result of Settling Time

3.11 Slew Rate

Slew rate is the maximum rate at which the voltage at the output can change. Slew rate is related to bandwidth of the amplifier. It is usually expressed in Volts per microsecond.

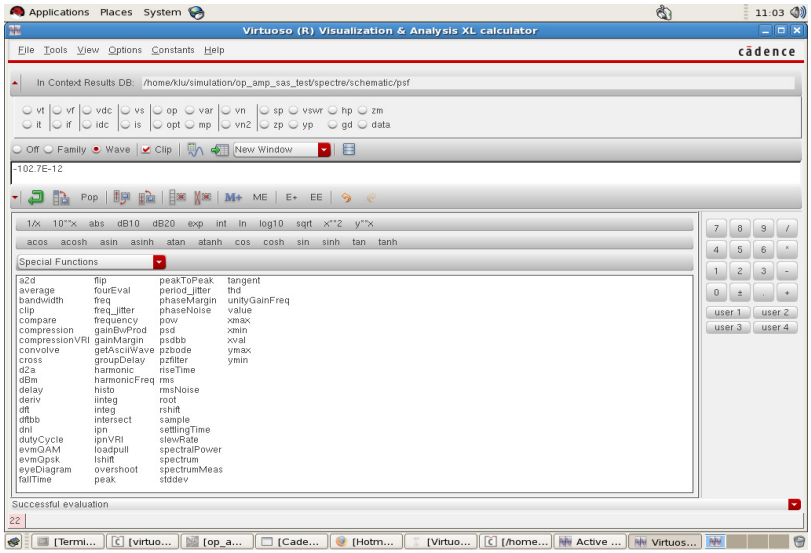

Fig 11: Simulation Result of Slew Rate

In general terms the higher the slew rate the higher the bandwidth, and the higher the maximum frequency that the op-amp can handle.

3.12 Unity Gain Frequency

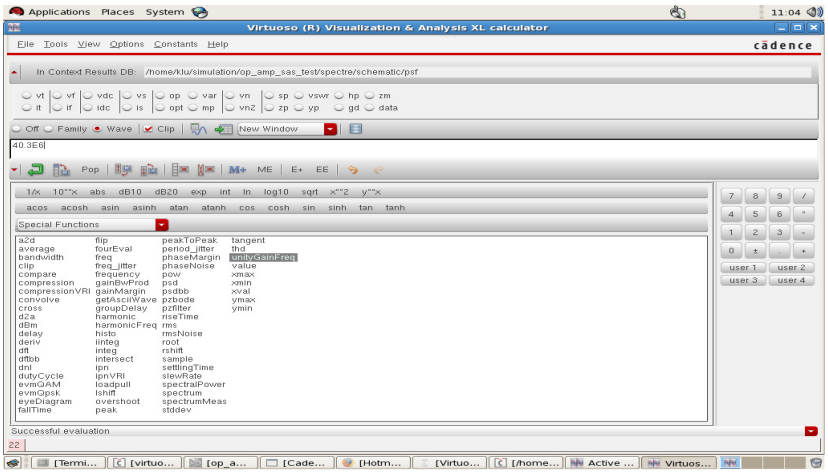

Fig 12: Simulation Result of Unity Gain Frequency

3.13 Transient Response

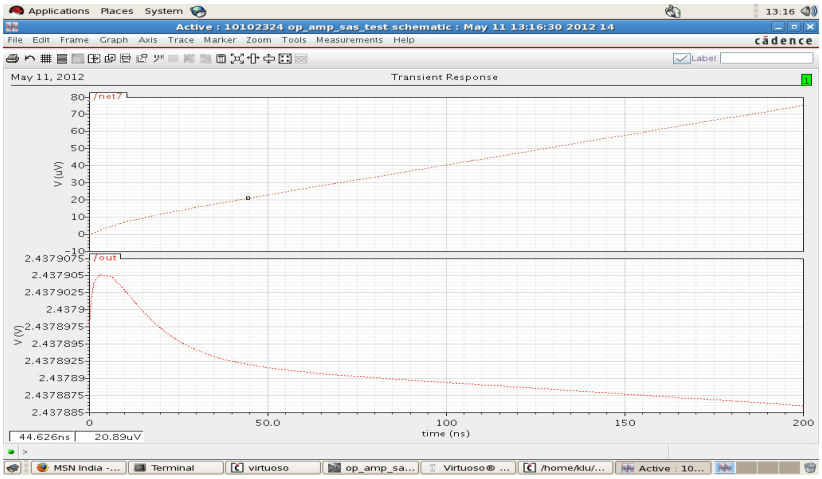

Fig 13: Simulation Result of Transient Response

3.14 Power Calculation

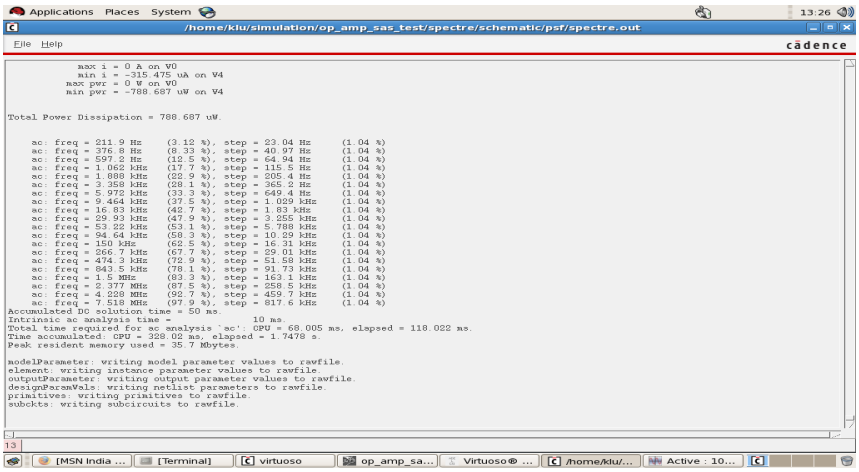

Fig 14: Result of Power Calculation

IV. CONCLUSIONS

In this paper, the design of low power high frequency OPAMP using frequency compensation technique has been implemented which is mainly used in the high frequency and low power applications. The operational amplifier is designed by selecting the folded cascode architecture. After designing the low power Op-Amp, in order to increase the frequency response of the Op-Amp, current buffer compensation technique was used and attained the higher frequency response as compared to the previous response. First one is the input stage which consists of the differential N-pair and P-pair. By using this differential pair the transconductance of the operational amplifier is not constant.To reduce the transconductance and to attain low power application requirement, complementary circuit was used. So extra circuitry, constant transconductance stage is used to make it constant. The second stage is the current summing stage. The third stage is the output buffer stage which consists of CMOS complementary class- AB output stage. At the output stage, to attain the maximum output from the input, push pull stage was used. Current Buffer compensated op-amp there is improvement of bandwidth, gain, phase margin, CMRR, Slew rate but power dissipation increases and PSRR decreases. Also, area requirement for current buffer compensation technique is very less as compared to other compensation techniques and also the compensation capacitor is less for current buffer compensated op-amp as compared to other compensation technique.

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