LOW POWER SEQUENTIAL ELEMENTS FOR MULTIMEDIA AND WIRELESS COMMUNICATION APPLICATIONS

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ABSTRACT

In integrated circuits, power consumption is a one of the top three challenges like area, power and speed. Power optimization of IC's can be achieved in gate level, logical level, algorithmic level and circuit level (transistor level). From these levels one of the best optimization is transistor level, because the structure of the transistor will play a major role in power dissipation. Practically, clocking system consumes large portion of total chip power which consists of clock distribution network and flop-flops. Various design techniques are available to reduce the flip flop power. In this paper removal of noise coupling transistor approach is implemented in new flip flop then further power reduction is carried out by employing already existing methods like double edge triggering and SVL method. Based upon those techniques, the proposed flip flops in this paper having improved power reduction capability than existing flip flop by 6%~90% and improved PDP by 9%~90%. Some of the proposed flip flops are used in multimedia and error detector application.

KEYWORDS: *Flip-flops, low power, Double edge Triggering, SVL, Delay buffer, Error detector.*

I. INTRODUCTION

In current scenario the requirement of portable equipment is increasing rapidly like Pocket calculators, Hearing aids, Wristwatches etc. Portability is achieved by System-on-chip designs (SoC), which hold multiple functions "systems" on a single silicon chip like processor, bus and other elements on a single monolithic substrate. Next approach for portability is battery. For some applications, heavy battery pack up is not possible in practice and frequent recharge is inconvenient. Aggressive design rules will increase circuit density, and improve overall chip performance. If design rules are too aggressive then complexity arises in manufacturing. On the other hand, slack design rules may result in increased die size, delays, and lower chip performance.

If density of chip goes on increasing means heat will be dissipated due to the high power consumption. Some cooling systems like heat sinks, refrigeration cooling systems, and water cooled heat exchanger are used to reduce the heat. It has limited ability to remove the excess heat. The requirement of sophisticated cooling systems and high cost battery is reduced linearly, if we are reducing the interior power in integrated chip. From the high performance microprocessor design, clocking systems consumed 40% of the chip power; thermal management was a major concern [1]. Low power flip flop design will play a vital role in high performance system design.

There is a wide variety of low power flip flops are available in the literature [2] – [7]. For example HLFF [2], SDFF [3] called as fastest flip flop but they are consuming large amount of power due to redundant switching activity in the internal nodes. Low swing clock double edge trigger flip flop (LSDFF [4]), using low swing voltage and double edge triggering method to reduce the power consumption. Clock gatting techniques also used to reduce the flip flop power by disable the clock signal when particular block is idle condition, example GMSFF [5].

This paper organized as follows: Section II deals with power reduction techniques for proposed flip flops. Section III presents existing flip flops. The proposed flip flops are explained in Section IV. In Section V, application of proposed flip flops is explained and Section VI shows the simulation results. Section VII concludes this paper. Finally Section VIII gives the future work.

II. LOW POWER FLIP FLOP DESIGN SURVEY

There are three source of power dissipation in digital complementary metal-oxide-semiconductor (CMOS) circuit. That is static power dissipation, dynamic power dissipation and short circuit power dissipation. Dynamic and short circuit power dissipation fall under the category of Transient Power Dissipation. Static power dissipation is due to leakage currents.

$$P=P_{dynamic} + P_{short\ circuit} + P_{leakage} \qquad (1)$$

Dynamic Power is also called as switching Power. It is caused by continuous charging and discharging of output parasitic capacitance. Short circuit power is the result when pull up and pull down network will conduct simultaneously. Leakage power dissipation arises when current flow takes place from supply to ground in idle condition. Power consumption is directly proportional to supply voltage, frequency and capacitance.

2.1. Low Power flip flop design Techniques

There are many low power techniques available to reduce the flip flop power like Low swing Voltage[4], Conditional operation [6], Double Edge triggering [7][8], Clock gating[5], Dual Vt/MTCMOS [9], Proposed Pulsed flip flop [17] and Reducing the capacity of clock load[10] etc. In this paper the Removal of noise coupling transistor, Double Edge triggering [8] and SVL [11] methods is used for proposed flip flops to reduce the total power consumption because, it can be easily incorporated in new flip flop.

2.1.1. Removal of Noise coupling Transistors

Sometimes, the flip flop will take wrong initial conditions due to noise coupling output, then false output is the result with more glitches.To avoid those draw backs we can eliminate the noise coupling transistors in the output as well as the input.

2.1.2. Double Edge Triggering

Most of the flip flops are designed to operate in single clock edge i.e. either in positive edge or negative edge. In double edge triggering [8] the flip flop is made to operate in both clock edges. With this method the opposite clock edge will not be wasted and speed of operation is increased.

2.1.3. Self Controllable Voltage Level Circuit

This SVL [11] method is implemented in memory circuits in prior papers to reduce the power consumption. In this paper the same SVL approach is applied to the new flip flop to reduce the leakage current and power which leads to total power reduction. Two blocks, Upper SVL and Lower SVL circuit will give the maximum V_{dd} and minimum *ground* level to the flip flop(load) when *active* mode. In other hand it will give lower V_{dd} and higher *ground* level to the load in *standby* mode.
The following sections will describe about existing flip flops and proposed flip flops with above said methods in detail.

III. EXISTING FLIP FLOPS

3.1 Clocked Pair Shared Flip Flop

This existing low power flip flop [12] is the improved version of Conditional Data Mapping Flip flop (CDMFF[10]). It has totally 19 transistors including 4 clocked transistors as shown in figure 1. The N3 and N4 are called clocked pair which is shared by first and second stage. The floating problem is avoided by the transistor P1 (always ON) which is used to charge the internal node *X*. This flip flop

will operate, when *clk* and *clkdb* is at logic *'1'*. When *D*=1, *Q*=0, *Qb_kpr*=1, N5=OFF, N1=ON, the *ground* voltage will pass through N3, N4 and N1 then switch on the P2. That is *Q* output pulls up through P2. When *D*=0, *Q*=1, *Qb_kpr*=0, N5= ON, N1= OFF, *Y*=1, N2= ON, then *Q* output pulls down to zero through N2, N3 and N4.

The flip flop output is depending upon the previous output *Q* and *Qb_kpr* in addition with clock and data input. So the initial condition should be like when *D*=1 the previous state of *Q* should be *'0'* and *Qb_kpr* should be *'1'*. Similarly when *D*=0 the previous state of *Q* should be *'1'* and *Qb_kpr* should be *'0'*. Whenever the *D*=1 the transistor N5 is idle, Whenever the *D*=0 input transmission gate is idle.

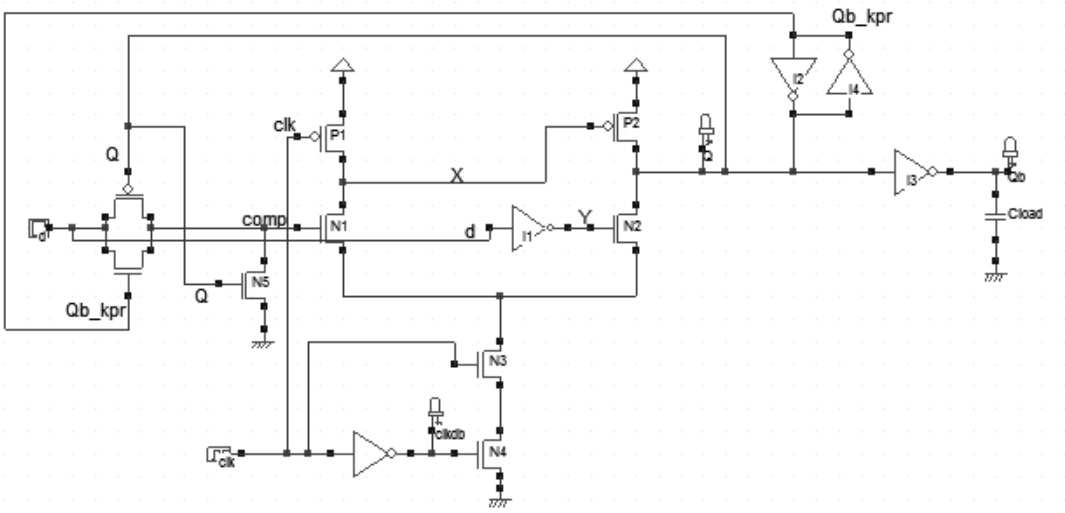


Figure 1. Clocked Pair Shared Flip Flop

In high frequency operation the input transmission gate and N5 will acquire incorrect initial conditions due to the feedback from the output. The noise coupling occurred in the *Q* output due to continuous switching at high frequency. The glitch will be appearing in the *Q* output. It will propagate to the next stage which makes the system more vulnerable to noise.

In order to avoid the above drawbacks and reduce the power consumption in proposed flip flop, we can make the flip flop output as independent of previous state. That is without initial conditions and removal of noise coupling transistors. In addition double edge triggering [8] can be applied easily for power reduction to the proposed flip flop. It will be a less power consumption than other flip flops.

3.2 Five Transistor True single Phase Clocked Flip flop

The schematic of 5T-TSPC flip-flop is shown in figure 2. It consists of 3-NMOS and 2-PMOS transistor [13]. It is positive edge triggered D latch. When *clk=1, D=1,* then M2=M3=M4=ON and M1=M5=OFF, output becomes high [13]. The drawback of this flip flop is high leakage power in lower technology. The leakage power increases as technology is scaled down.

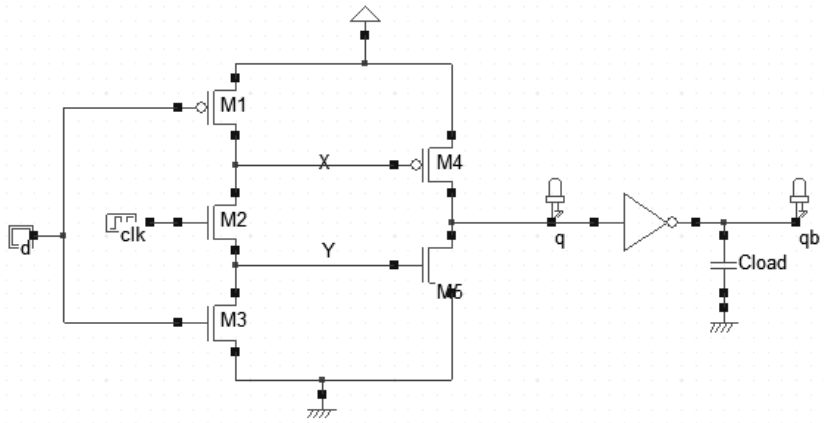


Figure 2. 5T-TSPC Flip Flop

This leakage power is reduced by using best technique among all run time techniques. The newly-developed leakage current reduction circuit called a "Self-controllable Voltage Level (SVL) [11]" circuit is implemented in proposed flip flop in order to reduce the leakage power. Formerly this SVL circuit is used for reducing the power in memory cell like SRAM. Now it can be applicable for flip flops. Double edge triggering method also implemented to proposed flip flop.

IV. PROPOSED FLIP FLOPS

4.1 Direct Data Clocked Pair Shared Flip Flop

This is the first proposed flip flop called DDCPSFF. The noise coupling transmission gate, N5 and output inverters I2 and I4 is removed in CPSFF discussed in Section 3.1. The data is applied to N1 directly, instead of applying through the transmission gate, named as Direct Data Clocked Pair Shared Flip Flop. So the power consumption is reduced than the CPSFF. Compared to a static D-flip-flop, the absence of feedback loops leads to an increase in speed. The data signal does not need to overwrite nodes.

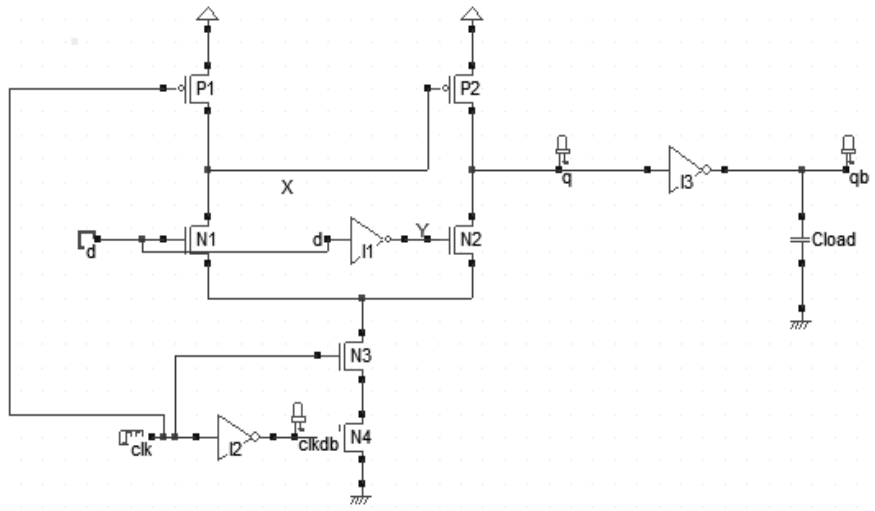


Figure 3. Direct Data Clocked Pair Shared Flip Flop

Feedback-inverters are also writing to this, holds only for circuits where the feedback cannot be disconnected by clocked transmission gates. However, these disconnecting transmission gates lengthen the feedback path and require proper clocking to turn off immediately [14]. The schematic of DDCPSFF is shown in the figure 3. The total number of transistor is *twelve* and number of clocked transistor is *four*. So it will lead to 37% of transistor reduction than CPSFF. If the number of transistor is reduced the power consumption is also reduced.

Whenever *clk* and *clkdb* is high the output follows the input. If *d=1* and *clk=0*, the node *X* pre-charge to vdd through the P1, i.e. the node *X* act as a capacitor. This phase is called pre-charging phase. Then *d=1* and *clk=1*, the MOSFET N1, N3, N4 is switched ON and P1 is Switched OFF and P2 is ON, the node *X* is discharged to *GND*. Then *q=1*. This phase is called evaluation phase. The analysis is extended to other input combination in the same manner. The glitches are reduced in this flip flop. Simulated results will be explained in the Section VI.

4.2 Double Edge Triggered DDCPSFF

In double edge triggering flip flop the number of clocked transistor is high than single edge triggering flip flop. This method is preferable to the circuits which consist of reduced number of clocked transistors. In dual edge triggering the flip flop is triggered in both edges of clock pulses. So the half of the clock operating frequency is enough and it will reduce the power consumption.

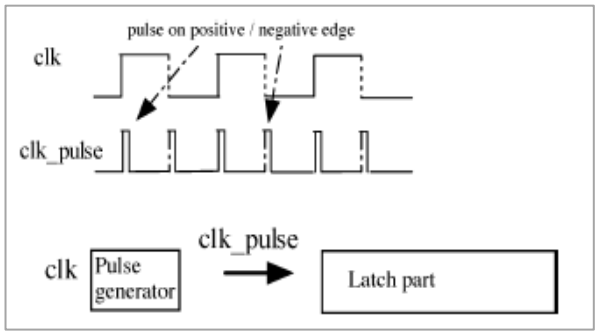


Figure 4. Dual Pulse Generator scheme

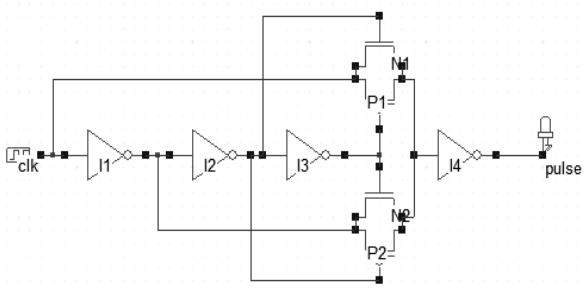


Figure 5. Dual Pulse Generator Circuit

Instead, applying the clock signal to the flip flop the dual pulse is applied using dual pulse generator scheme [8] shown in figure 4. The flip flop will evaluate the output in both edge of the clock.

4.2.1. Dual Pulse Generator Circuit

The pulse generator consists of two transmission gates and four inverters shown in figure 5. When *clk=1* the upper TG is ON and lower TG if OFF the output *pulse=0*. When the *clk* transit from 1→0 suddenly the *pulse=1*. That is the output of the invertor I3 is '1' after three inverter delay. Similarly, When *clk=0* the lower TG is responsible to produce the *pulse* at negative edge of the clock.

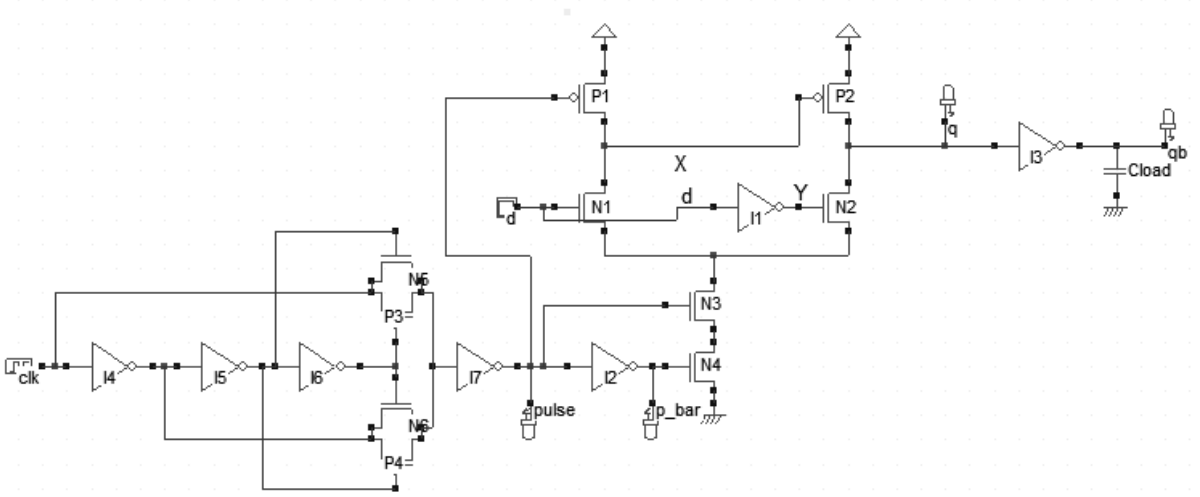


Figure 6. Schematic of DET-DDCPSFF

The pulse generator is interfacing with the DDCPSFF flip flop we get the second proposed flip flop called *double edge triggered direct data clocked pair shared flip flop (DET-DDCPSFF)* as shown in figure 6. The pulse generator circuit is the external circuit it may drive one or more flip flop. Whenever the pulse is high the *q* output follows the *d* input. The pulse is applied to the input of the inverter I2 instead of clock. The working principle is same as the DDCPSFF.

4.3 Double Edge Triggered 5TTSPC Flip flop

This is the third proposed flip flop. The same double edge triggering [8] scheme is applied to the flip flop discussed in the Section 3.2. Then named as, *double edge triggered five transistor true single phase clocked flip flop (DET-5TTSPC Flip Flop)* the schematic as shown in figure 7. We can make the 5T-TSPC flip flop to operate in both the edge of the clock. The node *X* and *Y* act as a capacitor. When *pulse=1* (N1 is ON) and *d=0* (P1 is ON and N2 is OFF) the node *Y* is charged to V_{dd} through P1 and N1 which is ON, *q=0* in *pre-charge phase*.

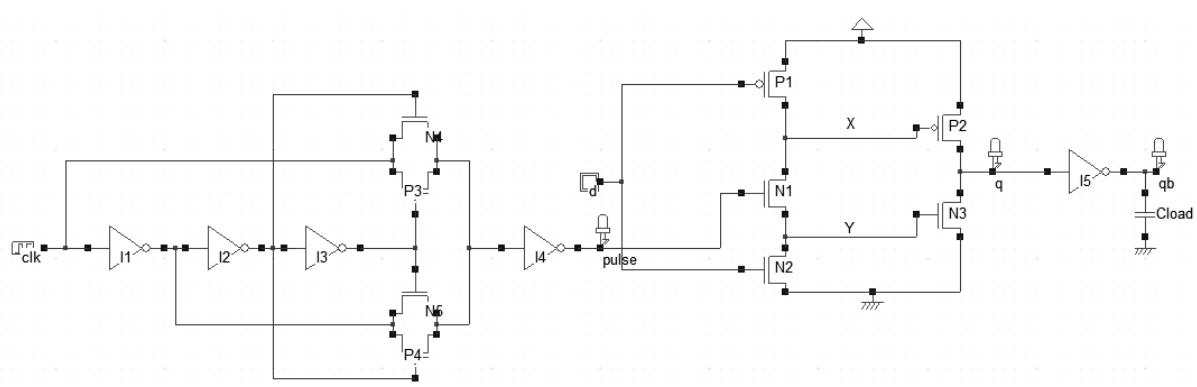


Figure 7. Schematic of DET-5TTSPC Flip Flop

When *pulse=d=1(N1* and *N2 is ON),* the node *X* is discharged to *GND* (P1 is OFF and P2 is ON), then *q=1* in *evaluation phase*. This flip flop also a less power consumption than the other double edge triggering flip flop.

4.4 SVL-5TTSPC Flip Flop

In section 3.2 we discussed about the drawback of 5T-TSPCFF like high leakage power in lower technology due to high leakage current.

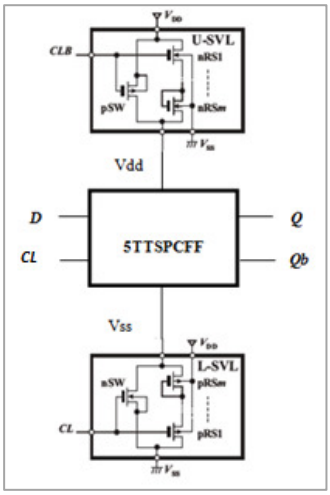


Figure 8. Block diagram of SVL-5TTSPCFF

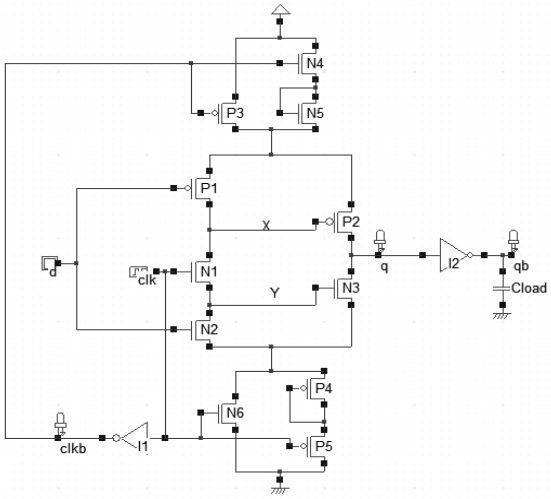


Figure 9. Schematic of SVL-5TTSPC Flip Flop

In order to avoid that we can incorporate the leakage reduction circuit called "Self-Controllable Voltage Level Circuit"[11] to this flip flop to reduce the power consumption. The block diagram of SVL-5TTSPC flip flop is shown in figure 8. The two circuits called upper SVL (U-SVL) and Lower SVL (L-SVL) is used to construct the above fourth proposed flip flop. Upper SVL consists of one PMOS (pSW) act as a switch and multiple NMOS (nRSm) act as resistors connected in series. Similarly, Lower SVL constructed by one NMOS (nSW) and multiple PMOS (pRSm) in series.

4.4.1. Working Principle of SVL-5TTSPCFF

When 5TTSPCFF is active mode i.e. *clk=1* and *clkb=0,* P3 and N6 is ON but N4 and P5 is OFF. Therefore the Upper and Lower SVL blocks can supply a maximum supply voltage V_{dd} and a minimum *ground* level V_{ss} respectively to the 5TTSPCFF, and then the operating speed of the flip flop is increased. The circuit diagram of SVL-5TTSPC flip flop as shown in figure 9.
While the 5TTSPCFF is stand-by mode i.e *clk=0* and *clkb=1,* P3 and N6 is OFF but N4 and P5 is ON. Upper SVL circuit generate lower supply *Vdd (=Vdd-Vn<Vdd) to* a flip flop and Lower SVL

circuit gives higher ground level voltage *Vss (=Vp>0).* Where *Vn* and *Vp* is the total voltage drop of N4, N5 and P4, P5 respectively. In this mode the back-gate bias (V_{BGS}) of the P3 and N6 are increased. Then V_{ts} of P3 and N6 also increases. Thus, the leakage current and power is decreases. Finally the total power consumption of flip flop is reduced.

V. LOW POWER FLIP FLOP APPLICATIONS

Portable multimedia and communication devices have experienced explosive growth recently. Longer battery life is one of the crucial factors in the widespread success of these products. As such, low-power circuit design for low power application has become very important [15]. The above low power proposed flip flops are useful in the area of *multimedia* and *wireless* communication applications and also applicable in counters, shift register, Error detector and phase detector.

5.1 Delay Buffer

As demand for the application in multimedia networks is increasing rapidly, it is important to provide multimedia services in mobile environment (ME). Obtaining to multimedia services which satisfy *synchronization* constraints in ME and improving the delay time and Quality of Services (QoS) between media streams. A *streaming* application, which is delivered to many users, magnifies the traffics. For avoiding such traffics we need *synchronization* [16].

Delay buffer play a vital role in the area of interactive and non-interactive application like, IP telephony, interactive voice/video, videoconferencing, Video-on-demand (VOD), streaming audio/video, Virtual reality etc. The level of *delay* requirement determined by degree of interactivity. For example the interactive voice applications will require strict delay and video application requires less delay. The relaxed *delay* requirements for streaming applications are in the order of seconds. *Delay* requirements are important in the satellite communication to *synchronize* the data pocket from earth station to satellite and vice-versa. Existing delay buffer is Ring Counter with Clock gated by C-element. The delay element used is double edge trigger flip flop as shown in figure 10. [15].

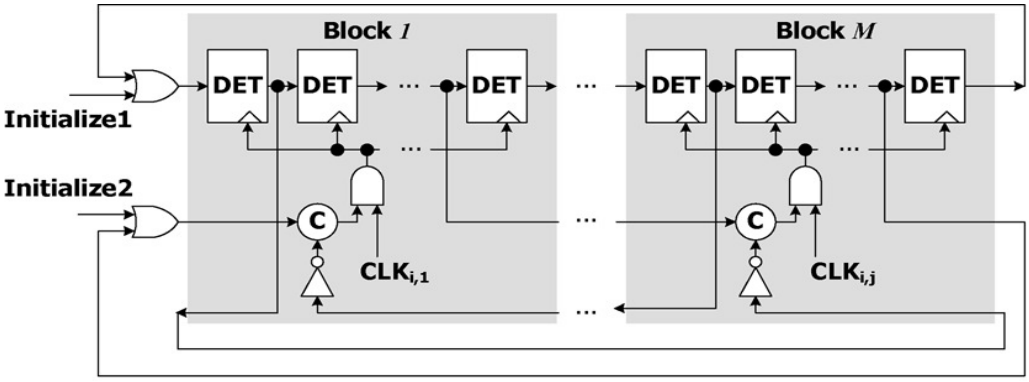


Figure 10. Ring counter with clock gated by C-elements

In the above figure the number delay block depends upon the delay requirement. The C-element in each block is used to control the delivery of clock signal to the flip flops which act as a handshaking element. The logic diagram of C-element is below figure 11. [15]. the logic of C-element is given by,

$$C^{+} = AB + AC + BC \qquad (2)$$

Where *A* and *B* is the two inputs, *C* and C^{+} is the present and next outputs. If $A=B$ the next output $C^{+}=A$. If $A \neq B$ the output unchanged.

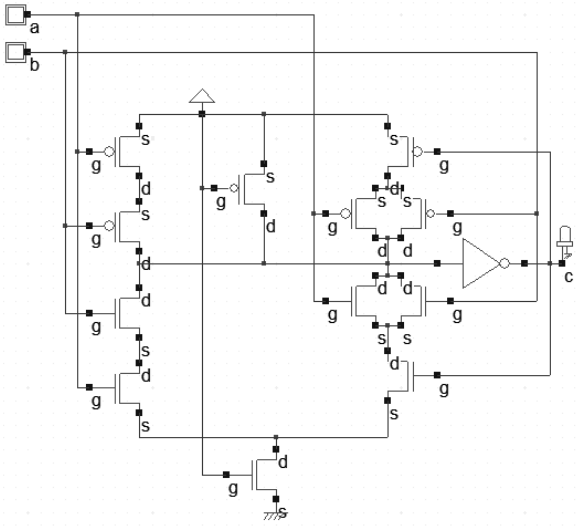


Figure 11. Logic Circuit of C-element

The clock gating technique by C-element will avoid the glitches. The proposed delay buffer will use low power DDCPSFF to reduce the total power consumption than existing delay buffer.

5.1.1. Proposed Delay Buffer

In this proposed delay buffer the Double edge trigger flip flop in figure 10. is replaced by low power DDCPSFF. Because the Double edge trigger flip flop used in existing delay buffer consist of 22 transistors including 8 clocked transistors. But DDCPSFF contain 12 transistors including 4 clocked transistors only.

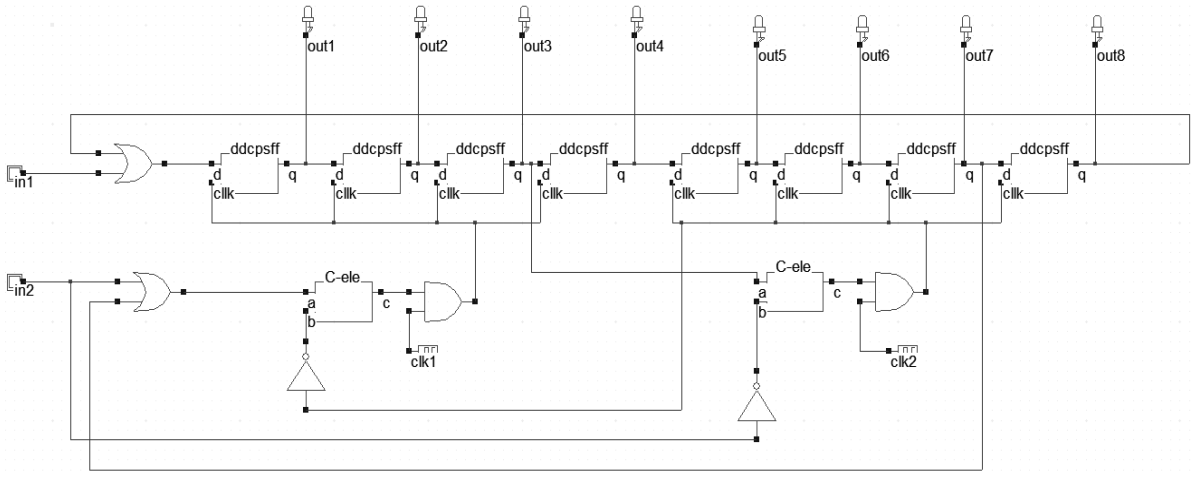


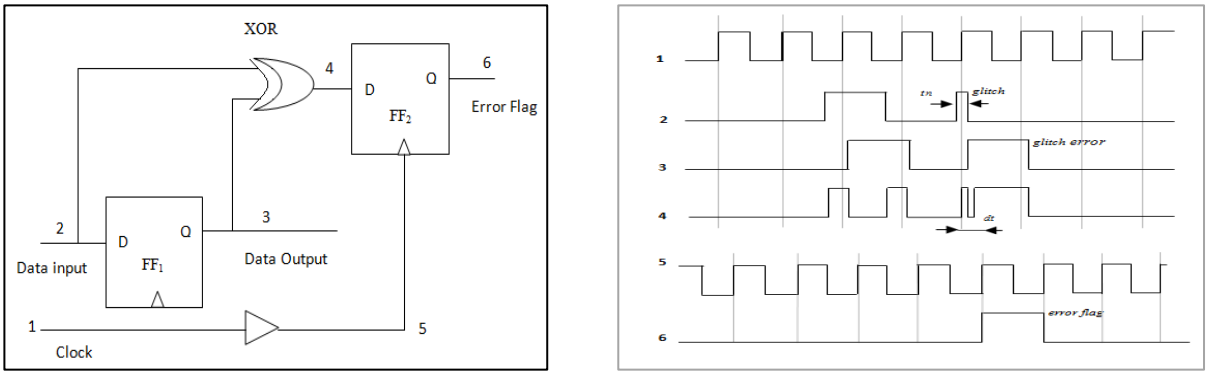
Figure 12. Proposed Delay Buffer with DDCPSFF delay Element

The working mechanism of above delay buffer is, consider the first 4 DDCPSFF is first block and second 4 DDCPSFF is second block. When the input of last flip flop in first block is "1", both input of C-element in second block will be same and the output of C-element is high. Clock signal is enabled for second block, at the same time both input of C-element in first block will go to "0", and then clock is disabled to first block. Then bit is buffered to second block. If we require more delay we can add more blocks further.

5.2 Error Detector

Integrated circuit operating frequency and density increases due to deep submicron technology. Single chip containing many complex functional blocks with interconnects and buses. As complexity of

circuit increases noise effect also increases like capacitive or inductive cross talk, transmission line effect etc. One of the common approaches to reduce the noise hazard is to bound the noise.
Some deterministic method like BIST will generate the test pattern and detect the faults due to noise. Another approach is to detect the noise is on-line testing method. It will test the functional block during operation time. It has many advantages over deterministic methods. This method is highly reliable, increased system performance and high degree of noise tolerance. Double Sampling Data Checking Technique is the one of the on-line testing method [16].



(a) (b)

Figure 13. Error detector (a) Block Diagram (b) Timing Diagram

The principle behind this method is input data is sampled by two flip flops at a time interval dt and consistency is checked from the two latched data's with each other. Consider the noise interval tn is less than dt . One of the flip flop will catches the error and sends the error signal, and then rest of the clock cycle will indicate error (i.e difference) is occurred by comparing the two flip flops. The block diagram of error detector and its timing diagram is illustrated in figure 13. [16]. in wave form no.2 the first two transitions, from $0 \rightarrow 1$ and $1 \rightarrow 0$ there is no error flag is set in the wave no.6, due to valid transition. After some time the first flip flop acquire the glitch at interval t_n . The output of first flop is glitch error output in the wave no.3. To detect the error properly, the buffer time of on-line error detector should be set suitably. dt must be longer than the noise active region so that the second flip flop FF_1 can catch the difference between outputs of FF_1 and FF_2 correctly. The dt must satisfy the following constraint [16].

$$\max(t_{DFF}, t_n)t_{xor} + t_{setup} < dt < t_{pd} + t_{xor} + t_{setup} - t_{ske} \quad (3)$$

Where t_{DFF} and t_{xor} are the FF_1 and the XOR propagation time respectively. t_n is the noise active duration. t_{setup} and t_{ske} is the FF_2 set up time and worst case clock skew respectively. t_{pd} is the incoming signal minimal path delay.

5.2.1. Proposed Low power Error Detector

In this proposed error detector, the conventional D-flip flop is replaced by low power SVL-5TTSPC flip flop discuss in section 3.4.1.

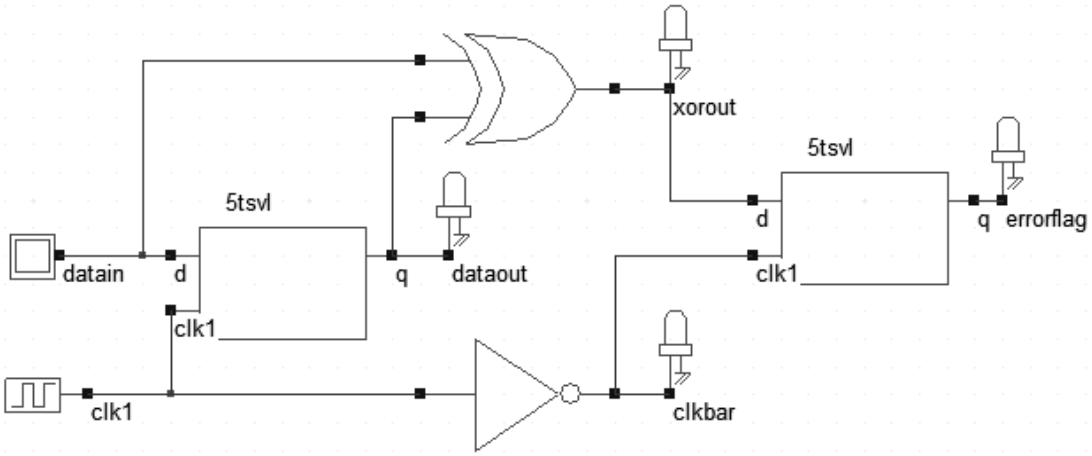


Figure 14. Proposed Low Power Error Detector

Working principle of detector is same as the existing one. The difference between existing and proposed error detector is later will consume less power than existing one. The simulation results of proposed delay buffer and error detector will discussed in next section.

VI. SIMULATION RESULTS

6.1 Proposed Flip Flops

The simulation results were obtained from MICROWIND2.0 in 90nm CMOS process at room temperature VDD is 1V. All existing and proposed flip flops were simulated with output load capacitance C_{load} and layout level. The clock frequency for single triggering and double edge triggering flip flop is 1GHz and 0.5GHz respectively. Following six flip flop metrics are carried out to compare the performance of the existing and proposed flip flops.

***Total no of Transistors*:** The total number of transistors is measured which contribute more area and power consumption in the integrated circuit design.

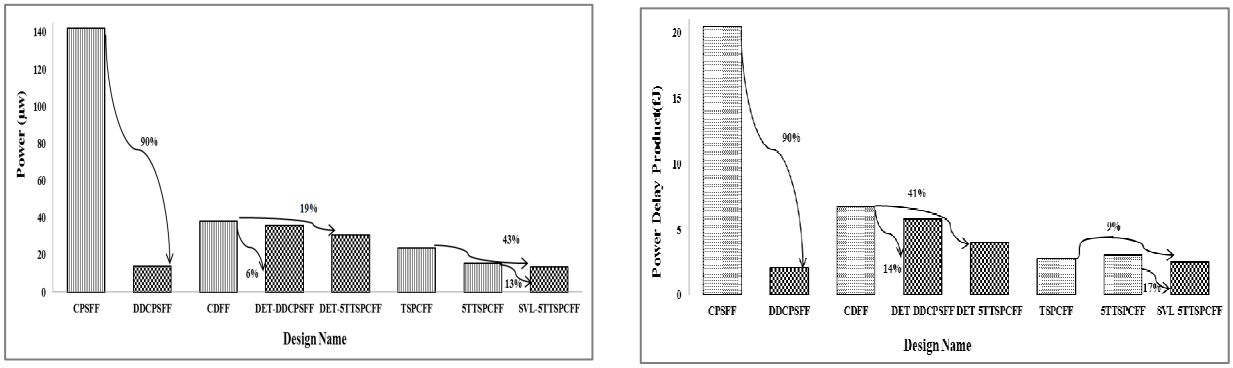
Number of clocked Transistor: Clocked transistors will contribute more power consumption due to high switching activity.

Delay: Delay is data to output delay (D-to-Q delay) which is sum of the *Set up time* and *clock to output (Q) delay*. Set up time is minimum time needed between the D input signal change and the triggering clock signal edge on the clock input. This metric guarantees that the output will follow the input in worst case conditions of process, voltage and temperature (PVT). This assumes that the clock triggering edge and pulse has enough time to capture the data input change. Clock-to-Q delay is the propagation delay from the clock terminal to the output Q terminal. This is assuming that the data input D is set early enough with respect to the effective edge of the clock input signal. The D-to-Q delay is obtained by sweeping the 0→1 and 1→0 data transition times with respect to the clock edge and the minimum data-to-output delay corresponding to optimum set up time is recorded. The output is considered as Qb. Since, the load capacitor is connected to Qb output. The unit is *ps (Pico second).*

Power: It is the total power consumption of flip flop in terms of *μw (micro watt).*

Power Delay Product (PDP): To quantify how effective or efficient a digital design technology is in terms of delay and power; Product of the delay and the power dissipation in terms of fJ *(femto joule).*

Area: It is nothing but total layout area of the flip flop in mm^2 *(mille meter square).*



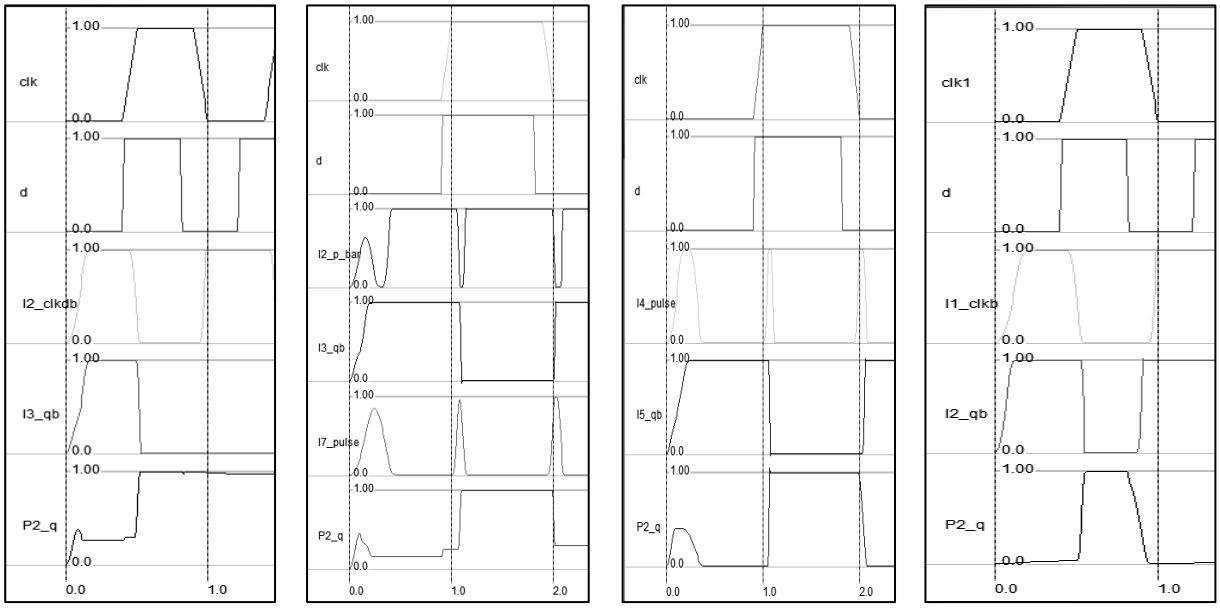
(a) (b)

Figure 15. Comparison chart (a) Design Vs Power (b) Design Vs PDP

Table 1. Comparison of Flip Flop Metrics

Design Name	No.of Flip Flops[a]	No.of Clocked Flip Flops	Delay(ps)[b]	Power(µw)	PDP(fJ)	Area(mm^2)
CPSFF	19	4	144	142.000	20.448	161
DDCPSFF	12	4	149	13.883	2.068	160
CDFF	28	2	177	38.055	6.735	340
DET-DDCPSFF	24	2	161	35.785	5.761	290
DET-5TTSPCFF	19	2	130	30.683	3.988	260
TSPCFF	11	4	116	23.816	2.760	230
5TTSPCFF	7	1	194	15.607	3.027	117
SVL-5TTSPCFF	15	5	184	13.657	2.512	160

[a] Including Clocked Transistor
[b] Delay uses DQb



(a) (b) (c) (d)

Figure 16. Simulated waveforms (a) DDCPSFF (b) DET-DDCPSFF (c) DET-5TTSPCFF (d) SVL-5TTSPCFF

Table 1 shows the flip flop metrics comparison in terms of delay, power, PDP and area. The single edge triggered DDCPSFF achieved 90% of power reduction than CPSFF. Double edge triggered flip flops DET-DDCPSFF and DET-5TTSPCFF achieved 6% and 19% power reduction than CDFF

respectively. The SVL-5TTSPCFF is 13% and 43% reduced power consumption than 5TTSPCFF and TSPCFF correspondingly. Simulated waveforms for four proposed flip flops as shown in figure 16. The area reduction achieved about 1% ~ 30% and PDP improvement about 9% ~ 90%.

6.2 Proposed Delay Buffer and Error Detector

Existing and proposed delay buffers were simulated in 90 nm technology for different supply voltages. The clock frequency is 50 MHz. Similarly, the error detector was simulated at the same environment for 1V. From Table 2, the Proposed delay buffer improves the overall power consumption from 89.8% ~ 92.7% than existing delay buffer with conventional DFF.

Table 2. Comparison Table for Delay Buffer

Design	Power(µw)				Area(mm^2)	Total No.of Transistor
	1V	1.5V	2V	2.5V		
Existing delay buffer	745	846	947	1045	2054	194
Proposed delay buffer	75.97	76	76.05	76.1	1456	114
Improvement	89.8%	91%	91.9%	92.7%	29%	41%

The projected delay buffer achieved 29% and 41% of area and total number of transistors reduction than existing one. If supply voltage is increases power consumption is also increased. Because the total power consumption is directly proposonal to supply voltage. The simulated waveform of proposed delay buffer is as shown in figure 17.

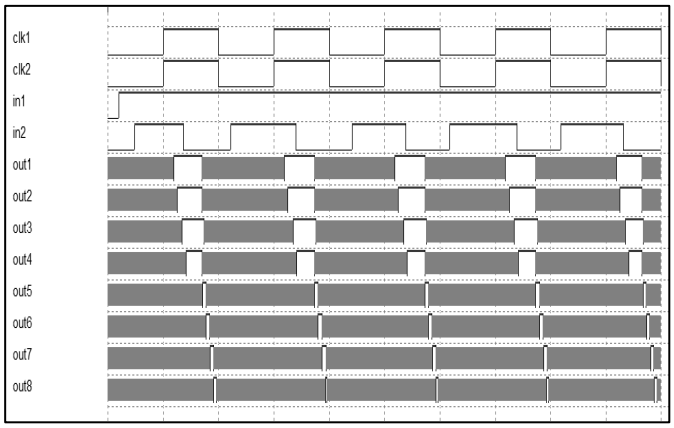


Figure 17. Simulated waveform of Proposed Delay Buffer

Table 3 shows the comparison of error detector in terms of power and area. Proposed error detector improves the power and area reduction about 25% and 15% respectively.

Table 3. Comparison Table for Error Detector

Design	Power(µw)	Area(mm^2)
Existing Error detector	131.48	427
Proposed Error detector	98.73	363
Improvement	25%	15%

Figure 18. shows the simulated waveform of proposed error detector.

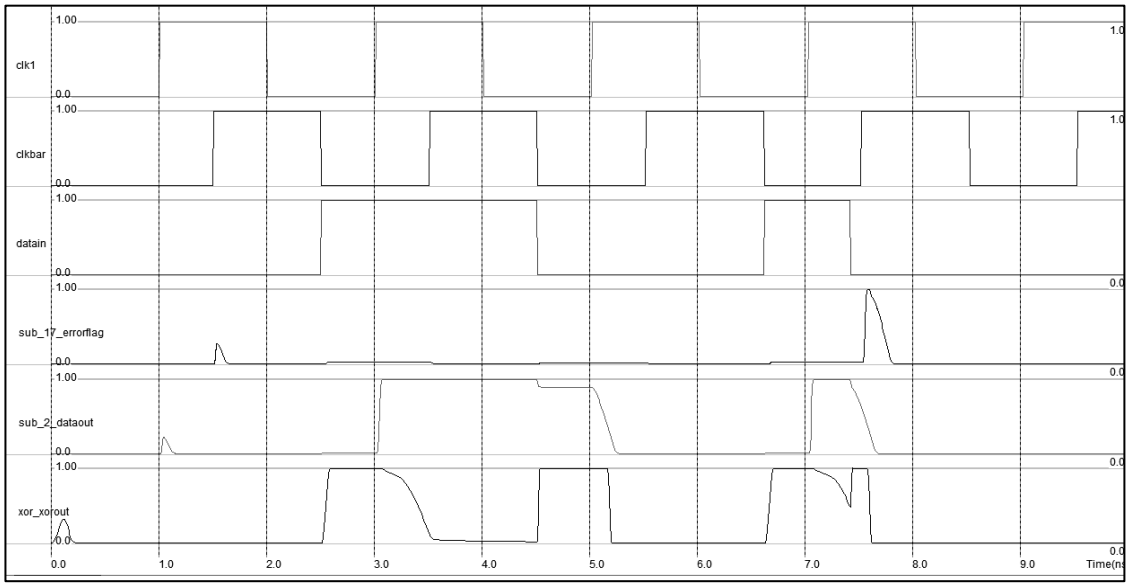


Figure 18. Simulated waveform of proposed error detector

VII. CONCLUSIONS

In this paper the proposed direct data clocked pair shared flip flop employed a new approach called removal of noise coupling transistor to reduce the power consumption called DDCPSFF. Some other existing low power techniques are implemented in new flip flop like double edge triggering and self-controllable voltage level circuit for further power reduction, then other three new flip flops will be DET-DDCPSFF, DET-5TTSPCFF and SVL-5TTSPCFF. The new flip flops give 6% ~ 90% power reductions than existing one. The DDCPSFF and SVL-5TTSPCFF flip flops are used as a delay buffer and error detector in the area of multimedia and wireless communication applications. The proposed delay buffer and error detector gives overall power reduction improvement from 89.8% ~ 92.7% and 25% than existing. DDCPSFF gives 55% improvement, DET-5TTSPCFF and SVL-5TTSPCFF will give 1.3% ~ 56% improvements in power reduction than Proposed Pulsed flip flop in the recent paper [17].

VIII. FUTURE WORK

Furthermore we can reduce the power consumption by using low swing voltage approach. If supply voltage is halved the switching activity of the transistor will be reduced leads power reduction. Then transistor scaling or layout optimization is another way to reduce power consumption.

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