DESIGN OF LOW POWER LOW NOISE BIQUAD GIC NOTCH FILTER IN 0.18 μM CMOS TECHNOLOGY

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ABSTRACT

In design of analog circuits not only the gain and speed are important but power dissipation, supply voltage, linearity, noise and maximum voltage swing are also important. In this paper a biquad GIC notch filter is design which provides low power. In this research, the design and VLSI implementation of active analog filter, based on the Generalized Impedance Converter (GIC) circuit, are presented [1]. The circuit is then modeled and simulated using the Cadence Design Tools software package. Active filters are implemented using a combination of passive and active (amplifying) components, and require an outside power source. Operational amplifiers are frequently used in active filter designs. These can have high Q factor, and can achieve resonance without the use of inductors. This paper presents a new biquad GIC notch filter topology for image rejection in heterodyne receivers and Front End receiver applications. The circuit contains two op-amp, resistor, capacitor topology for testing purposes. It is implemented with standard CMOS 0.18μm technology. The circuit consumes 0.54 mW of power with a open loop gain 0dB, 1 dB compression point the linear gain obtained +7.5dBm at 1.1 kHz and 105 degree phase response from a 1.8V power supply optimum [2].

KEYWORDS: *Opamp, GIC, Notch filter, low power.*

I. INTRODUCTION

In concern of power, a low power design has made a revolutionary change in our life style. And still people are fighting for low power and better performance.
The design of analog circuits itself has evolved together with the technology and the performance requirements. As the device dimension shrink, the supply voltage of integrated circuit drops, and the analog and digital circuit are fabricated on one chip, many design issues arise that were unimportant only few decade ago. In design of analog circuits not only the gain and speed are important but also power dissipation, supply voltage, linearity, noise and maximum voltage swing.
Active filters are implemented using a combination of passive and active (amplifying) components, and require an outside power source. Operational amplifiers are frequently used in active filter designs. A filter is an electrical network that alters the amplitude and/or phase characteristics of a signal with respect to frequency. Ideally, a filter will not add new frequencies to the input signal, nor will it change the component frequencies of that signal, but it will change the relative amplitudes of the various frequency components and/or their phase relationships.
In circuit theory, a filter is an electrical network that alters the amplitude and/or phase characteristics of a signal with respect to frequency. Ideally, a filter will not add new frequencies to the input signal, nor will it change the component frequencies of that signal, but it will change the relative amplitudes of the various frequency components and/or their phase relationships. Filters are often used in electronic systems to emphasize signals in certain frequency ranges and reject signals in other frequency ranges. Such a filter has a gain which is dependent on signal frequency.

II. THE GIC TOPOLOGY

The integrated circuit manufacturing of resistors and inductors is wrought with difficulty, exhibits poor tolerances, is prohibitively expensive, and is, as a result, not suitable for large scale

implementation. The use of active components, the General Impedance Converter (GIC) design will allow for the elimination of resistors and inductors by simulating their respective impedances.

The generalized impedance converter (GIC) is highly insensitive to component variation. The GIC filter design was introduced by Mikhail and Bhattacharya and proved to be very insensitive to non–ideal component characteristics and variations in component values. Figure 10 shows the general topology of the GIC filter. GIC biquads are two op–amps with good high frequency performance. All but the even notch stages are tuneable. The high pass, low pass and band pass stages are gain adjustable. The notch and all pass stages have a fixed gain of unity. All GIC stages have equal capacitor values, unless a capacitor is required to adjust the gain. Notch stages do not rely on element value subtractions for notch quality and are thus immune from degradations in notch quality due to element value error [3].

Analog circuits such as audio and radio amplifiers have been in use since the early days of electronics. Analog systems carry the signals in the form of physical variables such as voltages, currents, or charges, which are continuous functions of time. The manipulation of these variables must often be carried out with high accuracy. On the other hand, in digital systems the link of the variables with the physical world is indirect, since each signal is represented by a sequence of numbers. Clearly, the types of electrical performance that must be achieved by analog and digital electronic circuits are quite different. Nowadays, analog circuits continue to be used for direct signal processing in some very-high-frequency or specialized applications, but their main use is in interfacing computers to the analog world. The development of the very-large-scale-integration (VLSI) technology has led to computers being pervasive in telecommunications, consumer electronics, biomedicine, robotics, the automotive industry, etc. As a consequence, the analog circuits needed around them are also pervasive. Interfacing computers or digital signal processors to the analog world requires various analog functions, among them amplification, filtering, sampling, (de)multiplexing, and analog-to-digital (A/D) and digital-to-analog (D/A) conversions. Since analog circuits are needed together with digital ones in almost any complex chip and the technology for VLSI is the complementary metal–oxide–circuits. Semiconductors (CMOS), most of the current analog circuits are CMOS.[4]

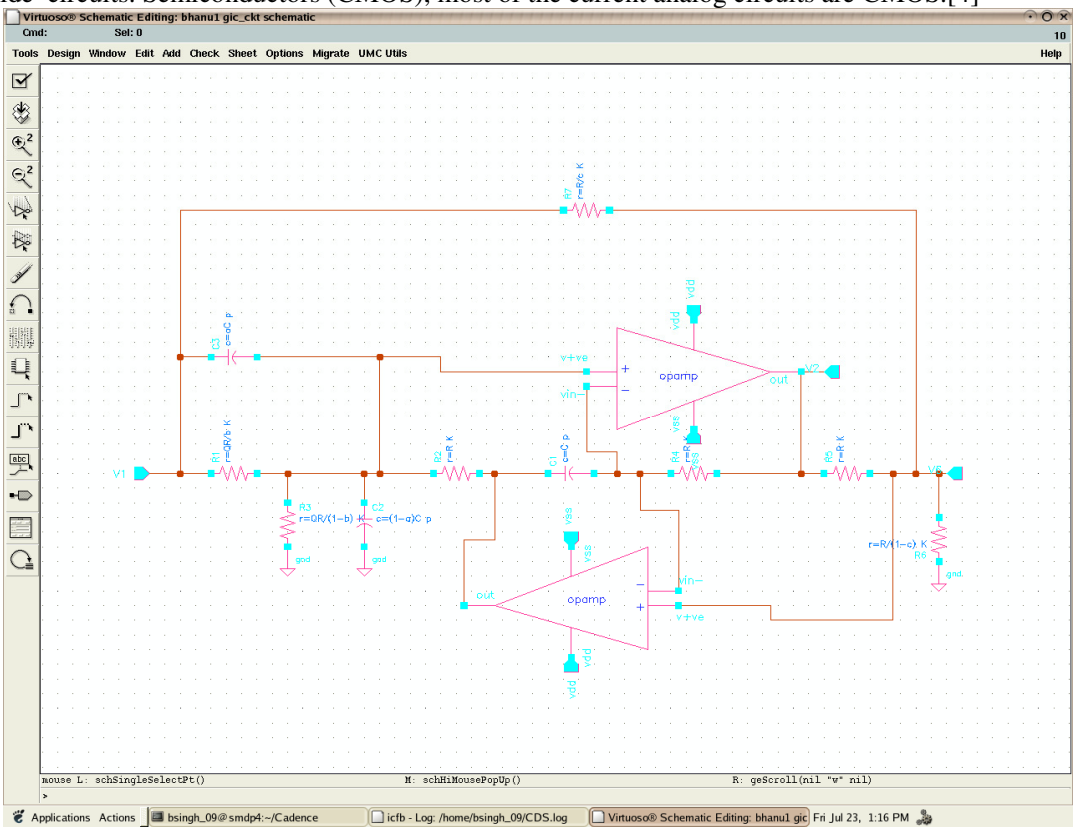

Figure 1.Generalized Biquad GIC Schematic

It has been shown that in order to implement all possible filter types using passive components a circuit network must contain resistors, capacitors, and inductors. Modern IC manufacturing techniques allow for the accurate construction of capacitors, and a method for the elimination of resistors by using switched capacitors. However, we are still left with the problem of inductors. Discrete inductors of suitable impedance values are available for use in circuits. Discrete inductors of suitable impedance values are available for use in circuits. However, these inductors tend to be large and costly. Additionally, the focus of modern electronics on fully integrated circuits. Integrated circuit manufacture of suitable inductors is very difficult, if not possible.

IC inductors take up vast quantities of valuable chip area, and suffer from terrible tolerances. How then can we develop the full range of filter types in light of the problems involving inductors? It was recognized in the 1950s that size and cost reductions, along with performance increases, could be achieved by replacing the large costly inductors used in circuits with active networks. This is not to say that the need for inductive impedance was obviated. Rather a suitable replacement, or means simulation was necessary. A variety of methods for the simulation of inductances have been developed. One of the most important and useful of these methods is the Generalized Impedance Converter (GIC) developed by Antoniouetal.

III. DESIGN OF TWO STAGE DIFFERENTIAL OPERATIONAL AMPLIFIER

The most commonly used configuration for CMOS operational amplifiers is the two stage amplifier. There is a differential front end which converts a differential voltage into a current and a common source output stage that converts the signal current into an output voltage. An important criterion of performance for these op amps in many applications is the settling time of the amplifier.

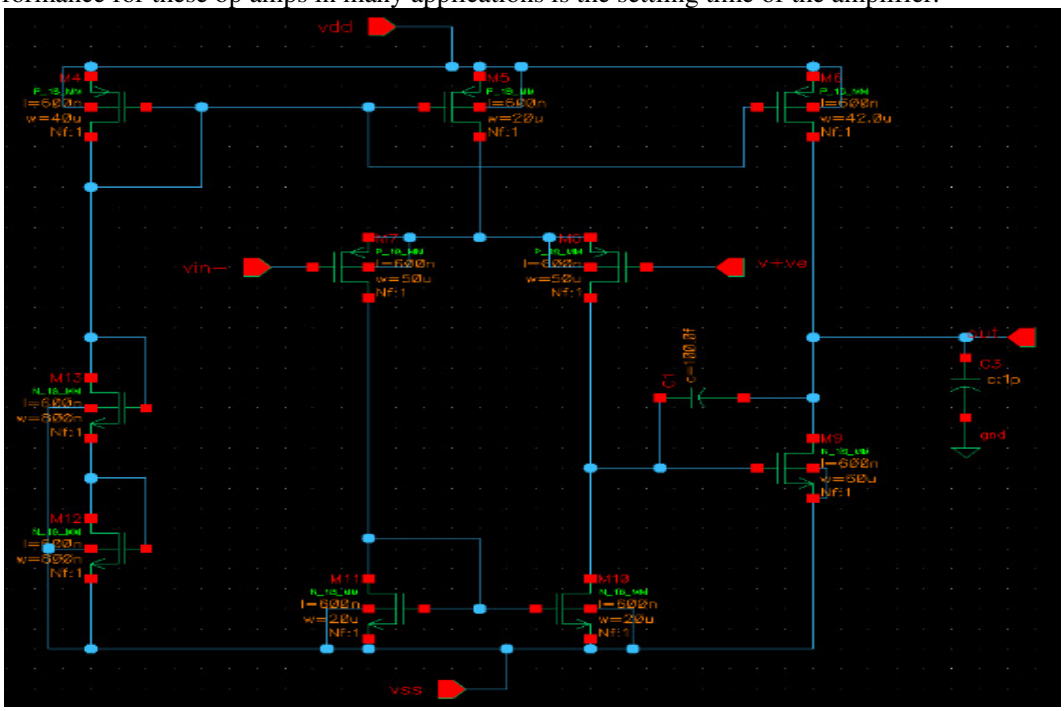

Figure 2. Schematic of two stage op-amp

In a never-ending effort to reduce power consumption and gate oxide thickness, the integrated circuit industry is constantly developing smaller power supplies. Today's analog circuit designer is faced with the challenges of making analog circuit blocks with sub 1V supplies with little or no reduction in performance. Furthermore, in an effort to reduce costs and integrate analog and digital circuits onto a single chip, the analog designer must often face the above challenges using plain CMOS processes. A schematic diagram of the two stage op-amp with output buffer is shown in figure 2. The First stage is a Differential-input, single-ended output stage. The second stage is a common-source gain stage that

has an active load. Capacitor Cc is included to ensure stability when op-amp is used with feedback. It is Miller capacitance. The third stage is a common drain buffer stage. If the op-amp is intended to drive a small purely capacitive load. An operational amplifier, often referred to as an 'op-amp', is a DC-coupled electronic differential voltage amplifier, usually of very high gain, with one inverting and one non-inverting input.

Design of op-Amp: operational amplifier is very important to get accurate result. The Op-Amp is characterized by various parameters like open loop gain, Bandwidth, Slew Rate, Noise and etc. The performance measures are fixed due to design parameters such as transistors size, bias current and etc. This op-amp is designed using UMC 0.18 µm technology with a supply voltage of 1.8 V. The value of the load capacitance is taken as 1pF. The main constraints in the design are the requirement of low power consumption. The open Loop Gain obtained 70.49dB, which confirm the design parameters we took at the starting of the design. Open loop gain should be greater than 70dB (figure.5).

IV. EQUATION

The first goal will be to develop the transfer function of the circuit in terms of the generic admittance values. Then we can substitute in values for the admittances in order to realize the various filter types.

$$T(s) = V2/V1 = \frac{s^2 (2a - c) + s (\omega_0/Q) (2b - c) + c\omega_0^2}{S^2 + s\omega_0/Q + \omega_0^2}$$

We observe that above equation can realize an arbitrary transfer function with zeros anywhere the s-plane.

V. DESIGN OF ACTIVE BIQUAD GIC NOTCH FILTER

Design the notch filter with the GIC biquad of figure. To be eliminated is the frequency component at f_0 = 1 kHz from a signal. The low and high frequency gains must be 0 dB and the attenuation must not be larger than 1 dB in a band of width 100 Hz around f_0. The transfer function of this filter is

$$T(s) = \frac{s^2 + \omega_0^2}{s^2 + s\,\omega_0/Q}$$

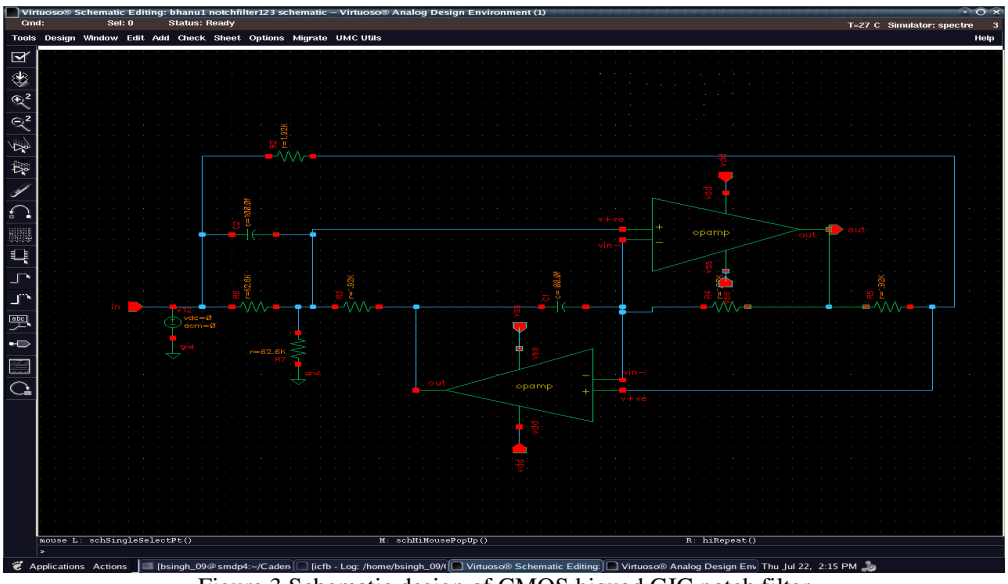

Figure 3.Schematic design of CMOS biquad GIC notch filter

To design schematic of notch filter, we have chose C = 0.1μF, R = $1/(\omega_0 C)$ = 1.918 kΩ, and

Q = 16.3.

It is the schematic of CMOS biquad GIC notch filter using the AM biquad topology. The design of this CMOS biquad GIC notch filter is done using Cadence Tool. The Simulation results are found using Cadence Spectre environment with UMC 0.18 μm CMOS technology.

VI. SIMULATION RESULT OF ACTIVE NOTCH FILTER AND OP-AMPLIFIER

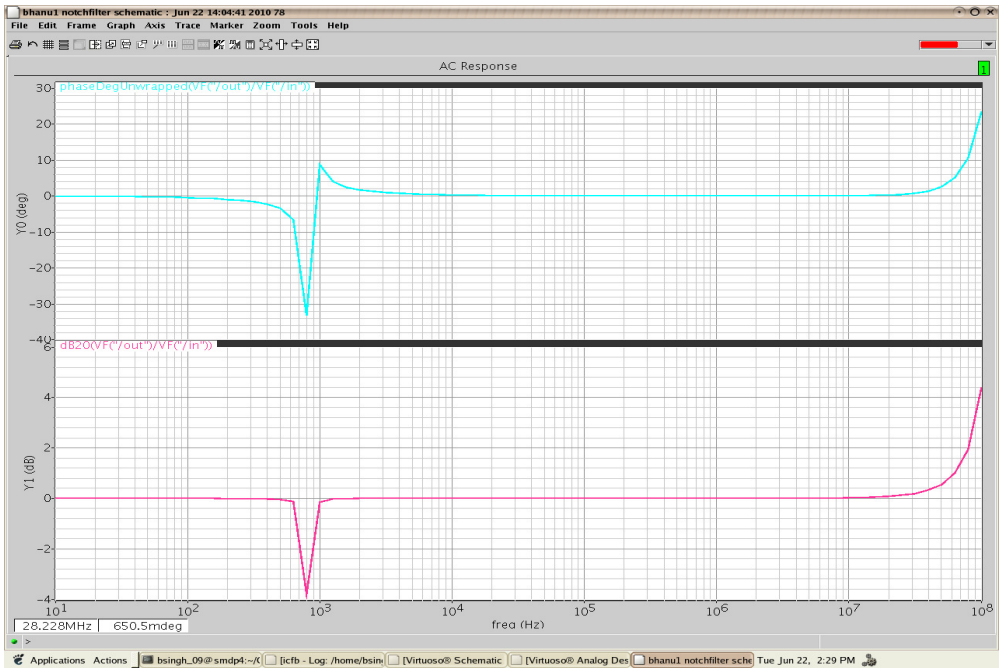

Figure 4.Simulation result of Gain and Phase response

The open Loop Gain obtained 0dB which confirm to the design parameters we took at the starting of the design. This simulation result shows the phase response of the given filter, its gives 105 degree. Its value obtains by adjusting the value of capacitances.

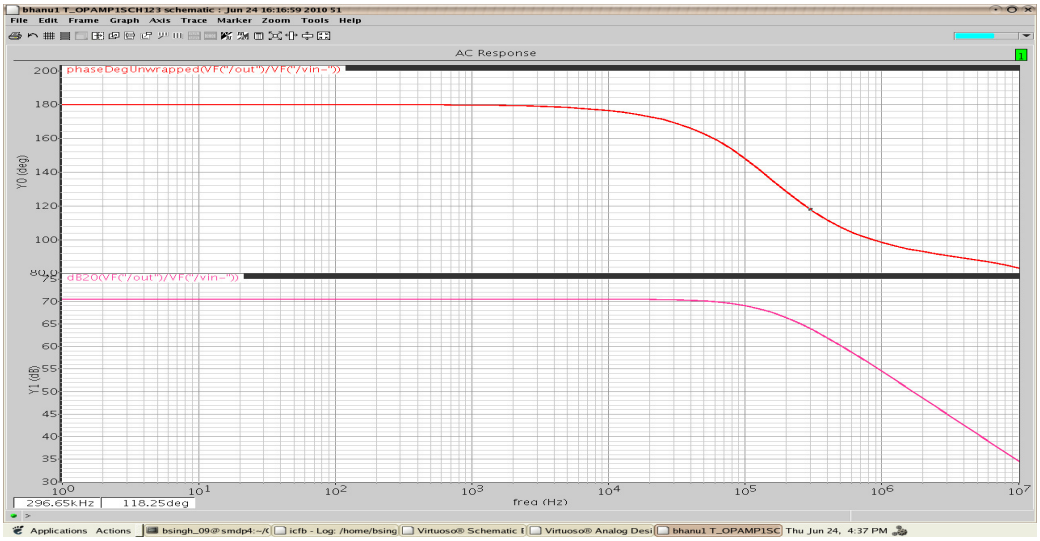

Figure 5. Gain and phase response of CMOS Op-amp

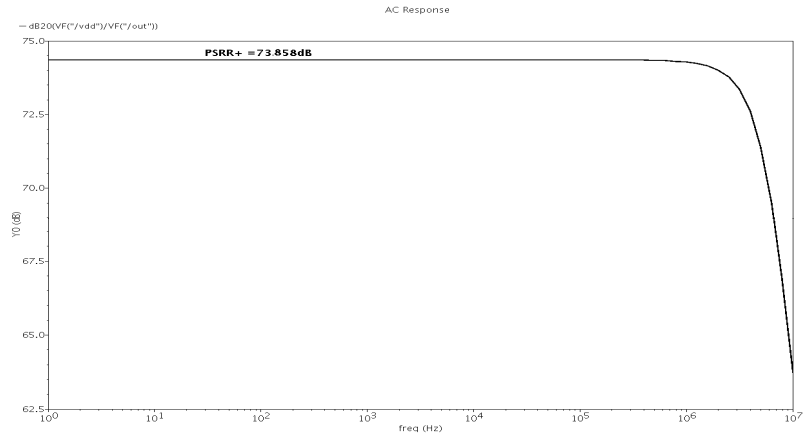

Figure 6.Simulation result of PSRR+ response(notch filter)

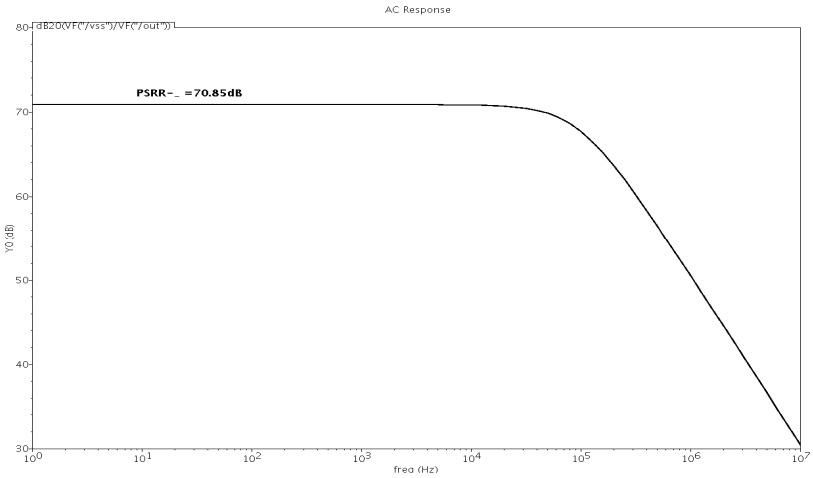

Figure 7. Simulation result of PSRR- response (notch filter)

Above figure shows the simulation result of power supply rejection ratio (PSRR).In this method we apply common mode dc potential to the input transistors and ±1.8V AC signal is inserted between Vdd supply and Vdd port of the circuit. The power supply rejection ratios are obtained as 74 dB and 70 dB with PSRR+ and PSRR- respectively.

VII. CONCLUSION

In this design, a low-voltage CMOS biquad GIC notch filter is designed using a Generalized Impedance Converter topology. The proposed techniques can be used to design low-voltage and low-power biquad GIC notch filter in a standard CMOS process. To demonstrate the proposed techniques, a ±1.8V, second-order filter implemented in a standard 0.18µm CMOS process. In this designing mainly work on low power, linearity and phase response. The Active- RC biquadratic cell exploits the frequency response of the op-amp to synthesize a complex poles pair, reducing the unity gain bandwidth requirements of the op-amp in the closed loop topologies. A proper bias circuit is used to fix the operating point of the biquad. The third design exploits the source follower principle. Very low current consumption (0.54mW) is performed at ±1.8 supply voltage in the 1 KHz cut-off frequency.

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