DEEP SUB-MICRON SRAM DESIGN FOR DRV ANALYSIS AND LOW LEAKAGE

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ABSTRACT

This paper deals with the design opportunities of Static Random Access Memory (SRAM) for lower power consumption and propagation delay. Initially the existing SRAM architectures are investigated, and thereafter a suitable basic 6T SRAM structure is chosen. The key to low power dissipation in the SRAM data path is to reduce the signal swings on the highly capacitive nodes like the bit and data lines. While designing the SRAM, techniques such as circuit partitioning, divide word line and low power layout methodologies are reviewed to minimize the power dissipation.

KEYWORDS: *SRAM,SNM, DRV,SOC,CMOS, DIBL*

I. INTRODUCTION

Ever since the early days of semiconductor electronics, there has been a desire to miniaturize the components, improve their reliability and reduce the weight of the system. All of these goals can be achieved by integrating more components on the same die to include increasingly complex electronic functions on a limited area with minimum weight. Another important factor of successful proliferation of integration is the reduced system cost and improved performance.

SRAM cell design considerations are important because of following reasons.

1. The design of an SRAM cell is key to ensure stable and robust SRAM operation.
2. The continuous drive to enhance the on-chip storage capacity; the SRAM designers are motivated to increase the packing density. Therefore, an SRAM cell must be as small as possible while meeting the stability, speed, power and yield constraints.
3. Near minimum size cell transistors exhibit higher susceptibility with respect to process variations.
4. The cell layout largely determines the SRAM critical area, which is the chip yield limiter.
5. In scaled technologies the cell stability is of paramount significance. Static Noise Margin (SNM) of a cell is a measure of its stability

A significantly large segment of modern SoCs is occupied by SRAMs. SRAM content in ASIC domain is also increasing. Therefore, understanding SRAM design and operation is crucial for enhancing various aspects of chip design and manufacturing. The memory leakage power [13] has been increasing dramatically and becomes one of the main challenges in future system-on-a-chip (SoC) design.

For mobile applications low standby power [4] [16] is crucial. A mobile device often operates in the standby mode. As a result, the standby leakage power has a large impact on the device battery life. Memory leakage suppression [18] is important for both high speed and low power SoC designs. A large variety of circuit design techniques available to reduce the leakage power of SRAM cells and the memory peripheral circuits.

In recent years, significant progress has been made in design and development of low power electronics circuits. Power dissipation has become a topic of intense research and development of portable electronic devices and systems. In VLSI chip, with higher levels of integration, packaging density of transistors is increasing. As a result, for high levels of integration power dissipation

becomes the dominant factor. CMOS technology is known for using low power at low frequency with high integration density. There are two main components that determine the power dissipation of a CMOS gate, first component is the static power dissipation [9] due to leakage current and second component is the dynamic power dissipation [10] due to switching transient current and charging/discharging of load capacitance. In order to accurately determine the heat produced in a chip, one must determine the power dissipated by the number of gates and the number of off-chip drivers and receivers.

The need for low power design [11] [10] is becoming a major issue in high performance digital systems, such as portable communication devices, microprocessors, DSP's and embedded throughput. Hence low power design of digital integrated circuits has emerged as a very active developing field. As integrated chip designers accelerate their adoption of today's deep sub micron semiconductor (DSM) technologies, squeezing the maximum transistor count into and the maximum performance, minimum power and noise out of their high performance designs, increasing importance is placed on the accuracy of cell characterization systems. The common traits of high-performance chips are the high integration density and high clock frequency. The power dissipation of the chip increases with the increasing clock frequency. In most of the real time applications, the requirements for low power consumption must be met along with the high chip density.

In this paper, a circuit level leakage technique is adapted for the core cell to minimize the leakage by having good data stability. In section II, the SRAM cell design opportunities are explained and corresponding design trade-offs are listed. The existing leakage techniques are investigated and optimal V_{DD} value is fixed with the help of SNM and DRV in section III. The simulation results are presented to compare the stability and optimal VDD are given in section IV and conclusion is given in section V.

II. SRAM DESIGN OPPORTUNITIES

Modern SRAMs strive to increase bit counts while maintaining low power consumption [6] and high performance. These objectives require continuous scaling of CMOS transistors. The supply voltage must scale down accordingly to control the power consumption and maintain the device reliability. Scaling the supply voltage and minimum transistor dimensions that are used in SRAM cells challenge the process and design engineers to achieve reliable data storage in SRAM arrays. This task is particularly difficult in large SRAM arrays that can contain millions of bits. Random fluctuations in the number and location of the doping atoms in the channel induce large threshold [5] voltage fluctuations in scaled-down transistors.

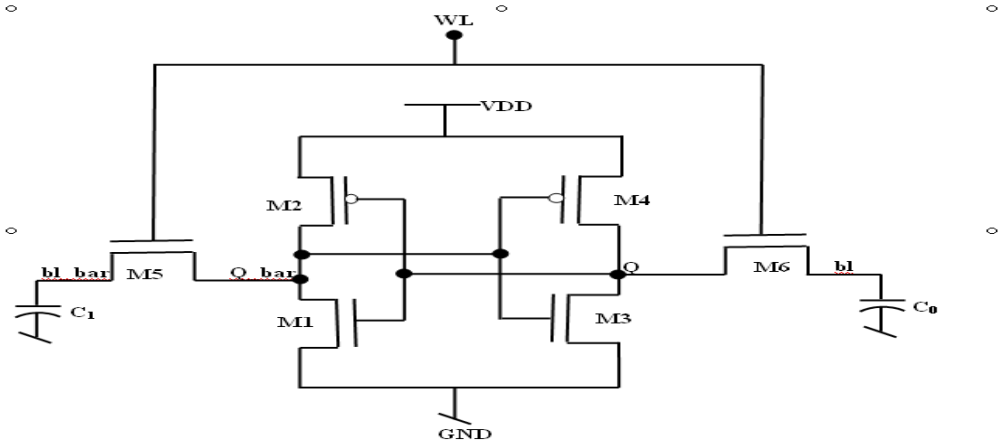

Figure 1. Schematic of SRAM cell

Other factors affecting the repeatability of the threshold voltage and introducing V_{TH} mismatches even between the neighboring transistors in SRAM cells are the line edge roughness, the variations of the poly critical dimensions and the short channel effects. SRAM stability margin or the Static Noise Margin (SNM) is projected to reduce by 4X as scaling progresses from 250 nm CMOS technology down to 50 nm technology [3]. Since the stability of SRAM cells is reducing with the technology scaling, accurate estimation of SRAM data storage stability in pre-silicon design stage and verification of SRAM stability in the post-silicon testing stage are increasingly important steps in SRAM design.

III. EXISTING AND PROPOSED WORK

A large variety of circuit design techniques used to reduce the leakage power of SRAM cells and the memory peripheral circuits (decoding circuitry, I/O, etc). The leakage of the peripheral circuits can be effectively suppressed by turning off the leakage paths with switched source impedance (SSI) during idle period. Our work focuses on the leakage control of 6T -structure SRAM core cell of Fig 1 during the standby mode. The existing SRAM cell leakage reduction techniques include novel SRAM cell design, dynamic-biasing [1], and VDD-gating. Memory operations at such a low voltage effectively reduce both the active and standby power.

The dynamic-biasing techniques use dynamic control on transistor gate-source and substrate-source bias to enhance the driving strength of active operations and create low leakage paths during standby period. At the current technology nodes (130nm and 90nm), the above dynamic-biasing schemes typically achieve 5-7X leakage power reduction. This power saving becomes less as the technology scales, because the worsening short-channel effects cause the reverse body bias effect on leakage suppression to diminish [12]. In order to design for a higher (>30X) and sustainable leakage power reduction [7], an SRAM designer needs to integrate multiple low-power design techniques, rather than using dynamic-biasing only.

The VDD-gating techniques either gate-off the supply voltage of idle memory sections, or put less frequently used sections into a low-voltage standby mode. There are three types of leakage mechanisms in an SRAM cell: sub-threshold leakage, gate leakage and junction leakage. A lower VDD reduces all of these leakages effectively. The reduction ratio in leakage power is even higher because both the supply voltage and leakage current are reduced. In recent years as the need of leakage reduction in high-utilization memory structures increases, there have been many research activities on low-voltage SRAM standby techniques.

Although the available techniques can be very effective in enhancing the efficiency of low-voltage memory standby operation, an important parameter needed by all of these schemes is the value of SRAM standby VDD. This is because a high standby VDD preserves memory data but produces high leakage current, and a very low standby VDD effectively reduces leakage power but does not guarantee a reliable data-retention [8]. An optimal standby VDD is needed to maximize the leakage power saving and satisfy the data preservation requirement at the same time. This will be the main focus of our work.

To determine the optimal standby VDD of an SRAM, it is important to understand the voltage requirement for SRAM data retention. Based on an in-depth study of SRAM low voltage data-retention behavior, this work defines the boundary condition of SRAM data retention voltage (DRV), and then derives both the theoretical and practical limits of DRV as functions of design and technology parameters. These DRV analysis and results provide insights to SRAM designers and facilitate the development of low power memory standby schemes. In addition to the analytical DRV study, developed a design technique that aggressively reduces the SRAM standby leakage.

In a typical 6T - SRAM design, the bit line voltages are connected to VDD during standby mode. This cell can be represented by a flip-flop comprised of two inverters. These inverters include access transistors M5 and M6. When VDD is reduced to DRV during standby operation, all six transistors in the SRAM cell are in the sub-threshold region. Thus, the capability of SRAM data retention strongly depends on the sub-threshold current conduction behavior.

As the minimum VDD required for data preservation, DRV of an SRAM cell is a measure of its state-retention capability under very low voltage. In order to reliably preserve data in an SRAM cell, the cross-coupled inverters must have a loop gain greater than one. The stability of an SRAM cell is also

indicated by the static-noise margin (SNM) [14] [17]. As shown in Fig 2, the SNM can be graphically represented as the largest square between the voltages transfers characteristic (VTC) curves of the internal inverters.

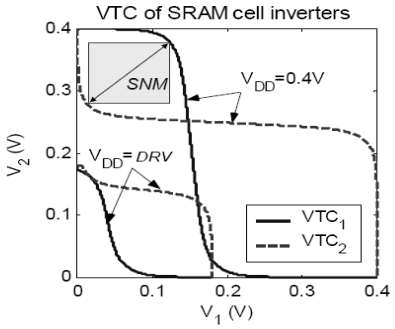

Figure 2. VTC of SRAM Cell Inverters

Noise margin can be defined using the input voltage to output voltage transfer characteristic (VTC). In general, Noise Margin (NM) is the maximum spurious signal that can be accepted by the device when used in a system while still maintaining the correct operation. If the consequences of the noise applied to a circuit node are not latched, such noise will not affect the correct operation of the system and can thus be deemed tolerable. It is assumed that noise is presented long enough for the circuit to react, i.e. the noise is "static" or dc. A Static Noise Margin is implied if the noise is a dc source. In case when a long noise pulse is applied, the situation is quasi-static and the noise margin asymptotically approaches the SNM.

When V_{DD} scales down to DRV [19], the VTC of the cross-coupled inverters degrade to such a level that the loop gain reduces to one and SNM of the SRAM cell falls to zero. If V_{DD} is reduced below the DRV, the inverter loop switches to the other biased state determined by the deteriorated inverter VTC curves, and loses the capability to hold the stored data.

Since DRV is a function of the SRAM circuit parameters, a design optimization used to reduce DRV. At a fixed SNM, a lower DRV reduces the minimum standby V_{DD} and the leakage power. When the V_{DD} is fixed, a lower DRV improves the SNM and enhances the reliability of SRAM data retention. Traditionally, a standard SRAM cell is designed based on a performance-driven design methodology, which does not optimize the data retention reliability. For example, using a large NMOS pull-down device and a small PMOS pull-up device reduce data access delay, but cause a degraded SNM at low voltage. In order to gain a larger SNM and lower the DRV, the P/N strength ratio needs to be improved during the standby operation.

The global variation in V_t or L has a much weaker impact on DRV. This is because a global variation affects both inverters in the same direction and does not cause significant SNM degradation. The leakage current increases substantially with a high V_{DD}. This is caused by the DIBL (Drain Induced Barrier Lowering) effect in short channel transistors. In the DRV analysis of a typical SRAM cell, the DIBL effect can be ignored because all the SRAM transistors operate in a weak-inversion mode. But when V_{DD} is significantly higher than the DRV, the DIBL effect causes a rapid increase in leakage current. This phenomenon reflects the importance of low-voltage standby leakage control in CMOS technologies, where the short-channel effect increases.

The memory structure method is adopted to minimize the power consumption. The memory squaring technique is one of the structural method but in this, larger the number of words in a row the larger the power consumption. For this reason, as long as area is not an issue, memory squaring is not an optimal solution. A divided word line structure is a better solution. In this, the number of cells on the WL (Word Line) is the number of bits per word, so the length of the WL will vary because of this, structure cannot be expanded into large memories. The used structural method is partitioned structure; it is a superior solution [19] to the hierarchical word line structure. The partitions can be seen as independent parts that may be placed where required without the bounds given by the hierarchical word line structure.

The partitioning is implemented on 64 Kb SRAM architecture, which is an asynchronous design. The entire SRAM can be divided into four blocks. Each block is of 32x32 columns, where each word is 16

bits. The sense amplifier is placed with each column and column circuitry is placed below sense amplifier. The typical specification of the RAM is an access time of 10ns; therefore the sense amplifier is placed before column circuitry.

IV. RESULTS AND DISCUSSIONS

Core Cell SNM

The Static Noise Margin (SNM) serves as a figure of merit in stability evaluation of SRAM cells. The Fig 3 shows the simulated result of SNM for the designed SRAM. Fig 4 and 5 represents the Read and Write margin [15] simulation results respectively. After the layout and schematic designs, the DRC and LVS procedures are verified for the designs.

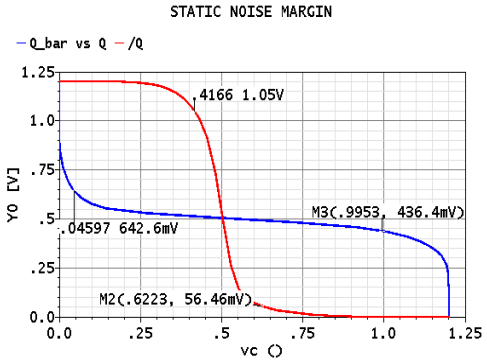

Figure 3. Static noise margin

The Fig 3 plots the voltage transfer characteristic (VTC) of Inverter 2 of Fig 1 and the inverse VTC of Inverter 1. The resulting two-lobed curve is called a "butterfly curve" and is used to determine the SNM. The internal node of the bit cell that represents a zero gets pulled upward through the access transistor due to the voltage dividing effect across the access transistor and drive transistor. This increase in voltage severely degrades the SNM during the read operation (read SNM).

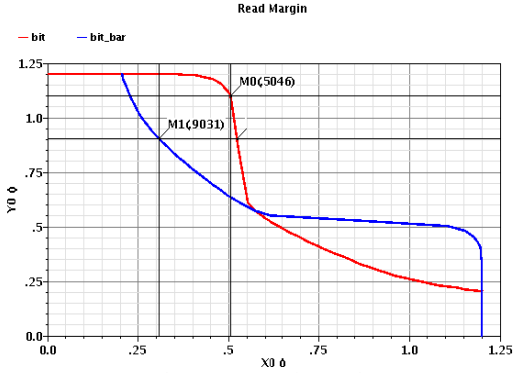

Figure 4: Read margin

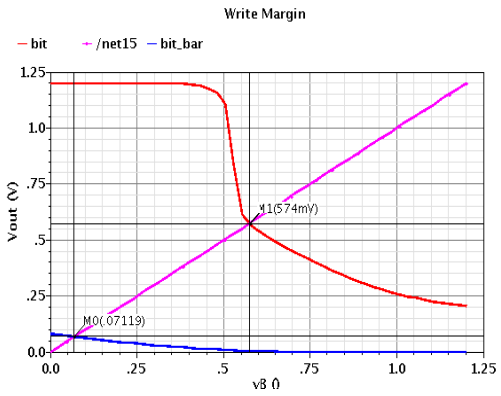

Figure 5: Write margin

TABLE I :CR vs. SNM

Technology(nm)	CR	SNM(mV)
130nm	0.8	38
	1.0	44
	1.2	48
	1.4	54
	1.6	58

The SRAM cell ratio (CR) (i.e. the ratio of the driver transistor's W/L to the access transistor's W/L) was introduced to simplify consideration of SNM optimization. The Table I show the variation of SNM with CR. From the graph of Fig 7 cell ratio vs. static noise margin, the value of static noise margin increases with the increase of cell ratio of the
SRAM cell in 130 nm technology. As the cell ratio is increased, average value of SNM increases because the driver transistor now has higher drive strength and is less susceptible to noise. At the same time, the variation in SNM reduces with increasing cell ratio. This is expected because in a wider driver transistor, there will be higher number of dopants and small variation in the number/location of these dopants will result in a smaller effect on overall device characteristics.

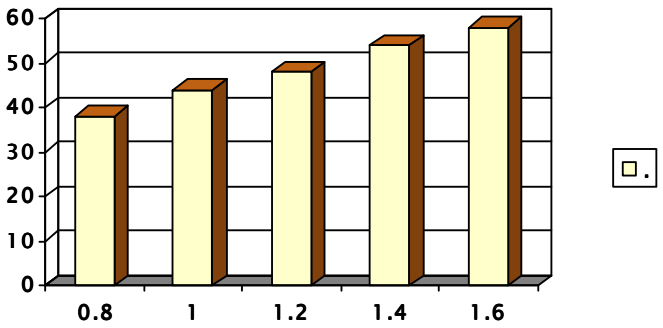

Figure 7. SNM vs. CR (130 nm)

V. CONCLUSION

This paper proposes a method to investigate optimal V_{DD} with the help of SNM and also size of the cell (CR). It also addresses the critical issues in designing a low power static RAM in Deep sub

micron (DSM) 130nm technologies. The bit cell operates properly for static noise margin of 0.466V, Read margin of 0.3985V and Write margin of 0.5028V. The feature work can be extended for minimizing leakage at architecture level and also on reconfigurable cell.

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