COMPARATIVE STUDY OF DIFFERENT SENSE AMPLIFIERS IN SUBMICRON CMOS TECHNOLOGY

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ABSTRACT

A comparison of different sense amplifiers are presented in consideration of SRAM memories using 250nm and 180nm technology. The sensing delay-time for different capacitance values of the bit line and for different values of power supply results are given by considering worst case process corners and high temperatures. The effect of various design parameters on the different sense amplifiers has been discussed and reported.

KEYWORDS: *CMOS, SRAM, CTSA, CONV, CBL, DLT*

I. INTRODUCTION

Performance of embedded memory and its peripheral circuits can adversely affect the speed and power of overall system. Sense Amplifier is the most vital circuits in the periphery of CMOS memory as its function is to sense or detect stored data from read selected memory. The performance of sense amplifiers [1] strongly affects both memory access time and overall memory power dissipation. The fallouts of increased memory capacity are increased bit line capacitance which in turn makes memory slower and more energy hungry.

A sense amplifier is an active circuit that reduces the time of signal propagation from an accessed memory cell to the logic circuit located at the periphery of the memory cell array and converts the arbitrary logic levels occurring on a bit line to the digital logic levels of the peripheral Boolean circuits.

The memory cell being read produces a current "I_{DATA}" that removes some of the charge (dQ) stored on the pre-charged bit lines. Since the bit-lines are very long, and are shared by other similar cells, the parasitic resistance "R_{BL}" and capacitance "C_{BL}" are large. Thus, the resulting bit-line voltage swing (dV_{BL}) caused by the removal of "dQ" from the bitline is very small $dV_{BL} = dQ/C_{BL}$. Sense amplifiers are used to translate this small voltage signal to a full logic signal that can be further used by digital logic.

To improve the speed, performance of memory and to provide signals which conform the requirements of driving peripheral circuits within the memory, understanding and analyzing the circuit design of different sense amplifier types and other substantial elements of sense circuits is necessary. Sense amplifiers may be classified by circuit types such as differential and non differential and by operation modes such as voltage, current and charge amplifiers. A differential sense amplifier can distinguish smaller signals from noise than its non differential counterpart, the signal detection can start sooner than in a non differential sense amplifier .Although differential sensing compromises some silicon area yet in most of the design the use of differential amplifier allow to combine very high packaging density with reasonable access time and low power consumption. The rest of the paper is organized as follows. In the section 11 describe the different sense amplifier, then in section

III describes the comparative study of different current sense amplifier ,then in section IV describe the conclusion of this paper.

II. DIFFERENTIAL SENSE AMPLIFIER

Differential sense amplifier may be classified as:

1. Voltage sense amplifier
2. Current sense amplifier
3. Charge transfer sense amplifier (CTSA)

The simplest voltage sense amplifier [2] is the differential couple. When a cell is being read, a small voltage swing appears on the bit line which is further amplified by differential couple and use to drive digital logic. However the bitline voltage swing is becoming smaller and is reaching the same magnitude as bitline noise, the voltage sense amplifier become unusable.

The fundamental reason for applying current mode sense amplifier in sense circuit is their small input impedances. Benefits of small input and output impedances are reductions in sense circuit delays, voltage swings, cross-talking, substrate currents and substrate voltage modulations.

The operation of the CTSA is based **on** the charge re distribution mechanism between very high bit-line capacitance and low output capacitance of the sense amplifier. A differential charge transfer amplifier takes advantage of the increased bit-line capacitance and also offers a low-power operation without sacrificing the speed.

2.1 Voltage sense amplifier

The voltage sense amplifier can be classified as follows

1. Basic differential voltage amplifier.
2. Simple differential voltage sense amplifier.
3. Full complementary differential voltage sense amplifiers
4. Positive feedback differential voltage sense amplifiers.
5. Full complementary positive feedback voltage sense amplifiers.

1. Basic differential voltage amplifier

The basic MOS differential voltage amplifier circuit contains all elements required for differential sensing. A differential amplifier takes small signal differential inputs and amplifies them to a large signal single ended output. The effectiveness of a differential amplifier is characterized by its ability to reject common noise and amplify true difference between the signals. Because of rather slow operational speed provided at considerable power dissipation and inherently high offset basic differential voltage amplifier is not applied in memories.

2. Simple differential voltage sense amplifier

It has less power dissipation and offset in comparison of basic differential voltage sense amplifier. The simultaneous switching of load devices is fundamental drawback of differential voltage sense amplifier in obtaining fast sensing operation.

3. Full complementary differential voltage sense amplifiers

The full complementary sense amplifier [3] reduces the duration of signal transients by using active loads in large signal switching, improves small signal amplification and common mode rejection ratio (CMRR) by providing virtually infinite load resistances and approximately constant source current of the inception of signal sensing. The full complementary differential sense amplifier is able to combine high initial gain, common mode rejection ratio, a large input impedance and small output impedance. The operation can be made even faster by using positive feedback.

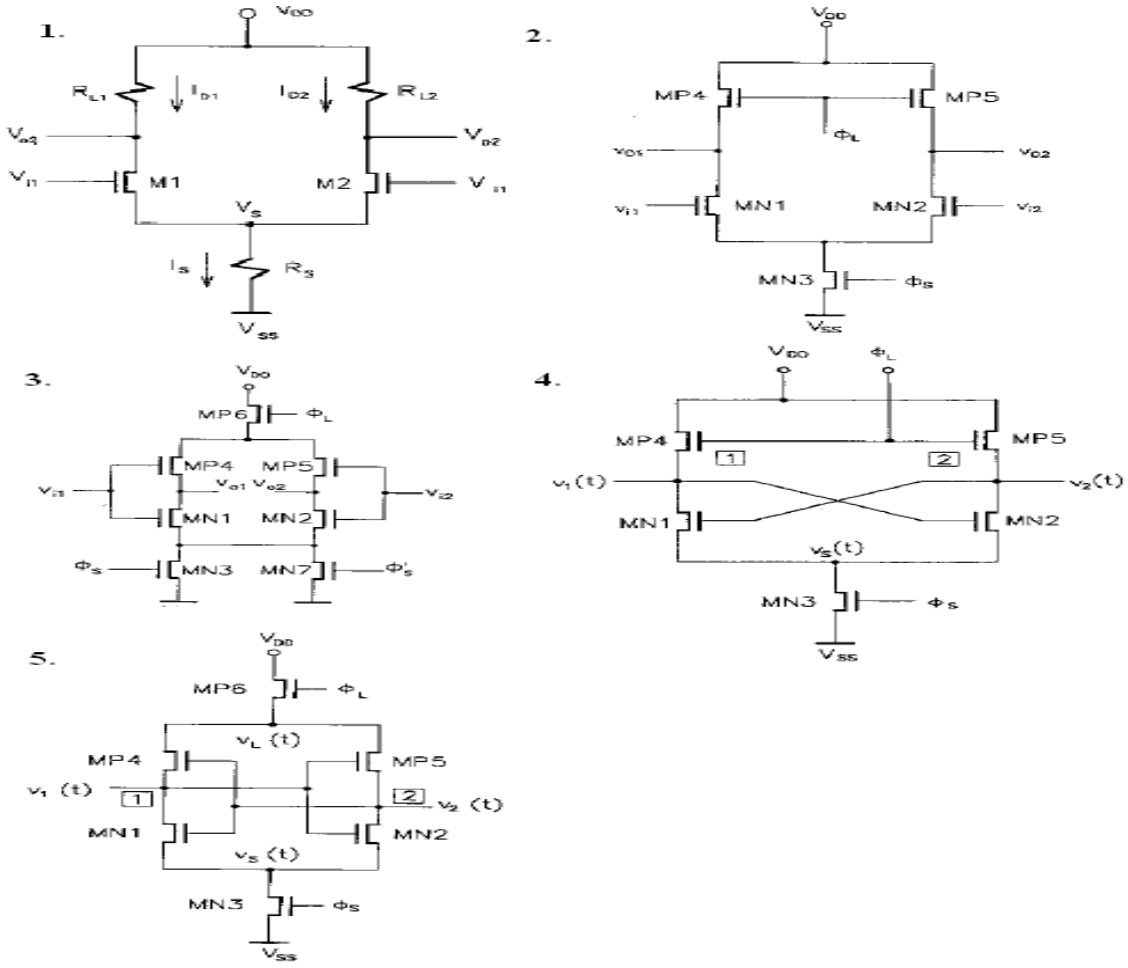

Figure 1.Basic differential voltage amplifier, Figure 2. Simple differential voltage sense amplifier**,** Figure 3.Full complementary differential voltage sense amplifiers, Figure 4.Positive feedback differential voltage sense amplifiers**,** Figure 5.Full complementary positive feedback voltage sense amplifiers**.**

4. Positive feedback differential voltage sense amplifiers

The positive feedback in differential sense amplifiers [4] makes possible to restore data in DRAM cell simply, increases the differential gain in the amplifier and reduces switching times and delays in sense circuit.

5. Full complementary positive feedback voltage sense amplifiers

The full complementary positive feedback sense amplifier improves the performance of simple positive feedback amplifier by using an active circuit constructed of devices MP4, MP5 and MP6 in positive feedback configuration.

There are many ways of enhancing the performance of different voltage mode sense amplifier by adding a few devices to the differential voltage sense amplifier. Out of these few ways are

1. Temporary decoupling of bit lines from the sense amplifiers.
2. Separating the input and output in feedback sense amplifiers.
3. Applying constant current source to the source devices,
4. Optimizing the output signal amplitude.

Approaches (1) and (2) decreases capacitive load of sense amplifier. By approach (3) the sense amplifier source resistance is virtually increased to achieve high gain, and by approach (4) amount of switched charges is decreased.

2.2 Current sense amplifier

Current sense amplifier can be broadly classified as:

1. Conventional current mode sense amplifier
2. Conventional current mirror sense amplifier
3. Clamped bit line sense amplifier
4. Simple 4T sense amplifier
5. PMOS bias type sense amplifier
6. Differential latch type sense amplifier.
7. Hybrid current sense amplifier

1) Conventional current mode sense amplifier

The conventional current mode sense amplifier [6] (CONV) is illustrated in Figure 6. The design of the sensor is based on the classic cross-coupled latch structure (M4-M7) with extra circuitry for sensor activation (M8) and bit-line equalisation (Ml-M3). The operation of the sense amplifiers presents two common phases: precharge and sense signal amplification. In the precharging phase the EQ signal is low and the bit-lines are precharged to V_{dd}. In the sensing phase the EQ and EN signals go to high. This activates the cross-coupled structure and drives the outputs to the appropriate values.

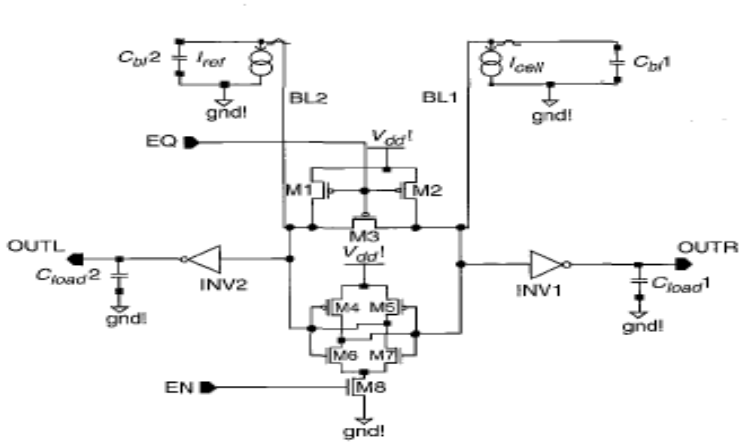

Figure 6. Conventional current mode (CONV) sense amplifier

This structure is suitable for realizing high speed and large size memories. Also suitable for low voltage operation, as no large voltage swing on the bitline is needed. However the performance of this sense amplifier structure is strongly dependent on C_{bl} , because output node is loaded with bitline capacitance. The performance is also degraded at low voltage operati on (<1.5V).

2) Conventional current mirror current mode sense amplifier

This architecture includes two current-mirror cells shown in figure 7 that copy the current of bit-lines and then subtract them and the outputs are complementary. This conventional sense amplifier uses simple current mirror cell which has a strong dependence of the output current on output voltage. To minimize the effect of finite output impedance, a cascade configuration can be used. The improved Wilson mirror cell also can be used in a current sense amplifier [7]. This type of sense amplifier has increased output impedance compared to conventional configuration. To minimize the loading effect, input impedance can be decreased with an active gain element in the feedback loop of a conventional current mirror cell [8].

3) Clamped bit line sense amplifier

Figure 8 presents the clamped bit-line sense amplifier (CBL). The circuit is able to respond very rapidly, as the output nodes of the sense amplifier are no longer loaded with bitline capacitance. The

input nodes of the sense amplifier are low impedance current sensitive nodes. Because of this the voltage swing of the highly capacitance bitlines change is very small.

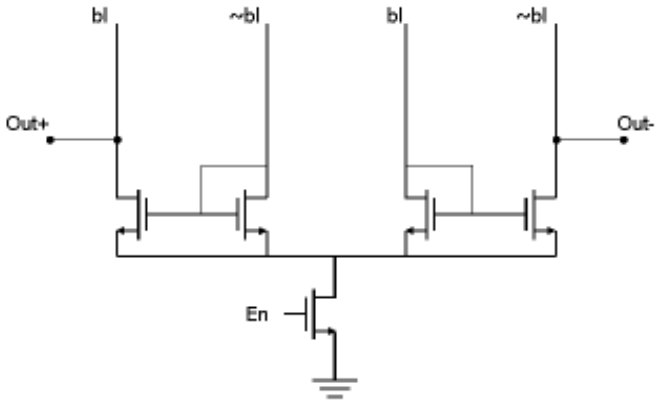

Figure 7.Conventional current mode sense amplifier

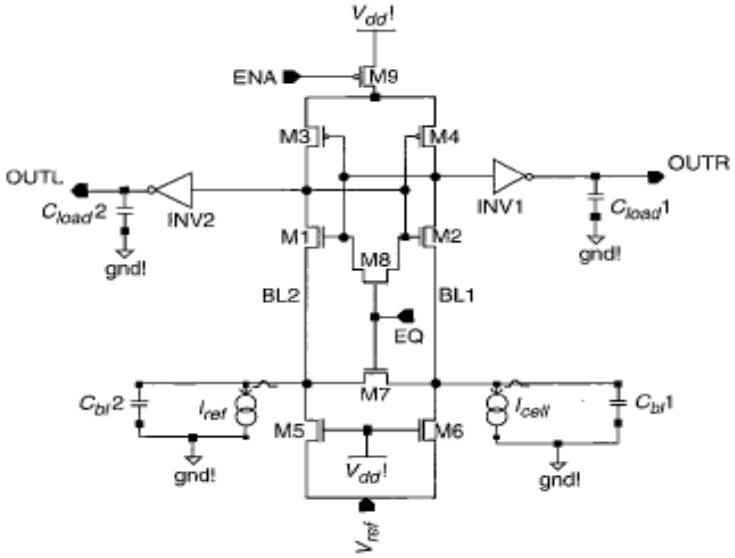

Figure 8.Clamped bit-line (CBL) sense amplifier

The improvement in the driving ability [9] of output nodes due to positive feedback and the small difference can be detected and translated to full logic. The is almost insensitive to technology and temperature variations. The main limitation of this circuit is that the bitlines are pulled down considerably from their precharge state through the low impedance NMOS termination. This result in significant amount of energy consumption in charging and discharging the highly capacitive bitlines. Also, the presence of two NMOS transistors in series with the cross-coupled amplifier results in an increase in the speed of amplification.

4) **Simple 4T current sense amplifier**

The simple four-transistor (SFT) current mode sense amplifier [10] is shown in Figure 9. This SA consists of only four equal-sized PMOS transistors. This configuration consumes lowest silicon area and is most promising solution for low power design.

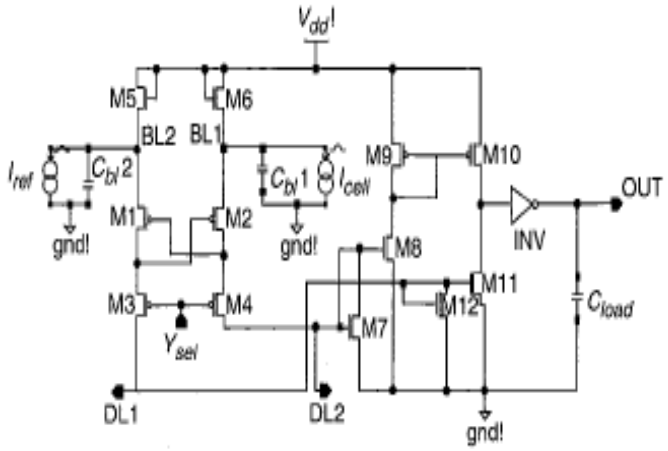

Figure 9. Simple four transistor (SFT) sense amplifier

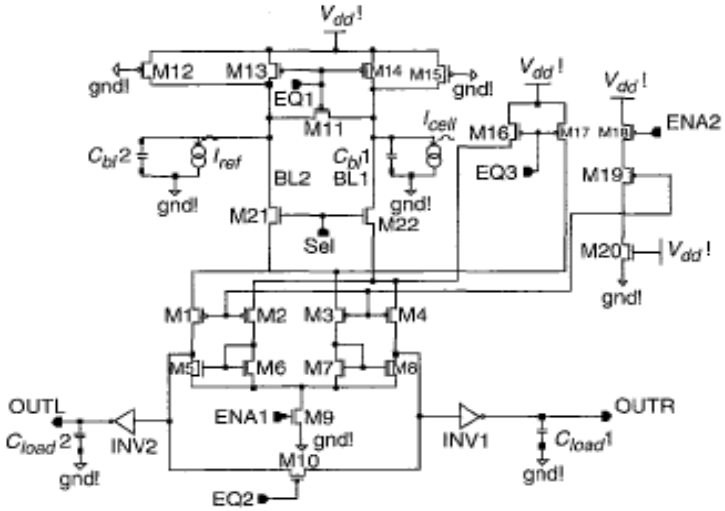

Figure 10. PMOS bias type (PBT) sense amplifier

In many cases it can fit in the column pitch, avoiding the need for column select devices, thus reducing propagation delay. This type of sense amplifier presents a virtual short circuit across the bitlines therefore the potential of the bitlines will be independent of the current distribution. The sensing delay is unaffected by the bitline capacitance since no differential capacitor discharging is required to sense the cell data. Discharging current from the bitline capacitors, effectively precharge the sense amplifier. However the performance is strongly affected at lower voltage operation. At lower power supply SFT is more sensitive than the CBL.

5) **PMOS bias type sense amplifier**

The PMOS bias type (PBT) current mode sense amplifier is shown in Figure 10. In the operation of this current sense amplifier, the voltage swing on the bit-lines or the common data lines does not play an important role in obtaining the voltage swing in the sense amplifier output. This means that the current sense amplifier can be used with a very small bit-line voltage swing, which shortens the bit-line signal delay without pulsed bit-line equalisation. In the sensing circuitry, a normally-on equalizer is used in the read cycle to make the bit-line voltage swing small enough to attain a fast bit-line signal transition. Omitting the pulsed bit-line equalisation is also a power-saving factor.

6) **Differential latch type sense amplifier**

The differential latch type sense amplifier (DLT) is shown in Figure 11. This sense amplifier also has separated inputs and outputs for low voltage operation and for the acceleration of the sensing speed. The DLT can satisfactorily operate with low voltages, even under worst-case and high temperature

conditions, with no significant speed degradation. This sense amplifier provides the most promising solutions in low power designs.

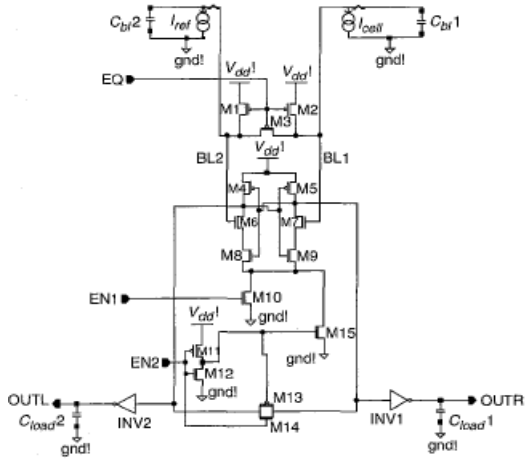

Figure 11. Differential latch type (DLT) sense amplifier

7) **Hybrid current sense amplifier**

A hybrid current sense amplifier is shown in Figure 12. It introduces a completely different way of sizing the aspect ratio of the transistors on the data-path, hence realizing a current-voltage hybrid mode Sense Amplifier.

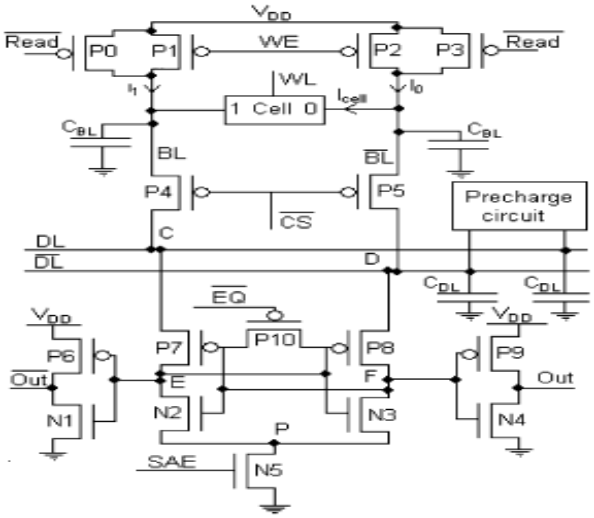

Figure 12. Hybrid current sense amplifier

It introduces a new read scheme that creatively combines the current and voltage-sensing schemes to maximize the utilization of I_{cell}, hence offering a much better performance in terms of both sensing speed and power consumption. Since only one of the BLs and one of the DLs are discharged to lower levels than V_{dd} while their complementary lines are kept at V_{dd}. The new SA is insensitive to the difference between C_{DL} and $C_{\overline{DL}}$. This feature helps it to cope with the increasing fluctuation of these parasitic capacitances due to the layout and fabrication processes. The new design can operate in a wide supply voltage range, from 1.8 to 0.9 V with minimum performance degradation.

III. COMPARATIVE STUDY OF DIFFERENT CURRENT SENSE AMPLIFIER

Table I present the sensing delay time, for different capacitance values of the bit-line. The CBL and DLT circuits exhibit a performance independent of the bitline capacitance (C_{BL}), while the performance of the rest of the sense amplifier circuits is strongly dependent on C_{BL}.

Table II show the worst sensing delay time, for different values of the power supply voltage. The DLT can satisfactorily operate with low voltages, even under worst case and high temperature conditions, with no significant speed degradation. The performance of the CBL design is limited down to 1.5 V, while for lower V_{dd} values the delay time significantly increases. The sensing delay time of the PBT is not seriously affected by the V_{dd} reduction.

TABLE I: The sensing delay-time for different capacitance values of the bitline

Structures	Sensing delay-time for different C_{BL} (ns)				
	C_{BL}=1pF	C_{BL}=2pF	C_{BL}=3pF	C_{BL}=4pF	C_{BL}=5pF
CONV_CSA	8	16	21	23	25
CM_CSA*	1	4	8	11	14
CBL_CSA	0.5	0.6	0.6	0.6	0.6
SFT_CSA	2	2.5	2.8	3	4
PBT_CSA	3	5	7	9	11
DLT_CSA	0.6	0.8	0.8	0.8	0.8
HBD_CSA*	0.3	0.3	0.3	0.3	0.3

Channel length=0.25µm; V_{dd}=2.5V; Temp. = 27^0C.
Channel length=0.18µm; V_{dd}=1.8V.

TABLE II : The sensing delay-time for different values of power supply

Structures	Sensing delay-time (ns) for different V_{dd}					
	V_{dd}=1.1V	V_{dd}=1.4V	V_{dd}=1.7V	V_{dd}=2.0V	V_{dd}=2.3V	V_{dd}=2.6V
CONV_CSA	14	11	9	8.5	8.5	8
CM_CSA*	13.4	13.39	13.42	13.4	13.4	13.43
CBL_CSA	5	2	1.5	1	0.8	0.5
SFT_CSA	7	6.8	6	2.5	2	2
PBT_CSA	5	4.5	4	3.5	3	3
DLT_CSA	2	1.5	1	1	1	1
HBD_CSA*	0.6	0.5	0.3	0.2	0.2	0.2

Channel length=0.25µm; C_{BL}=1pF; Temp. = 27^0C.
*Channel length=0.18µm

IV. CONCLUSION

A comparative study of various sense amplifiers proposed has been carried out. These sense amplifiers have been designed in 250nm and 180nm CMOS technology. According to these results, the CBL and DLT circuits exhibit a performance independent of the bit-line capacitance (C_{BL}) and the performance of the CBL design is limited down to 1.5V. The feature work can be done for analyzing silicon area utilization without compromising on performance.

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