

DESIGN AND VERIFICATION ANALYSIS OF APB3 PROTOCOL WITH COVERAGE

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ABSTRACT

Today in the era of modern technology micro electronics play a very vital role in every aspects of life of an individual, increasing use for micro electronics equipments increases the demand for manufacturing its components and its availability, reducing its manufacturing time, resulting in increasing the failure rate of the finished product. In order to overcome this problem the Technocrats develop a method called Verification, a process which is a part of manufacturing microelectronics products. So approximately 30% of the effort spent on the average project is consumed by design and 70% in verification. For this reason, methods which improve the efficiency and accuracy of hardware design and verification are immensely valuable. The current VLSI design scenario is characterised by high performance, complex functionality and short time-to-market. A reuse based methodology for SoC design has become essential in order to meet these challenges. The work embodied in this paper presents the design of APB 3 Protocol and the Verification of slave APB 3 Protocol. Coverage analysis is a vital part of the verification process; it gives idea that to what degree the source code of the DUT has been tested. The Functional coverage analysis increases the verification efficiency enabling the verification engineer to isolate the areas of un-tested function. The design and verification IP is built by developing verification components using Verilog and System Verilog respectfully with relevant tools such as Riviera, which provides the suitable building blocks to design the test environment.

KEYWORDS: *AMBA (Advanced Microcontroller Bus Architecture), APB(Advanced peripheral Bus), Functional coverage analysis, RTL (Register Transfer Level) design, System Verilog, SOC (System on chip), DUT (Design Under Test), Design intellectual property (DIP), Verification intellectual property (VIP).*

I. INTRODUCTION

Intellectual Property (IP) Cores are of first line of choice in the development of Systems-on-chip (SOC). Typically, a SoC is an interconnection of different pre-verified IP blocks which communicate using complex protocols. Approaches adopted to facilitate plug and- play style IP reuse include the development of a few standard on-chip bus architectures such as CoreConnect[11] from IBM, AMBA[9] from ARM among others, and the work of the VSI Alliance[8] and the OCP-IP[10] consortium. Designers are usually provided with voluminous specifications of the protocols used by the IP blocks and the underlying bus architecture. IP Cores are register transfer level (RTL) codes which achieve certain desired functionality. Today the foundation of digital systems design depends on Hardware description languages (HDLs) rather than schematic diagrams. These RTL codes are well tested codes which must be ready for any use in SOC development.

Modern computer systems rely more and more on highly complex on-chip communication protocol to exchange data. The enormous complexity of these protocol results from tackling high-performance requirements. Protocol control can be distributed, and there may be non-atomicity or speculation. The electronics industry has entered the era of multi-million-gate chips, and there is no turning back. This technology promises new levels of integration on a single chip, called the System-on-a- Chip (SOC) design, but also presents significant challenges to the chip designer. Processing cores on a single chip,

may number well into the high tens within the next decade, given the current rate of advancements [1]. The important aspect of a SOC is not only which components or blocks it houses, but also how they are interconnected. The current VLSI design scenario is characterised by high performance, complex functionality and short time-to-market. A reuse based methodology for SOC design has become essential in order to meet these challenges. AMBA is a solution for the blocks to interface with each other.

In the present paper the discussion is made on the Design intellectual property (DIP) of the master and slave of the APB3 protocols and the Verification intellectual property (VIP) slave with coverage analysis.

II. OBJECTIVE OF THE AMBA

The objective of the AMBA specification [1] is to:

1. facilitate right-first-time development of embedded microcontroller products with one or more CPUs, GPUs or signal processors,
2. be technology independent, to allow reuse of IP cores, peripheral and system macrocells across diverse IC processes, encourage modular system design to improve processor independence, and the development of reusable peripheral and system IP libraries
3. Minimize silicon infrastructure while supporting high performance and low power on-chip communication.

2.1 History of AMBA

The AMBA was introduced by ARM in 1996 and is widely used as the on-chip bus in SoC designs. AMBA is a registered trademark of ARM. The first AMBA buses were ASB and APB. In its 2nd version, AMBA 2, ARM [2] added AMBA AHB that is a single clock-edge protocol. In 2003, ARM introduced the 3rd generation, AMBA3 [3], including AXI to reach even higher performance interconnect and the Advanced Trace Bus (ATB) as part of the Core Sight on-chip debug and trace solution. In 2010, ARM introduced the 4th generation, AMBA 4,[1] including AMBA 4 AXI4, AXI4-Lite, and AXI4-Stream Protocol, the AMBA 4.0 protocol defines five buses/interfaces:

- Advanced extensible Interface (AXI)-A high performance ,flexible protocol
- Advanced High-performance Bus (AHB)-retained for compatibility and to ease the transition
- Advanced System Bus (ASB)- no longer actively supported
- Advanced Peripheral Bus (APB) - retained for support of simple, low bandwidth peripherals
- Advanced Trace Bus (ATB)

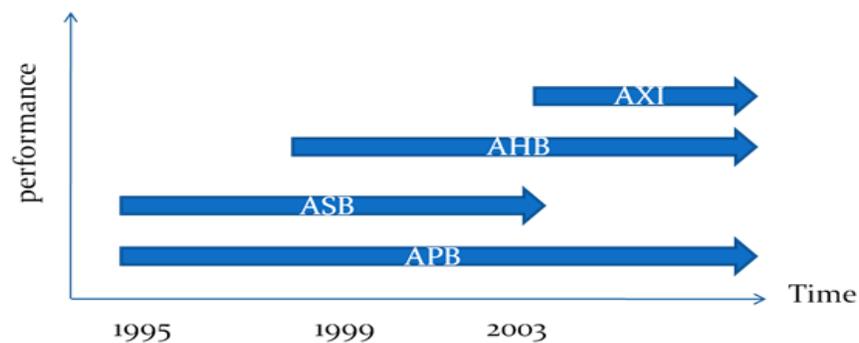


Figure 1. Protocols of AMBA

2.2. AMBA Protocol Family

AHB (Advanced High Performance Bus) is for high performance, high clock frequency system modules with suitable for medium complexity and performance connectivity solutions. It supports multiple masters.

AHB-Lite is the subset of the full AHB specification which intended for use where only a single master is used.

APB (Advanced Peripheral Bus) mainly used as an ancillary or general purpose register based peripherals such as timers, interrupt controllers, UARTs, I/O ports, etc. It is connected to the system bus via a bridge, helps reduce system power consumption. It is also easy to interface to, with little logic involved and few corner- cases to validate.

III. ABOUT APB 3 PROTOCOL

3.1 An AMBA APB 3 Typical System [1][15]

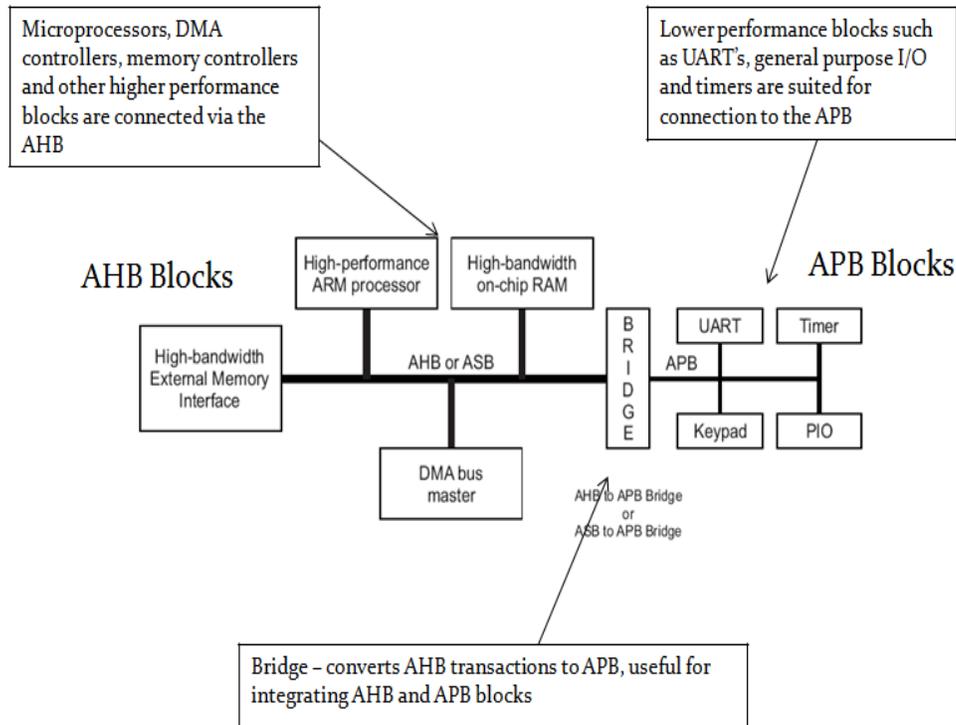


Figure 2. AMBA APB3 Typical System

Figure 2 illustrates a typical AMBA system. Several master or slave devices are connected via AHB which are often used as system bus. The data transfer between each memory module and peripheral devices also can be done by it. The bridge locates between system bus and peripheral bus. While transferring data from processor to peripheral devices like URAT, timer, peripheral I/O and keyboard, the bridge convert the transferred signal from one type to another for satisfying different performance and protocol.

The APB 3 provides a low-cost interface that is optimized for minimal power consumption and reduced interface complexity. The APB interfaces to any peripherals that are low-bandwidth and do not require the high performance of a pipelined bus interface. The APB has unpipelined protocol.

All signal transitions are only related to the rising edge of the clock to enable the integration of APB peripherals easily into any design flow. Every transfer takes at least two cycles.

The APB can interface with the AMBA Advanced High-performance Bus Lite (AHB-Lite) and AMBA Advanced Extensible Interface (AXI). You can use it to provide access to the programmable control registers of peripheral devices.

3.2. AHB VS APB [2][16]

Table1. AHB vs APB

	AMBA AHB	AMBA APB
Feature	<ul style="list-style-type: none"> •High performance •Pipelined operation •Multiple bus masters •Burst transfers •Split transactions •Single cycle bus master handover •Single clock edge operation (rising edge) •Wider data bus configuration 	<ul style="list-style-type: none"> •Low power •Latched address and control •Simple interface •Suitable for many peripherals •Single clock edge operation (rising edge)
components	<ul style="list-style-type: none"> •AHB master •AHB slave •AHB arbiter •AHB decoder 	<ul style="list-style-type: none"> •APB bridge (slave on AHB or ASB) •APB slave

3.3. When to use AHB OR APB [17][18]

AHB uses a full duplex parallel communication. It used in external memory interface, with high bandwidth peripheral with FIFO interfaces. It is also used in on chip memory blocks whereas the APB uses massive memory-I/O accesses.

The APB is mainly proposed for connecting to simple peripherals. It can be seen that the APB comes with a low power peripheral. This Bus can also be used in union with either version of the system bus. It group narrow bus peripherals to avoid loading the system bus.

Separate the bus address decoding into two levels make it easier (in most cases) to do timing budget. The address decoding logic will be easier to design as well. Usually, AHB decoder is used to decode larger memory blocks. And then I/O space (small memory blocks) is decoded by APB decoder (inside APB Bus Bridge).

E.g. you might have 4 memory blocks and 20 I/O devices. If you put them all into one level of address decoding, you might end up a big bus multiplexer which operates at lower clock frequency.

By separating I/O devices in APB memory map, you can have a smaller and faster AHB interconnect, and a second level of APB interconnect which might take one or two more extra cycle to access.

IV. APB3 FSM DIAGRAM

Figure 3 shows the Finite State diagram of peripheral bus activity of the APB[14].

IDLE This is the default state of the APB.

SETUP When a transfer is required the bus moves into the SETUP state, where the appropriate select signal, **PSELx**, is asserted. The bus only remains in the SETUP state for one clock cycle and always moves to the ACCESS state on the next rising edge of the clock.

ACCESS The enable signal, **PENABLE**, is asserted in the ACCESS state. The address, writes, select, and write data signals must remain stable during the transition from the SETUP to ACCESS state.

Exit from the ACCESS state is controlled by the **PREADY** signal from the slave:

- If **PREADY** is held LOW by the slave then the peripheral bus remains in the ACCESS state.

- If **PREADY** is driven HIGH by the slave then the ACCESS state is exited and the bus returns to the IDLE state if no more transfers are required. Alternatively, the bus moves directly to the SETUP state if another transfer follows

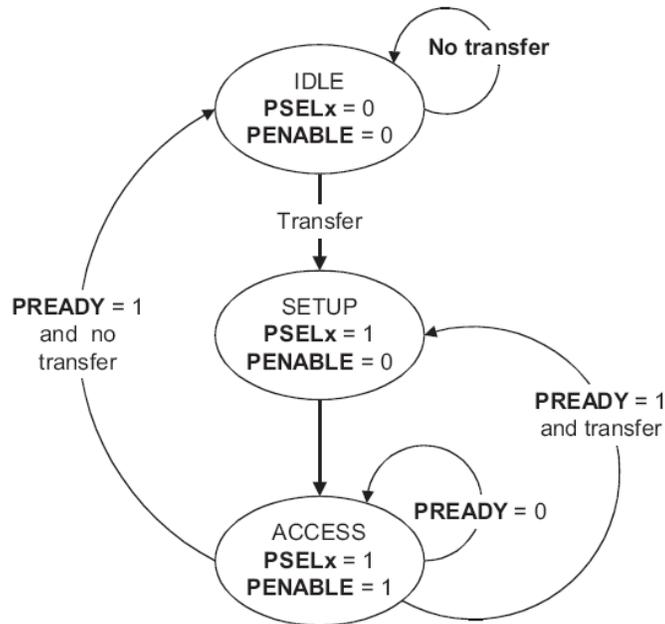


Figure 3. FSM diagram of APB3

V. MICRO ARCHITECTURE OF APB3

Figure 4. shows the micro architecture of APB3 Protocols[1]

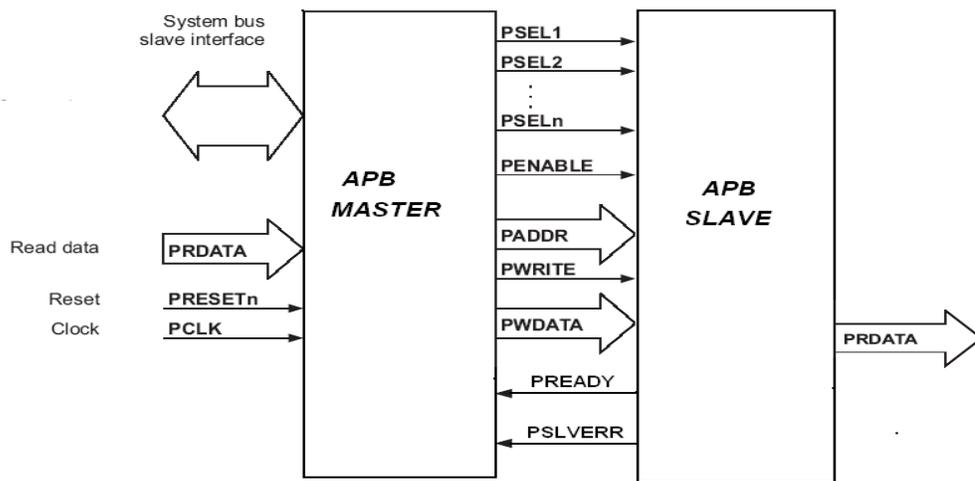


Figure 4. Interfacing of APB Master and Slave

5.1 APB3 Master Description

There is a single bus master on the APB, thus there is no need for an arbiter. The master drives the address and write buses and also performs a combinatorial decode of the address to decide which

PSELx signal to activate. It is also responsible for driving the PENABLE signal to time the transfer. It drives APB data onto the system bus during a read transfer.

5.2 APB3 Slave

APB slaves have a very simple, yet flexible, interface. The exact implementation the interface will be dependent on the design style employed and many different options are possible. In this two signals are main which mainly protect the loss data while transfer of data is taking place they are PSLVERR and PREADY.

VI. SIMULATION RESULTS OF DESIGN OF APB3

6.1. Master of APB3

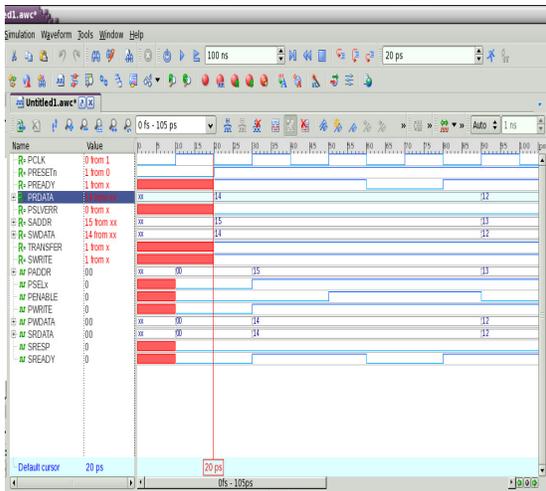


Figure 5. Read Operation

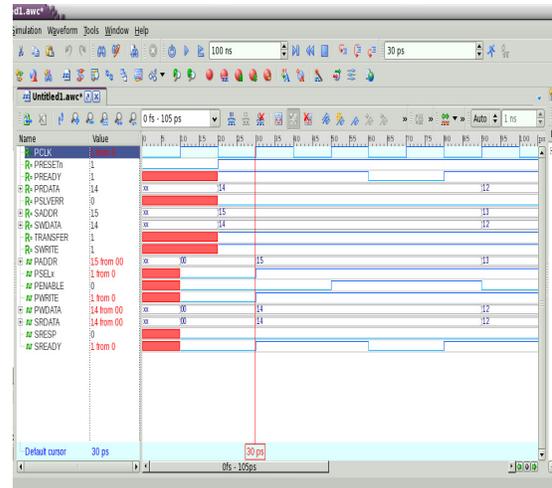


Figure 6. Write Operation

Figure 5 and Figure 6 shows the simulated result of the master APB3 read operation and write operation respectively. The main observation is made in the master APB3 is that, the data which the master has read by signal PRDATA (which is input of signal of master) is able to write by signal PWDATA (which is output signal of master) after certain clock pulse for the transfer purpose. Figure 6 shows the data that has been written what has been read in Figure 5.

6.2. SLAVE OF APB3

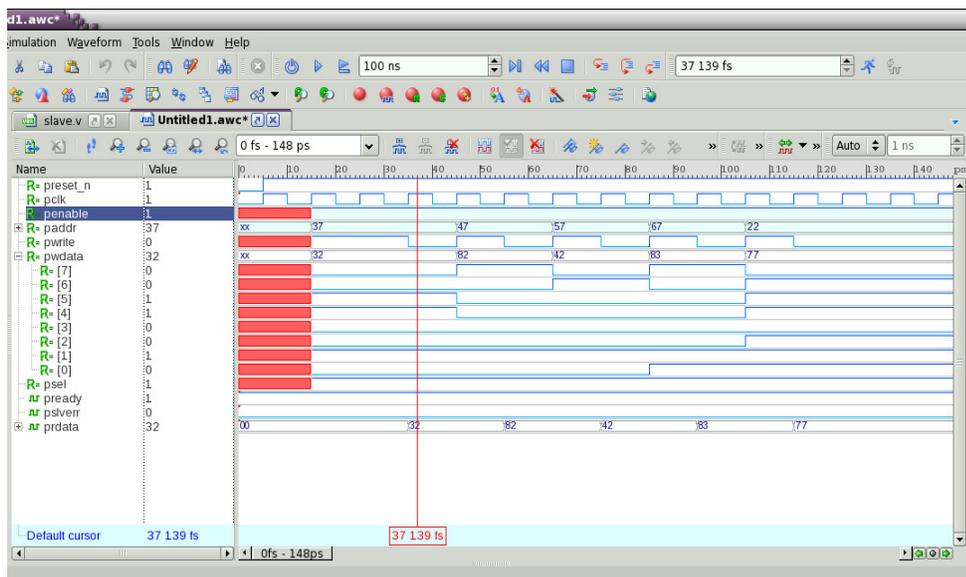


Figure 7. Write and Read Operation

Work of slave is to read that data by the signal PRDATA (which is output of slave) which was written the signal PWDATA (which is input of master). Figure 7 shows the simulate result of slave DIP in which PRDATA is same as PWDATA.

VII. SIMULATION RESULT OF VERIFICATION OF APB 3

In this paper the simulate result of VIP of slave of APB3 is shown.

7.1 SLAVE VERIFICATION

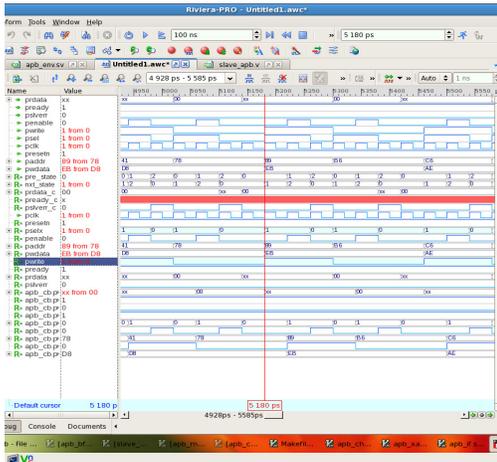


Figure 8. Write Operation

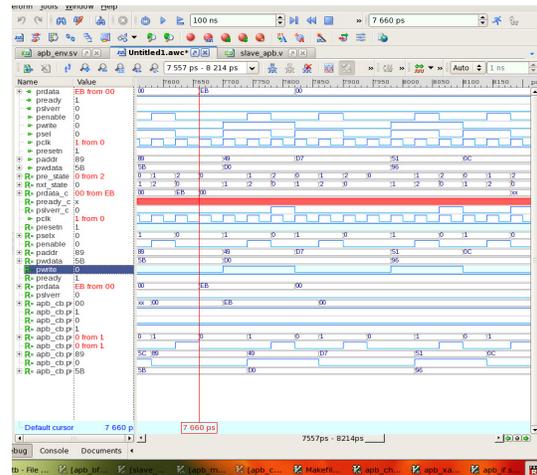


Figure 9. Read Operation

In the Figure 8 there are numbers of signals are shown. In which we can see the signal PWDATA which is for receiving the data from the master. This we have to verify that whether the data which we received in PWDATA can be read in PRDATA .In Figure 9 it is shown that the data which is written in signal PWDATA has been written in signal PRDATA.

VIII. COVERAGE ANALYSIS

The Coverage Summary and Coverage Report gives the details of the functional coverage when complete Analysis was done for the decoder and coverage report as shown in Figure 10 was generated it is found that the coverage is less than 100%.

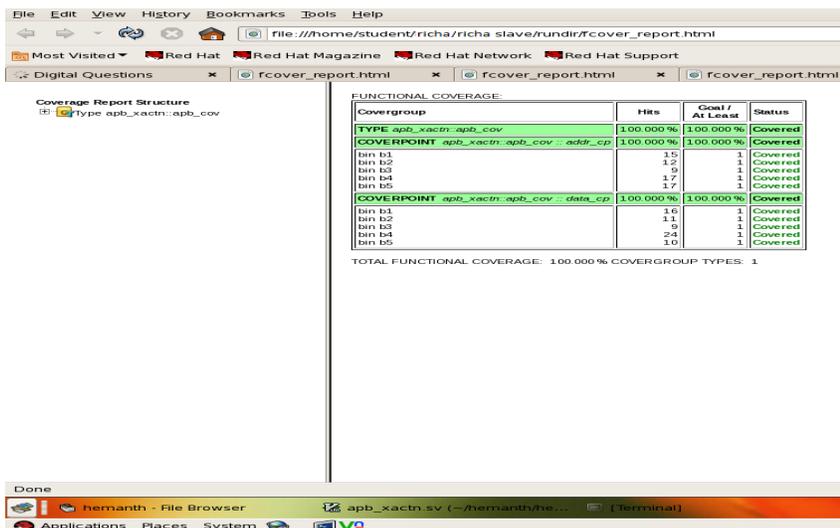


Figure 10. Coverage Result

IX. CONCLUSION

In the paper a general definition for APB3 protocol flexibility and compatibility is shown. We describe study of AMBA3 APB SOC bus protocol and their performance. Here the design and verification of low peripheral processor's data transfer protocol has been discussed. And also how the error has been reduced without loss of data while transferring.

ACKNOWLEDGEMENT

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