

DESIGN OF ENERGY-EFFICIENT FULL ADDER USING HYBRID-CMOS LOGIC STYLE

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ABSTRACT

We present new designs for full adder featuring hybrid-CMOS design style. The quest to achieve a good-drivability, noise-robustness and low energy operations guided our research to explore hybrid-CMOS style design. Hybrid-CMOS design style utilizes various CMOS logic style circuits to build new full adders with desired performance. We also classify hybrid-CMOS full adders into three broad categories based upon their structure. Using this categorization, many full adder designs can be conceived. The new full adder is based on XOR-XOR Hybrid CMOS model that gives XOR and XOR full swing output simultaneously. This circuit's outperforms its counterparts showing 4%-31% improvement in power dissipation and delay. The output stage also provides good driving capability and no buffer connection is needed between cascaded stages. During our experiments, we found out that many of the previously reported adders suffered from the problems of low swing and high noise when operated at low supply voltages. The proposed full adders are energy efficient and outperform several standard full adders without trading of driving capabilities and reliabilities. The new full-adder circuits successfully operate at low voltages with excellent signal integrity and driving capability. The new adders displayed better performance as compared to the standards full adder. The problem we face during the experiment leads us to different zones where efficient circuit can be developed using this new full adder.

KEYWORDS: Adders, Exclusive OR gate (XOR), Exclusive NOR gate (XNOR), Multiplexer, Hybrid-CMOS design style, low power.

I. INTRODUCTION

The necessity and popularity of portable electronics is driving designers to endeavor for smaller area, higher speeds, longer battery life and more reliability. Power and delay are the premium resources a designer tries to save when designing a system. The most fundamental units in various circuits such as compressors, comparators and parity checkers are full adders [1]. Enhancing the performance of the full adders can significantly affect the overall system performance. Figure 1 shows the power consumption breakdown in a modern day high performance microprocessor [2]. The data path consumes roughly 30% of the total power of the system [19] [23]. Adders are an extensively used component in data path and therefore careful design and analysis is required.

So far several logic styles have been used to design full adders. Each design has its own pros and cons. Classical designs use only one logic style for the whole full adder design. One example of such design is the standard static CMOS full adder [3]. The main drawback of static CMOS circuits is the existence of the PMOS block, because of its low mobility compared to the NMOS devices. Therefore, PMOS devices need to be sized up to attain the desired performance. Another conventional adder is the complementary pass-transistor logic (CPL) [3]. Due to the presence of lot of internal nodes and static inverters, there is large power dissipation. The dynamic CMOS logic provides a high speed of operation; however, it has several inherent problems such as charge sharing and lower noise immunity. Some other full adder designs include transmission-function full adder (TFA) [4] and

transmission –gate full adder (TGA) [5]. The main disadvantages of these logic styles are that they lack driving capability and when TGA and TFA are cascaded, their performance degraded significantly [23].

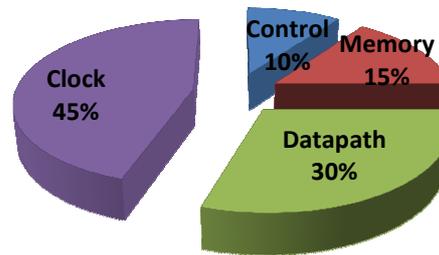


Figure 1: Power breakdown in high-performance microprocessors

The remaining adder designs use more than one logic style for their implementation which we call the hybrid-CMOS logic design style. Examples of adders built with this design style are DB cell [6], NEW 14-T adder [7], and hybrid pass logic with static CMOS output drive full adder [8] and new-HPSC [9] adder. All hybrid designs use the best available modules implemented using different logic styles or enhance the available modules in an attempt to build a low power full adder cell. Generally, the main focus in such attempts is to reduce the numbers of transistors in the adder cell and consequently reduce the number of power dissipating nodes. This is achieved by utilizing intrinsically low power consuming logic style TFA or TGA or pass transistors. In doing so, the designers often trade off other vital requirements such as driving capability, noise immunity and layout complexity. Most of these drivers lacking driving capabilities as the inputs are coupled to the outputs. Their performance as a single unit is good but when larger adders are built by cascading these single unit full adder cells, the performance degrades drastically [21] [25]. The problem can be solved by inserting buffers in between stages to enhance the delay characteristics. However, this leads to an extra overhead and the initial advantage of having a lesser number of transistors is lost.

A hybrid-CMOS full adder can be broken down into three modules [6]. Module-I comprises of either a XOR or XNOR circuits or both. This module produces intermediate signals that are passed onto Module-II and Module-III that generate Sum and C_{out} outputs, respectively. There are several circuits available in [1], [6] and [7] for each module and several studies have been conducted in the past using different combinations to obtain many adders [1], [6], [10].

This paper is structured as follows: Section 2 and its subsections briefly introduce three categorized model of full adder. Section 3 and its subsections represent our proposed circuits for three different Modules where we present a new improved circuit for the simultaneous generation of the XOR and XNOR outputs to be used in Module-I and propose a new output unit for Module-II and Module-III which consist of XOR-XNOR or Multiplexer. Using the new circuits in Module-I, II and III, we build new hybrid-CMOS full-adder cells which is discuss in Section 4. Section 5 briefly exhibits the results and discussion. The new adder is optimized for low power dissipation and delay then it is compared with the classical static-CMOS, CPL, TFA, TGA, NEW14T, HPSC, and NEW-HPSC full-adder cells. The proposed full-adder design exhibits full-swing operation and excellent driving capabilities without trading off area and reliability. Section 6 suggests the future work and modification of this paper. Section 7 concludes the paper.

II. FULL ADDER CATEGORIZATION

Depending upon their structure and logical expression we classified hybrid CMOS full adder cells [11] into three categories. The expression of sum and carry outputs of 1-b full adder based on binary input A, B, C_{in} are,

$$\text{Sum} = A \oplus B \oplus C_{in}$$

$$C_{out} = A \cdot B + C_{in} (A \oplus B)$$

These output expression can be expressed in various logic style and that's why by implementing those logics different full adders can be conceived. Moreover, the availability of different modules, as

discussed earlier, provides the designer with more choices for adder implementation [21] [25]. Using these different modules [8] we suggest three possible structures for full adder and these are as follows.

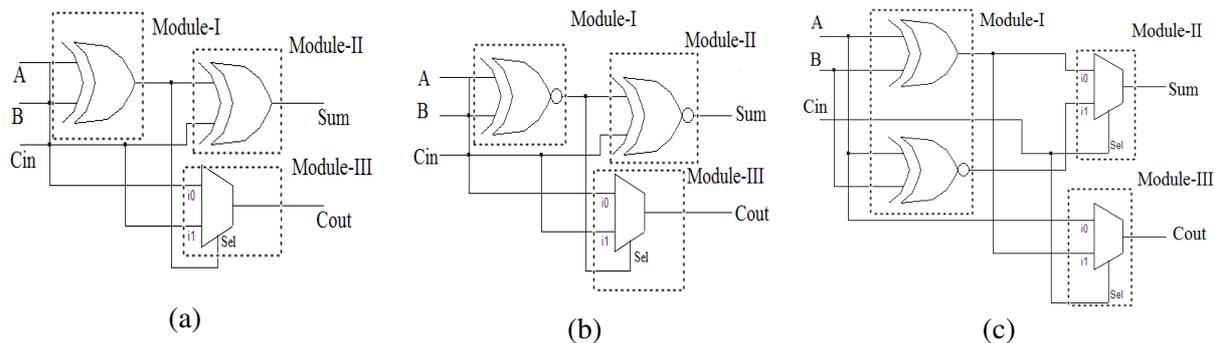


Figure 2: (a) General form of XOR-XOR based model, (b) General form of XNOR-XNOR based model, (c) General form of Centralized full adder

2.1 XOR-XOR BASED FULL ADDER

In this category, the Sum and Carry outputs are generated by the following expression, where H is equal to $A \oplus B$ and H' is the complement of H. The general form of this category is shown in Figure 2(a).

$$\text{Sum} = A \oplus B \oplus C_{in} = H \oplus C_{in}$$

$$C_{out} = A.H' + C_{in}.H$$

The output of the sum is generated by two consecutive two-input XOR gates and the C_{out} output is the output of a 2-to-1 multiplexer with the select lines coming from the output of Module-I. The Module-I can be either a XOR–XNOR circuit or just a XOR gate. In the first category, both Module-I and Module-II consist of XOR gates. In the first case, the output of the XOR circuit is again XORED with the carry from the previous stage (C_{in}) in Module- II. The H and H' outputs are used as multiplexer select lines in Module-III. The Sum adders belonging to this category are presented in [12], [13].

2.2 XNOR-XNOR BASED FULL ADDER

In this category, the Sum and Carry outputs are generated by the following expression where A, B and C_{in} are XNORed twice from the Sum and expression of C_{out} is as same as previous category. The general form of this category is shown in Figure 2 (b).

$$\text{Sum} = \overline{\overline{A \oplus B \oplus C_{in}}} = \overline{H' \oplus C_{in}}$$

$$C_{out} = A.H' + C_{in}.H$$

In this category, Module-I and Module-II consist of XNOR gates and Module-III consists of a 2-to-1 multiplexer. If the first module uses a XOR–XNOR circuit, then the H' output is XNORed with the C_{in} input to produce the Sum output. The static energy recovery full adder (SERF) [14] belongs to this category and uses a XNOR gate for Module-I and Module-II and a pass transistor multiplexer for Module- III.

2.3 CENTRALIZED FULL ADDER

In this category, the Sum and Carry outputs are generated by the following expression. The general form this category is shown in Figure 2(c).

$$\text{Sum} = H \oplus C_{in} = H.C'_{in} + H'.C_{in}$$

$$C_{out} = A.H' + C_{in}.H$$

Module-I is a XOR–XNOR circuit producing H and H' signals; Module-II and Module-III are 2-to-1 multiplexers with H and H' as select lines. The adder in [8] is an example of this category. It utilizes

the XOR–XNOR circuit presented in [7] and proposes a new circuit for output Module-III. The simultaneous generation of H and H' signal is critical in these types of adders as they drive the select lines of the multiplexers in the output stage. In another case (i.e. non simultaneous H and H'), there may be glitches and unnecessary power dissipation may occur. The final outputs cannot be generated until these intermediate signals are available from Module-I [20].

III. PROPOSED CIRCUIT FOR MODULE-I, II AND III

Hybrid CMOS full adders can be divided into three Modules. Each of the Models consists of XOR or XNOR or 2 to 1 multiplexer with selection lines. Module-I Consist of XOR or XNOR in all three categories; Module-II consists of XOR or XNOR for first two categories and 2 to 1 multiplexer for last category and Module –III consists of 2 to 1 multiplexer with selection lines in all three categories. Finally it can be said that three types of circuits used to from three categorized full adders. Here we will propose three new circuits for Module-I, Module-II and Module-III.

3.1 MODULE-I

Here we will talk about the proposed XOR and XNOR model. From the previous studies, we have found that XOR or XNOR gates based on transmission gate theory has limited transistor with enormous drawbacks. The drawbacks are the required complementary inputs and the loss of driving capability [14]. In general, if the output signals of a circuit come from V_{DD} or V_{SS} directly, we say this circuit has driving capability. If the circuit output will drive other circuits, it does better to cascade a canonical CMOS buffer to do so.

To follow without the loss of generality, all the methods we discuss will focus on the XOR function, mainly because the XNOR structure is very similar to XOR structure symmetrically. The skill for the XOR function can be applied to the XNOR function without question.

Based on the inverter configuration theory, two inverters are arranged to design XOR function as well as XNOR structure. These types of gates do not need the complementary signal inputs as like before and the driving property is better but it still have some defects such as no full driving capability on the output and more delay time [9].

In recent times simultaneous generation of XOR and XNOR has been widely used for Module-I, II [9], [14], [15]. This feature is highly desirable as non skewed outputs are generated that are used for driving the select lines of the multiplexer inside the full adder. Figure 3(a) shows a configuration using only six transistors and is presented in [14]. This circuit has been widely used to build full-adder cells [9], [14], [15]. The circuit has a feedback connection between XOR and XNOR function eliminating the non-full-swing operation [26]. The existence of V_{DD} and GND connections give good driving capability to the circuit and the elimination of direct connections between them avoids the short circuit currents component. However, when there is an input transition that leads to the input vector AB: XX-11 or AB: XX-00, there is a delay in switching the feedback transistors. This occurs because one of the feedback transistors is switched ON by a weak signal and the other signal is at high impedance state. This causes the increase in delay. As the supply voltage is scaled down, this delay tends to increase tremendously. This also causes the short circuit current to rise and causes the short circuit power dissipation to increase and eventually increase the power-delay product. To reduce this problem careful transistor sizing needs to be done to quickly switch the feedback transistors [9].

We found another improved version of XOR-XNOR circuit [8], [18], [26] which provides a full-swing operation and can operate at low voltages. The circuit is shown in figure 3(b). The first half of the circuit utilizes only NMOS pass transistors for the generation of the outputs. The cross-coupled PMOS transistors guarantee full-swing operation for all possible input combinations and reduce short-circuit power dissipation. The circuit is inherently fast due to the high mobility NMOS transistors and the fast differential stage of cross-coupled PMOS transistors. But the main drawback was it showed worse output at low voltage but at high voltage it showed completely opposite characteristic [18].

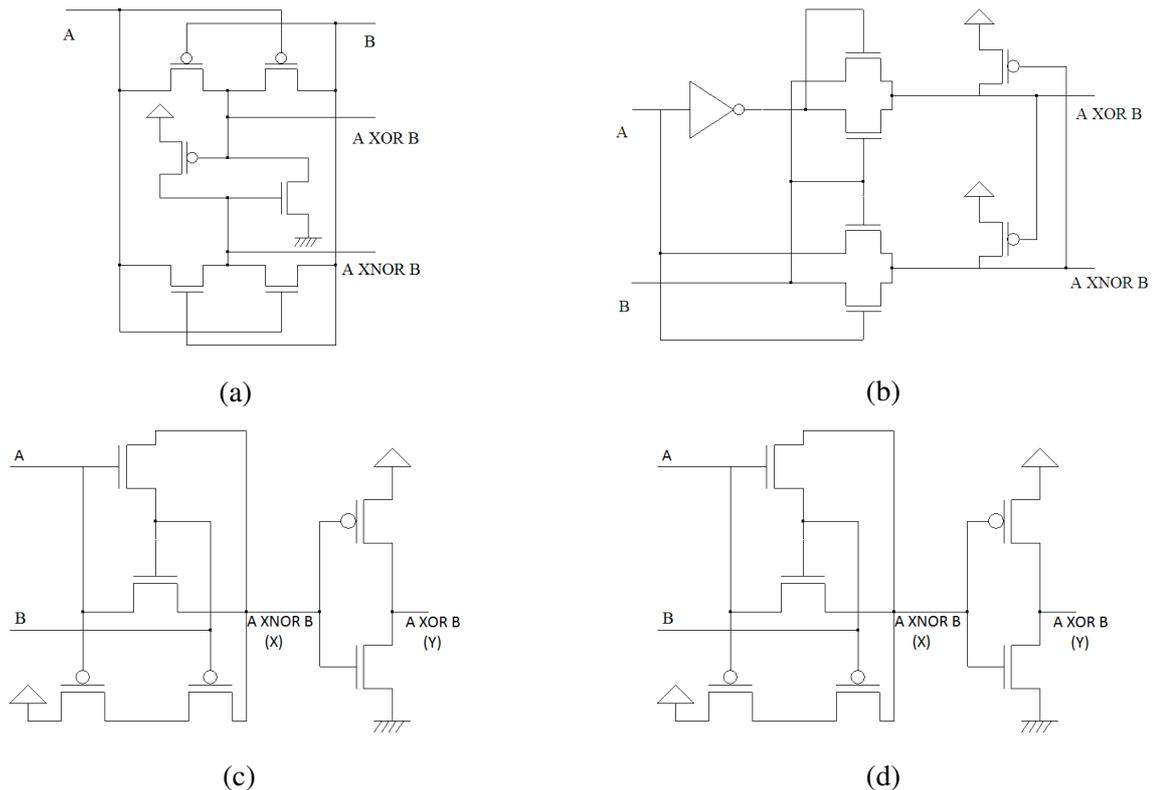


Figure 3: (a) Circuit 1 for XOR-XNOR model (b) circuit 2 for XOR XNOR model (C) Proposed XOR (d) proposed XNOR

We propose a novel XOR–XNOR circuit using six transistors that generates XOR and XNOR outputs simultaneously. Figure 3(c) and 3 (d) respectively represent Proposed XOR and XNOR circuit. On the 6-transistor design, the new proposed structures require non-complementary inputs and their output will be perfect. The initial plan was creating 4-transistor design but it was jeopardized due to worse output when both inputs were low for XOR and high for XNOR. Analysis of 4-transistor XOR structures, the output signal is the cases of input signal AB= 01, 10, 11 will be complete. When AB=00, each PMOS will be on and will pass a poor low signal at the output end. That is, if AB=00 the output end will display a voltage, threshold voltage, a little higher than low but path driving capability exist, due to NMOS being on. Hence though the output is not complete, the driving current will increase. For XNOR function, the output in the case of AB= 00, 01, 10 will be complete. While AB=11, each NMOS will be on and pass the poor high signal level to the output end. The analysis of driving capability is the same as XOR structure. By cascading a standard inverter to the XNOR circuit, a new type of 6-transistor XOR is found which will have a driving output, and the signal level at the output end will be perfect in all cases. The same property is presented in the 6-transistor XNOR structure. The proposed XOR-XNOR circuit was compared to circuits in figure 3(a) and 3(b) based on number of transistors, power and delay. In all the criteria our proposed model performs outstandingly. The simulation results at 2 V_{DD} and 2V input are shown in Table-I:

Table 1: Simulation results for the proposed XOR-XNOR Circuit at 50-MHz Frequency and 2V_{DD}

	Circuit [1]	Circuit [2]	Propose XOR	Propose XNOR
No. of Transistor	6	10	6	6
Power (μW)	7.524	8.750	4.07	4.07
Delay (ns)	0.305	0.210	0.108	0.106

3.2 MODULE-II

Here we will review some of the existing and most frequently used circuits that can be used in the different modules of the full adder. From previous studies, we learned about eight different circuits [15], [16] which performed best in their available ways with advantages and disadvantages. Among eight of them we choose the best two and used the more efficient one for our proposed model. Those two circuits are given in figure 4

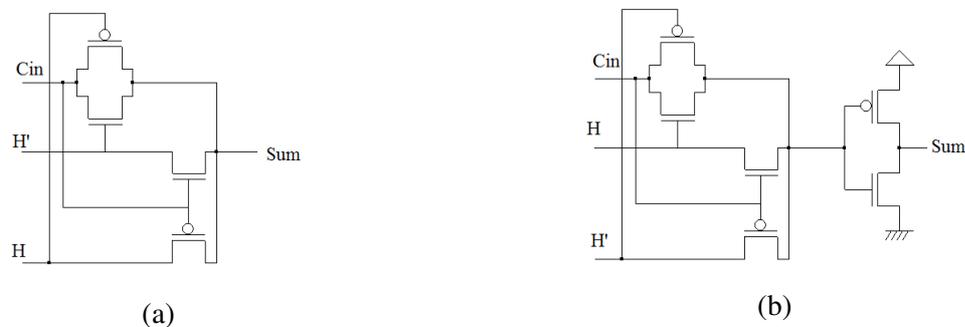


Figure 4: Circuits for Module-II

Figure 4(a) has transmission-function implementation of XOR and XNOR functions. This circuit does not have supply rails thereby eliminating short circuit current. Figure 4(b) is essentially the complement and has an inverter to produce Sum. This provides good driving capability due to the presence of the static inverter. This circuit is one of the best performers among all the circuits mentioned in [8] in terms of signal integrity and average power-delay product [6]. Both the circuits avoid the problem of threshold loss and have been widely used in adder implementation [15], [16]. We employ this circuit for our full-adder design.

3.3 MODULE-III

The expression of Module-III is,

$$C_{out} = A \cdot H' + C_{in} \cdot H$$

This expression is the output of 2 to 1 multiplexer with H and H' as the select lines. The most common implementation of the previous expression is using transmission gates (TG). Figure 5(a) shows the circuit for a 2-to-1 multiplexer using TG. The main drawback of this multiplexer is that it cannot provide the required driving capability to drive cascaded adder stages. One solution to this problem is to have an output buffer as shown in Fig. 5 (a). This would incur extra delay and an overhead of four transistors.

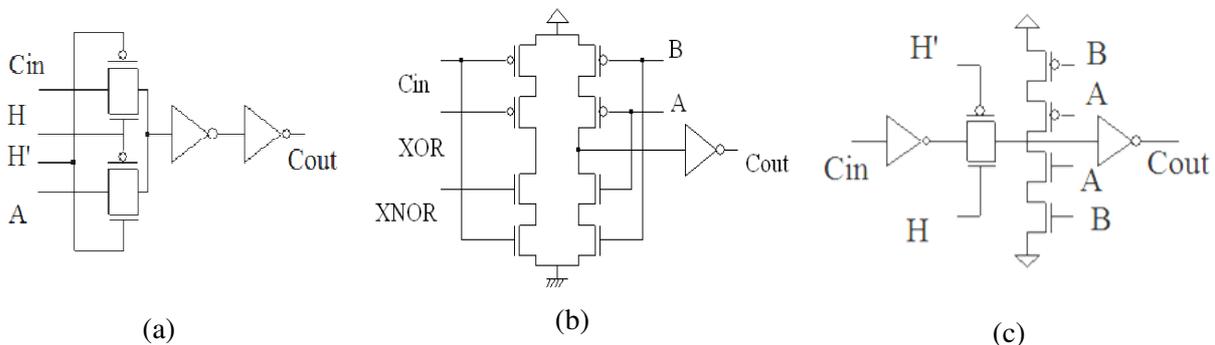


Figure 5: (a) multiplexer using transmission gate (b) Multiplexer based on the static-CMOS logic style (c) Multiplexer based on Hybrid-CMOS logic style

Another possibility is to use the complement of the expression, i.e.,

$$\overline{C_{out}} = \overline{A} \cdot H' + \overline{C_{in}} \cdot H$$

In this case, two inverters will be required to invert the A and C_{in} inputs and one inverter at the output. This will result in unbalanced SUM and C_{out} output switching times and extra delay.

A circuit based on the static-CMOS logic style is presented in [8] [22]. This circuit overcomes the problems of the TG multiplexer design. It uses ten transistors and is shown in Fig. 5 (b). This circuit possesses all the features of static CMOS logic style such as robustness to voltage scaling and good noise margins.

We propose a hybrid design for Module-III. We use the inherently low power consuming TG logic style and the robust static-CMOS logic style to create a new hybrid-CMOS circuit. The proposed circuit is shown in Fig. 5 (c). The new circuit also utilizes ten transistors and possesses the properties of both static-CMOS and TG logic styles. The carry is evaluated using the following logic expression:

$$C_{out} = \overline{(A \oplus B)C_{in}} + \overline{A} \cdot \overline{B}$$

A transmission gate preceded by a static inverter is used to implement $\overline{(A \oplus B)C_{in}}$. H and H' are the complementary gate signals to this TG. When H is at logic 1 and H' is at logic 0, this unit propagates the $\overline{C_{in}}$ signal to the output. Two PMOS pull-up transistors in series with two NMOS pull-down transistors are used to generate $\overline{A} \cdot \overline{B}$. Complementary A and B signal are not required. When A and B are at logic 0 they switch ON both PMOS transistor to generate C_{out} and assign in logic 1. When A and B are at logic 1 they switch ON both NMOS transistors to generate $\overline{C_{out}}$ and assign logic 0. At all other times, this section remains OFF. The static inverter at the output produces the desired C_{out} output. Table-II shows the results of proposed circuit when compared to the circuit in [15].

Table 2: Simulation results for the proposed Module-III at 50-MHz Frequency and 2V_{DD}

	Static-CMOS Multiplexer	Hybrid-CMOS Multiplexer
No. of Transistor	10	10
Power (μW)	1.337	1.437
Delay (ns)	0.1829	0.1224

Due to the additional inverter in the proposed design, it consumes slightly more power as compared to the circuit in [15]. There is redundant switching at the input since the complement of C_{in} is generated even if it is not propagated to the output. This can be avoided by placing the inverter after the TG but this causes a problem as charge can leak through the closed TG and cause a reversal of voltage level at the output. This tradeoff has to be made but this guarantees excellent signal integrity without any glitches.

IV. PROPOSED FULL ADDERS

As mentioned earlier in Section, the centralized full adders, both XOR and XNOR circuits are present (both in module I) that generate the intermediate signals H and H' . These signals are passed on to module II and III along with the carry from the previous stage and the other inputs A and B to produce and SUM and C_{out} (for both 1st and 2nd category). For the 3rd category, we use proposed circuits from module-I and III and one existing circuit from Module-II. The experiment procedure and the selection of our proposed model were very adaptive and symmetrical. Selecting the best circuits from each of the module we have created three combinations for three categories and compared it with other three combinations using traditional TG 2 to 1 multiplexer. The combinations are compared in terms of number of transistor used in circuits, power consumption and delay. Thus we test our proposed adder's performance and found it really encouraging. The three categorized adders are shown in Figure 7, 8 and 9 respectively.

In Module-I, the proposed XOR–XNOR circuit requires non-complementary inputs which will show perfect output. The analysis of driving capability is the same as XOR structure. By cascading a standard inverter to the XNOR circuit, we will have a driving output, and the signal level at the output end will be perfect in all cases. The same property is presented in the XNOR structure. Module-II is a transmission-function implementation of XNOR function to generate the SUM' followed by an inverter to generate SUM. This provides good driving capability to the circuit. Due to the absence of supply rails there are no short circuit currents. The circuit is free from the problem of threshold loss

amongst all circuits that are used for Module-II [6]. Module -II employs the proposed hybrid-CMOS output stage with a static inverter at the output. This circuit has a lower PDP as compared to the other existing designs. The static inverter provides good driving capabilities as the inputs are decoupled from the output. Due to the low PDP of module II and module III, the new adder is expected to have low power consumption.

V. RESULT AND DISCUSSION

Using our proposed models we created three categorized designs for hybrid-CMOS adder. First circuit based on XOR-XOR based full adder which belongs to first category. Here proposed XOR circuit is used as Module-I, II and proposed 2 to 1 multiplexer is used as Module-III. Figure 7(a) and 7(b) respectively represent the hybrid-CMOS adder (XOR-XOR based full adder) and output C_{out} and Sum together. Second circuit based on XNOR-XNOR based full adder of second category where proposed XNOR circuit used as Module-I, II and proposed multiplexer used as Module-III. Figure 8(a) and 8(b) represent consecutively the hybrid-CMOS adder (XNOR-XNOR based full adder) and outputs of C_{out} and Sum together. The final circuit based on Centralized full adder which belongs to our last category. Proposed XOR-XNOR circuit used as Module-I; Proposed transmission-function implementation of XOR and XNOR used as Module-II and proposed multiplexer used as Module-III. Figure 9(a) and 9(b) respectively represents the hybrid-CMOS adder (Centralized full adder) and output of C_{out} and Sum together.

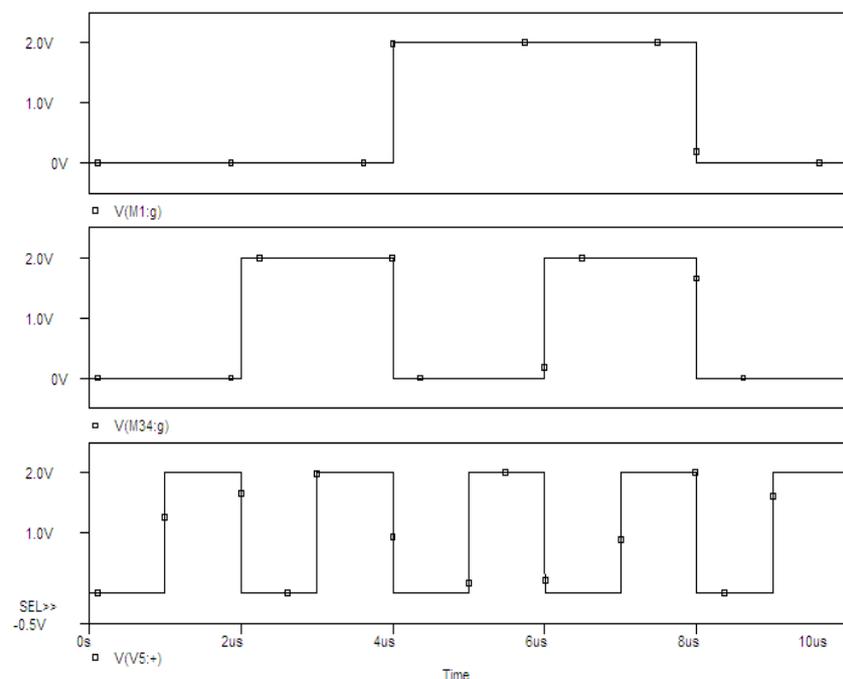


Figure 6: Common input for evaluating all adders

The performance of these three circuits is evaluated based on their transistor numbers, power dissipation and delay. Figure 6 represents the input voltage A , B and C_{in} that used to evaluate all three categorized circuits. Based on our result we finally observed that XOR-XOR based hybrid-CMOS full adder works more efficiently on the basis of all criteria we have mentioned above. Moreover, we have evaluated XOR-XOR based hybrid-CMOS full adder's performances by comparing with all conventional full adders. All simulations are performed using PSPICE, HSPICE and MATLAB.

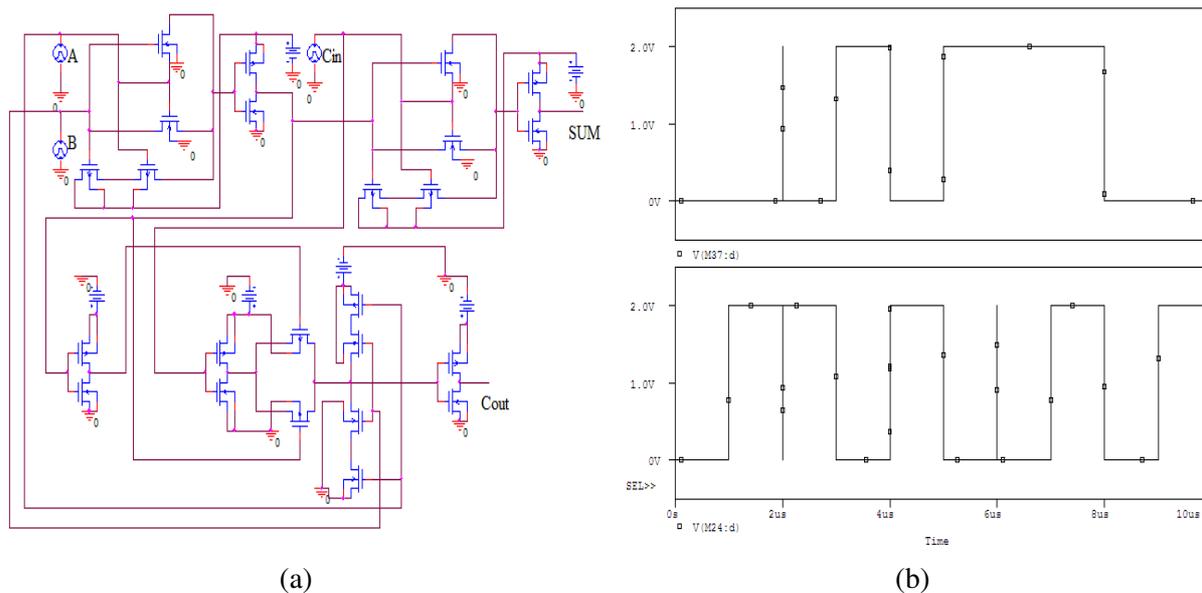


Figure 7: (a) XOR-XOR based Hybrid-CMOS full adder (b) C_{out} and Sum

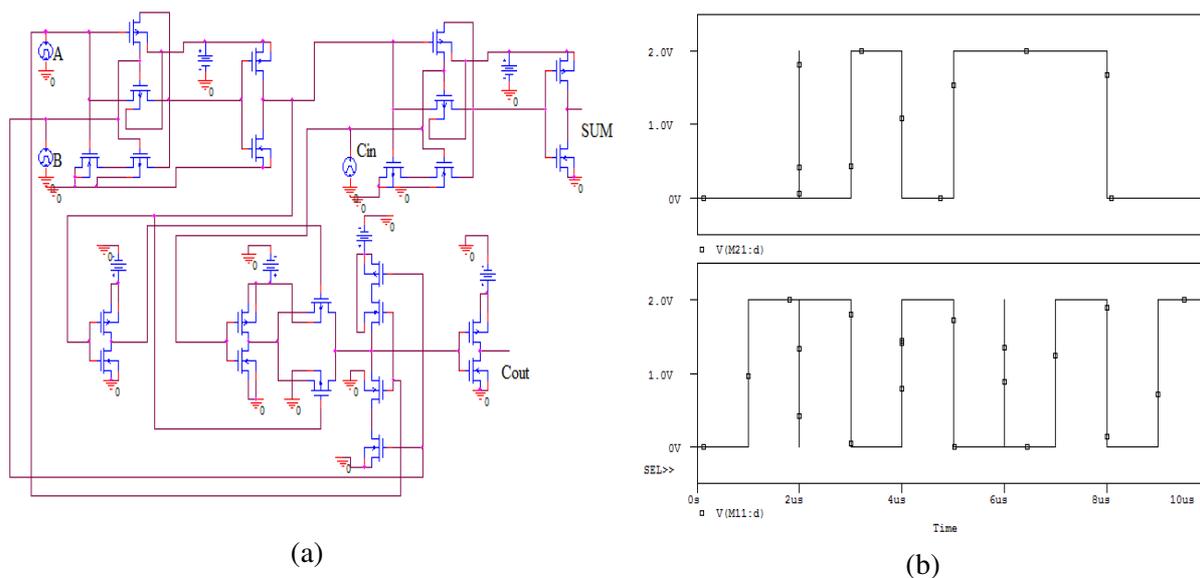


Figure 8: (a) XNOR-XNOR based Hybrid-CMOS full adder (b) C_{out} and Sum

Increase of transistor numbers in chip or digital circuit comes with typical obstacles, even number of transistor may have effect on the overall performance of the circuit. Due to this reason, it was one of our main concerns for designing the full adder without compromising its performance. Three of our proposed designs have twenty four transistors in each and none of them showed any sort of deficiency basis on power dissipation and delay.

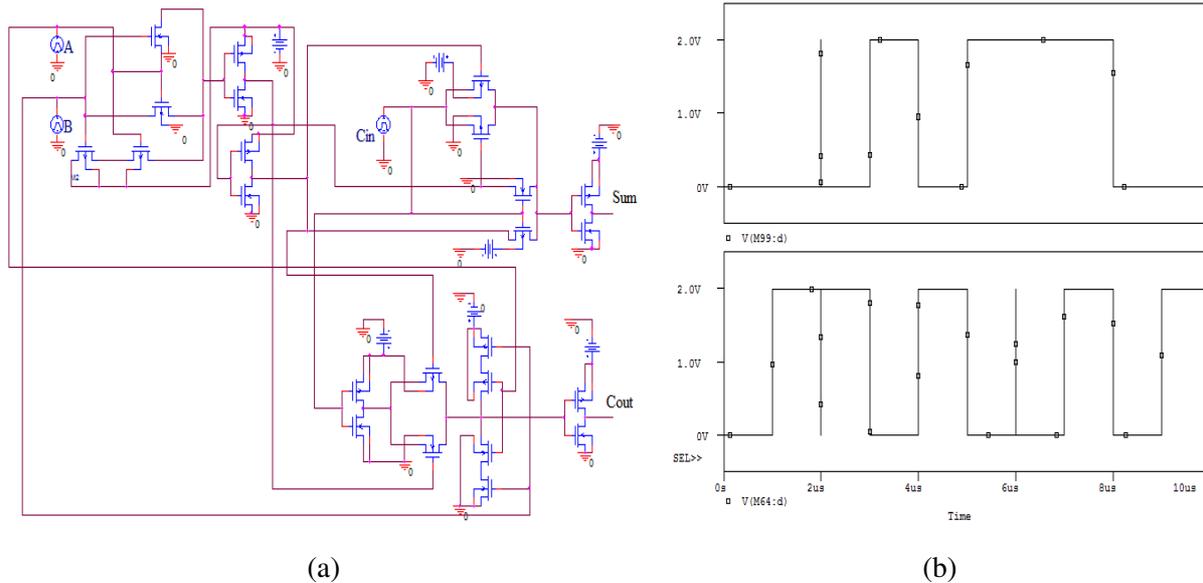


Figure 9: (a) Centralized Hybrid-CMOS full adder (b) C_{out} and Sum

The average power dissipation is evaluated under different supply voltages and different load conditions and is summarized in Figure 10(a) and 10(b) respectively. Among the conventional existing full adders, clearly CPL has the highest power dissipation. The adders TGA and TFA always dissipate less power than others and this can be shown in the graph. Between the two, TGA dissipates lesser power than TFA and the trend continues at low voltages. The degradation in performance of the TFA is higher than the TGA as supply voltage is scaled down. Behind, but closely following the two, comes the static-CMOS full adder. Under varying output load conditions, the adder without driving capability (TGA and TFA) show more degradation as compared to the ones with driving capability (CMOS and CPL). This is as expected since the speed degradation of these designs is highest.

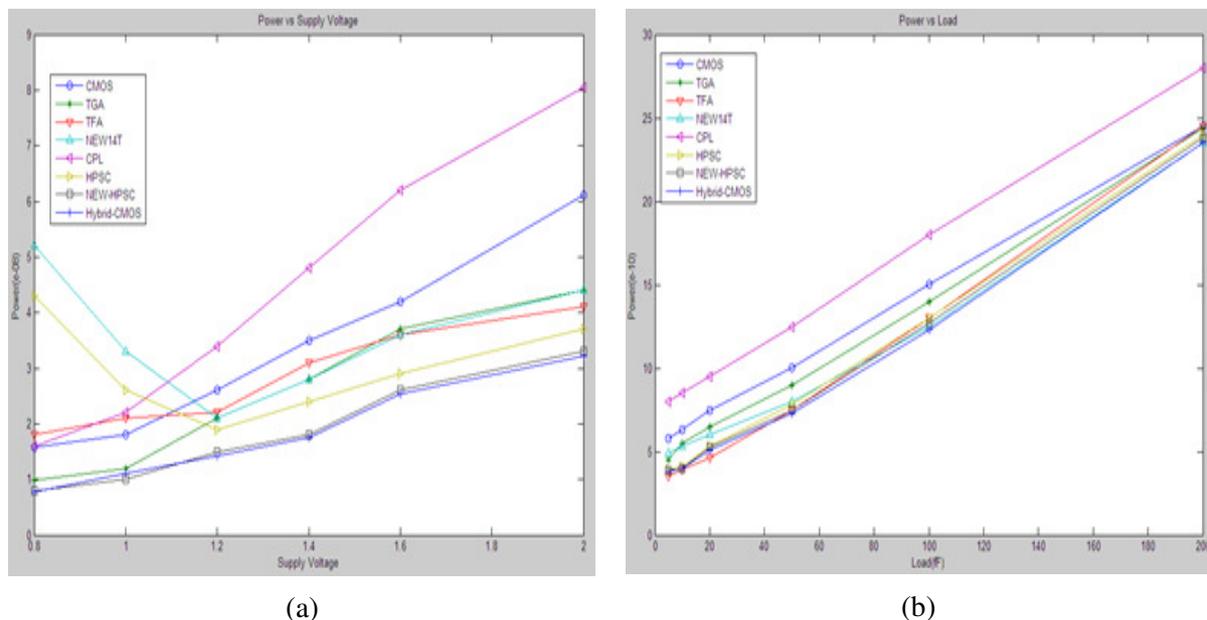


Figure 10: (a) Power vs. Supply Voltage for different full adders (b) Power vs. Load for different full adders

The static-CMOS full adder shows the best performance amongst the conventional full adders under varying load. Among the nonconventional or hybrid-CMOS full adders, the proposed hybrid-CMOS full adder and NEW-HPSC adder have the least power dissipation. The proposed full adder consumes 2% lesser power as compared to the NEW-HPSC adder at $2V_{DD}$ but when the supply voltage is scaled

down, NEW-HPSC adder consumes slightly lesser power. The power dissipation of the proposed adder is roughly 25% less than the next lowest power consuming adder (TGA). With increasing output load, the power dissipation of these adders remains the least as compared to all the considered full adders.

Figure 11(a) and 11(b) respectively represent the delays of full adders at $2V_{DD}$ and load (5.6-200fF). For easy comparison, Table III shows the delay values. From the observation we have learnt that amongst the existing conventional full adders, TGA and TFA (the adders without driving capability) have the smallest delays. TFA has slightly lower delay than TGA at higher supply voltages but the trend reverses at lower supply voltages. The static-CMOS full adder and CPL full adder follow the TGA and TFA adders, CMOS steadily remaining ahead of the CPL adder at each supply voltage. For varying load conditions, TGA and TFA have the low delay at small loads, but the speed degrades significantly at higher loads. Among the existing full adders, CMOS shows the least speed degradation followed by the CPL full adder. This shows that under heavy load conditions, adders with driving capability perform better than those without it (TGA and TFA). Due to these reasons, we compared the proposed hybrid-CMOS adders to the conventional CMOS adders.

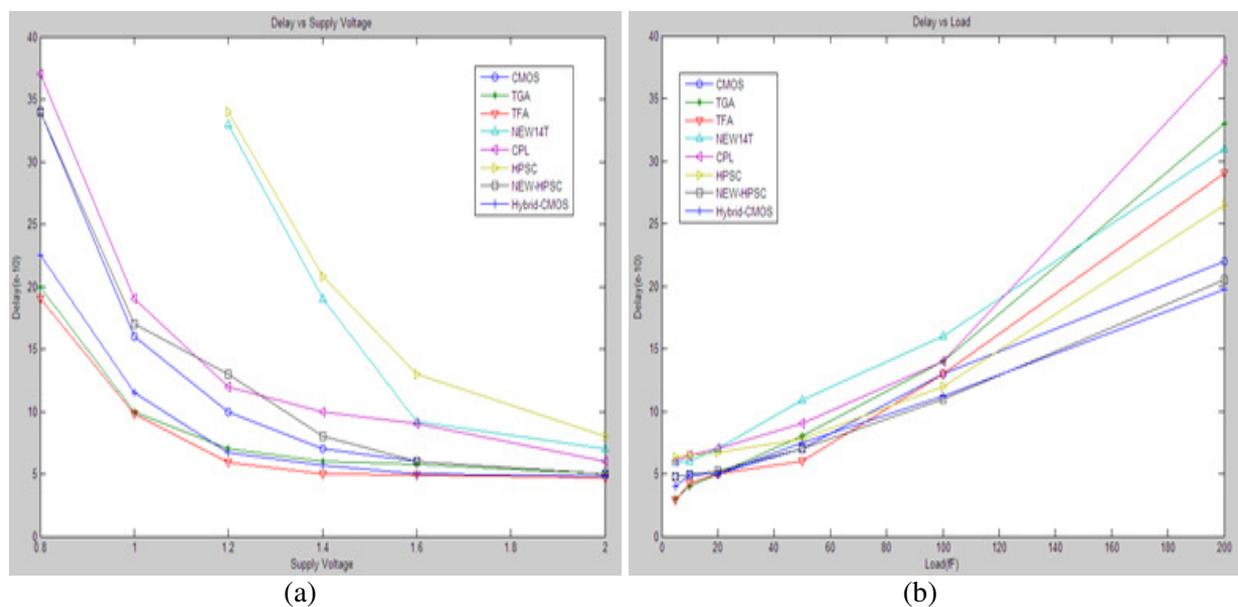


Figure 11:

(a) Delay vs. Supply Voltage for different full adders (b) Delay vs. Load for different full adders

Among the nonconventional or hybrid-CMOS full adders, the proposed hybrid-CMOS full adder shows minimum delay at all supply voltages when compared to the CMOS, HPSC, NEW14T, and NEW-HPSC full adders. At $2V_{DD}$, the proposed adder is 30%, 55%, 88%, and 29% faster than CMOS, HPSC, NEW14T and NEW-HPSC full adders, respectively. At lower supply voltages, the proposed full adder is the fastest. The delay of the proposed hybrid-CMOS adder is slightly higher than TGA and TFA but with increasing load, it displays minimum speed degradation. Overall, when compared to all adders, the proposed adder has minimum speed degradation with varying load.

VI. FUTURE WORK

In recent Years several variants of different logic styles have been proposed to implement 1 bit adder cells [22] [24]. These papers have also investigated different approaches realizing adders using CMOS technology; each has its own pros and cons. By scaling the supply voltage appears to be the most well known means to reduce power consumption. However, lowering supply voltage increases circuit delay and degrades the drivability of cells designed with certain logic style. One of the most important obstacles decreasing supply voltages is the large transistor count and V_{th} loss problem.

In this paper, we used Hybrid CMOS logic style to design our proposed circuit. This type of logic design provides designer flexibility to work on CMOS area to overall performance of a circuit. Different modules give us the opportunity to create new application basis on the requirements. By optimizing the area of CMOS in different modules more efficient designs can be found [19] [23]. But decreasing area size of different modules brings obstacles that can create a negative impact on the overall circuit's performance. So not compromising the negative impact, designer may work on the size and number of the transistors as minimal level as possible. Moreover, a slight improvement in the area of power dissipation, delay, PDP can create huge impact on the overall performance and that can be one of the main concerns for future work. Most of the conventional adders showed lower power consumption at low voltage and higher power consumption at high voltage but our proposed model overcome that obstacle and showed lower power consumption in every kind of input voltage. As different application can be generated using this different modules, designers should take a good look at the power consumption at different input voltage. Another important concern for designing circuits is delay. Decrease of delay and low input voltage might have an impact on the speed of overall circuits. Due to this reason delay is another area where designer can work in future.

VII. CONCLUSION

Hybrid CMOS design style become popular because it provides designer more freedom to work on the performance of single CMOS design to overall circuit. Based upon the application designers can choose required modules as well as efficient circuit from different modules for the implementation. Even by optimizing the transistor sizes of the modules it is possible to reduce the delay of all circuits without significantly increasing the power consumption, and transistor sizes can be set to achieve minimum PDP. Using the adder categorization and hybrid CMOS design style, many full adders can be conceived. As an example, a novel full adder designed using hybrid CMOS design style is presented in this paper that evaluated low power dissipation and delay. The proposed hybrid-CMOS full adder has better performance than most of the conventional full-adder cells owing to the novels design modules proposed in this paper. It performs well with supply voltage scaling and under different load conditions. We recommend the use of hybrid-CMOS design style for the design of high performance circuits.

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