VERIFICATION ANALYSIS OF AHB-LITE PROTOCOL WITH COVERAGE

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ABSTRACT

The SoC design faces a gap between the production capabilities and time to market pressures. The design space, grows with the improvements in the production capabilities in terms of amount of time to design a system that utilizes those capabilities. On the other hand shorter product life cycles are forcing an aggressive reduction of the time-to-market. Fast simulation capabilities are required for coping with the immense design space that is to be explored; these are especially needed during early stages of the design. This need has pushed the development of transaction level models, which are abstract models that execute dramatically faster than synthesizable models. The pressure for fast executing models extends especially to the frequently used and reused communication libraries. The presents paper describes the system level modelling of the Advanced High-performance Bus Lite (AHB-Lite) subset of AHB which part of the Advanced Microprocessor Bus Architecture (AMBA). The work on AHB-Lite slave model, at different test cases, describing their simulation speed. Accuracy is built on the rich semantic support of a standard language SystemVerilog on the relevant simulator Riviera has been highlighted.

KEYWORDS: *AMBA(Advanced Microcontroller Bus Architecture), AHB-Lite(Advanced High performance Bus-Lite), SystemVerilog, SoC(System on chip), Verification intellectual property (VIP).*

I. INTRODUCTION

The bus protocol used by the CPU is an important aspect of co-verification since this is the main communication between the CPU, memory, and other custom hardware. The design of embedded systems in general and a SoC in special will be done under functional and environmental constraints. Since the designed system will run under a well-specified operating environment, the strict functional requirements can be concretely defined. The environment restrictions on the other hand are more diverse: e.g. minimizing the cost, footprint, or power consumption. Due to the flexibility of a SoC design, ARM processors use different bus protocols depending on when the core was designed for achieving the set goals, involves analyzing a multi-dimensional design space. The degrees of freedom stem from the process element types and characteristics, their allocation, the mapping of functional elements to the process elements, their interconnection with busses and their scheduling. The enormous complexity of these protocol results from tackling high-performance requirements.Protocol control can be distributed, and there may be non-atomicity or speculation.

AHB-Lite systems based around the Cortex-M™ processors ARM delivers the DMA-230 "micro" DMA controller [13]. ARM delivers DMA controllers for both high-end, high-performance AXI systems based on the Cortex-A™ and Cortex-R™ families and cost-efficient AHB systems built around Cortex-M™ and ARM9 processors.

The CoreLink Interconnect family includes the following products for AMBA protocols:

- Network Interconnect (NIC-301) for AMBA 3 systems including support for AXI, AHB and APB
- Advanced Quality of Service (QoS-301) option for NIC-301

The third generation of AMBA defines the targeted at high performance, high clock frequency system designs and includes features which make it very suitable for high speed sub-micrometer interconnect. In the present paper the some discussion is made on the family of AMBA and a small introduction on SystemVerilog language which used during VIP. And also the briefly described the AHB-Lite Protocol. Further verification intellectual property (VIP) of slave of the AHB-Lite protocol with different test cases is shown.

II. AMBA PROTOCOLS

Figure 1. shows the different protocols performances from the time of initialization[9].

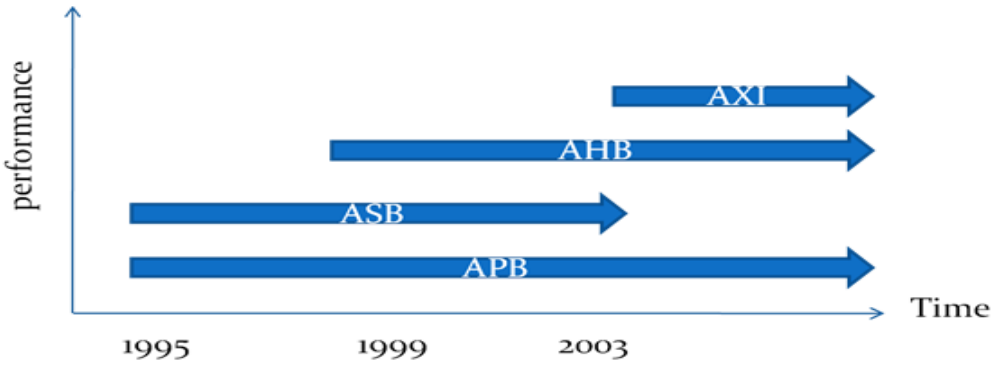

Figure 1. Protocols of AMBA[9]

- APB (Advanced Peripheral Bus) mainly used as an ancillary or general purpose register based peripherals such as timers, interrupt controllers, UARTs, I/O ports, etc. It is connected to the system bus via a bridge, helps reduce system power consumption. It is also easy to interface to, with little logic involved and few corner- cases to validate.
- AHB (Advanced High Performance Bus) is for high performance, high clock frequency system modules with suitable for medium complexity and performance connectivity solutions. It supports multiple masters.
- AHB-Lite is the subset of the full AHB specification which intended for use where only a single bus master is used and provides high-bandwidth operation.

III. SYSTEMVERILOG

SystemVerilog is a Hardware Description and Verification Language based on Verilog. Although it has some features to assist with design, the thrust of the language is in verification of electronic designs. The bulk of the verification functionality is based on the Open Vera language donated by Synopsys[12]. SystemVerilog has just become IEEE standard P1800-2005.SystemVerilog is an extension of Verilog-2001; all features of that language are available in SystemVerilog i.e Verilog HDL, VHDL, C, C++.

IV. AHB-LITE PROTOCOL SYSTEM

AMBA AHB-Lite protocol addresses the requirements of high-performance synthesizable designs. It is a bus interface that supports a single bus master and provides high-bandwidth operation.
AHB-Lite implements the features required for high-performance, high clock frequency systems including: [1]

- burst transfers
- single-clock edge operation
- non-tristate implementation

- Wide data bus configurations, 64, 128, 256, 512, and 1024 bits.

The most common AHB-Lite slaves are internal memory devices, external memory interfaces, and high bandwidth peripherals. Although low-bandwidth peripherals can be included as AHB-Lite slaves, for system performance reasons they typically reside on the AMBA Advanced Peripheral Bus (APB). Bridging between this higher level of bus and APB is done using a AHB-Lite slave, known as an APB bridge.

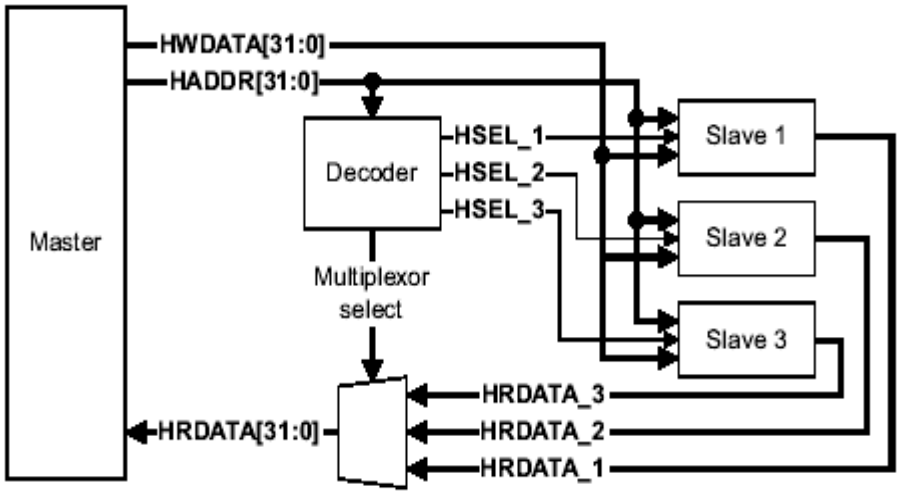

Figure 2. AHB-Lite block diagram

Figure 2. shows a single master AHB-Lite system design with one AHB-Lite master and three AHB-Lite slaves. The bus interconnect logic consists of one address decoder and a slave-to-master multiplexor. The decoder monitors the address from the master so that the appropriate slave is selected and the multiplexor routes the corresponding slave output data back to the master.The main component types of an AHB-Lite system are described in:

- Master
- Slave
- Decoder
- Multiplexor

4.1 Operations of AHB-Lite

The master starts a transfer by driving the address and control signals. These signals provide information about the address, direction, width of the transfer, and indicate if the transfer forms part of a burst. Transfers can be:[11]

Table 1. Transfer type values

Cycle Type	Description	HTRANS[1:0]
IDLE	No bus activity	00
BUSY	Master inserting wait states	01
NON-SEQUENTIAL	Trasnsfer with address not related to the previous transfer	10
SEQUENTIAL	Trasnsfer with address related to the previous transfer	11

The write data bus moves data from the master to a slave, and the read data bus moves data from a slave to the master. Every transfer consists of:[2]

- **Address phase** one address and control cycle
- **Data phase** one or more cycles for the data.

A slave cannot request that the address phase is extended and therefore all slaves must be capable of sampling the address during this time. However, a slave can request that the master extends the data phase by using **HREADY**. This signal when LOW, causes wait states to be inserted into the transfer and enables the slave to have extra time to provide or sample data.
The slave uses **HRESP** to indicate the success or failure of a transfer.

Table 2. Response type values

Description	HRESP[1:0]
Completed Successfully	00
Error occurred	01
Master should retry	10
Perform Split Protocol	11

V. SPECIFICATION DIFFERENT FROM AHB

The AHB-Lite specification differs from the full AHB specification in the following ways[2]:

- Only one master. There is only one source of address, control, and write data, so no Master-to-Slave multiplexor is required.
- No arbiter. None of the signals associated with the arbiter are used.
- Master has no **HBUSREQ** output. If such an output exists on a master, it is left unconnected.
- Master has no **HGRANT** input. If such an input exists on a master, it is tied HIGH.
- Slaves must not produce either a Split or Retry response.
- The AHB-Lite lock signal is the same as **HMASTLOCK** and it has the same timing as the address bus and other control signals. If a master has an **HLOCK** output, it can be retimed to generate **HMASTLOCK**
- The AHB-Lite lock signal must remain stable throughout a burst of transfers, in the same way that other control signals must remain constant throughout a burst.

VI. COMPATIBILITY

Table 3 shows how masters and slaves designed for use in either full AHB or AHB-Lite can be used interchangeably in different systems.

Table 3

Component	Full AHB system	AHB-Lite system
Full AHB master	✓	✓
AHB-Lite master	Use standard AHB master wrapper	✓
AHB slave (no Split/Retry)	✓	✓
AHB slave with Split/Retry	✓	Use standard AHB master wrapper

VII. SIMULATION RESULTS OF DESIGN OF AHB-LITE PROTOCOL

Figure 4. show single write and read operation which is taking place in AHB-Lite bus protocol. In the above simulated result the has been written by the signal Hw_data at the address Haddr when Hwrite signal is active high. The same data is been read by the system by the signal Hr_data at same address when the Hwrite signal is low.

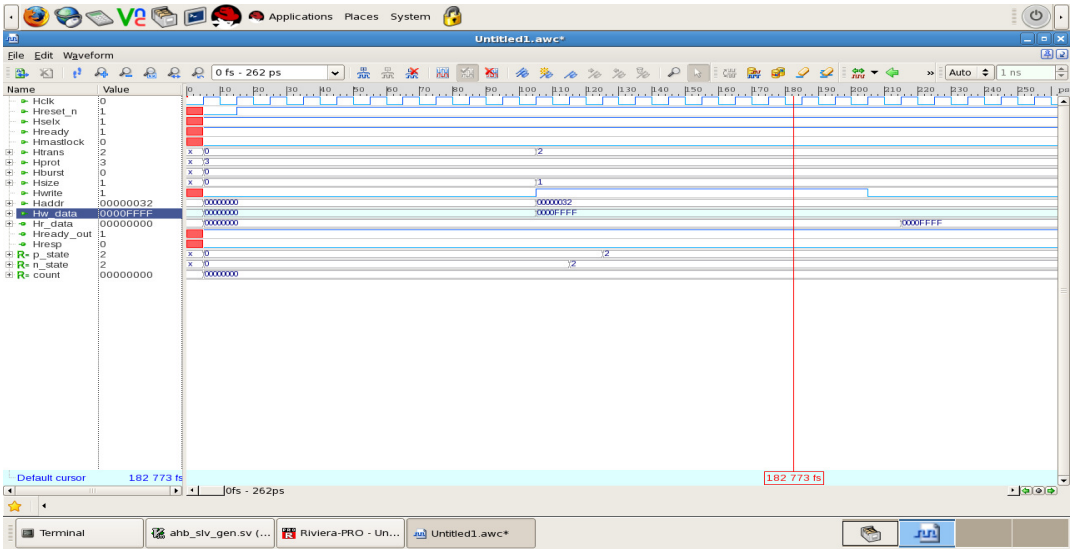

Figure 4. Single write and read operation

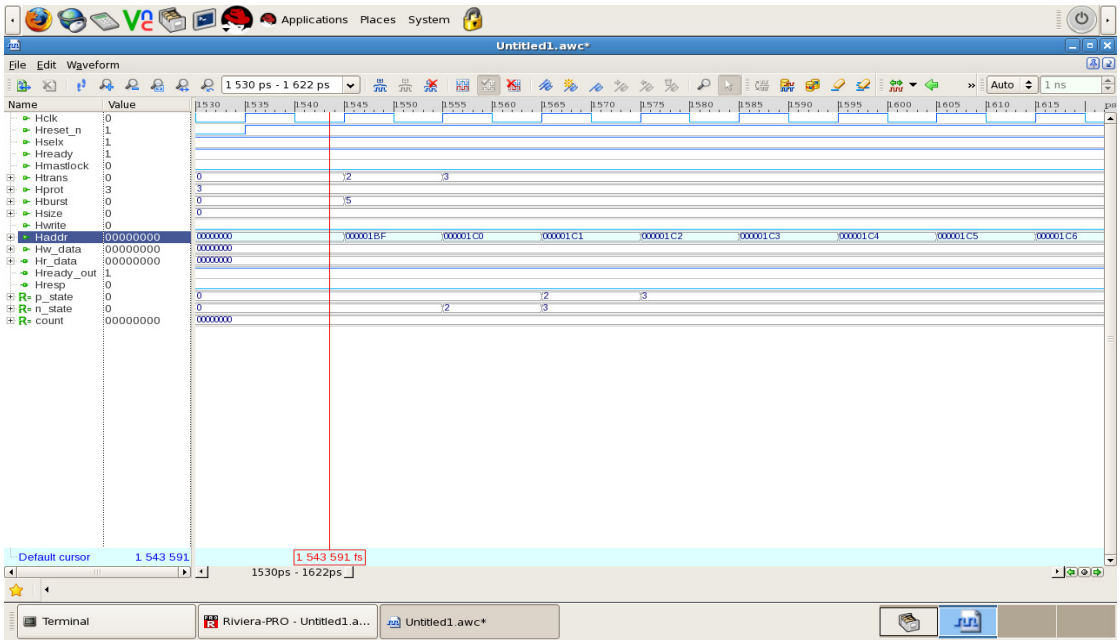

Figure 5. Read operation with unwritten

In Figure 5. Read operation with unwritten location is taking place i.e it is said to randomize operation. It is shows that the address is being added but Hw_data is 0000000 because this is taking place after the reset.

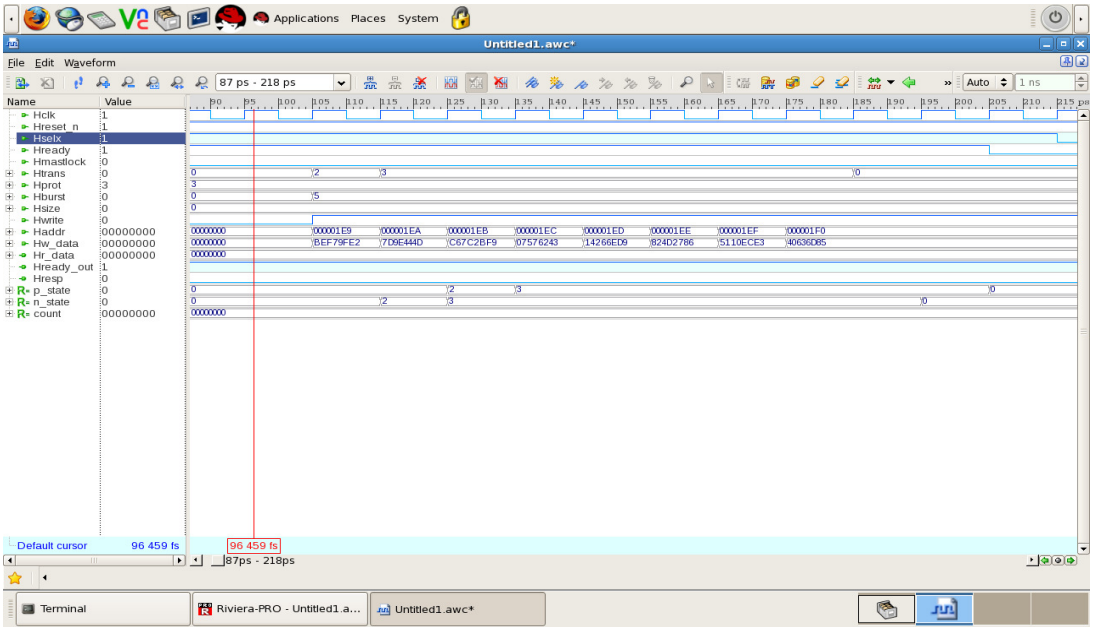

Figure 6. write_inc_8 operation

In Figure 6. it shown that inc_8 is taking place in Haddr of write. In Figure 7 inc_4 is taking place of write and read.

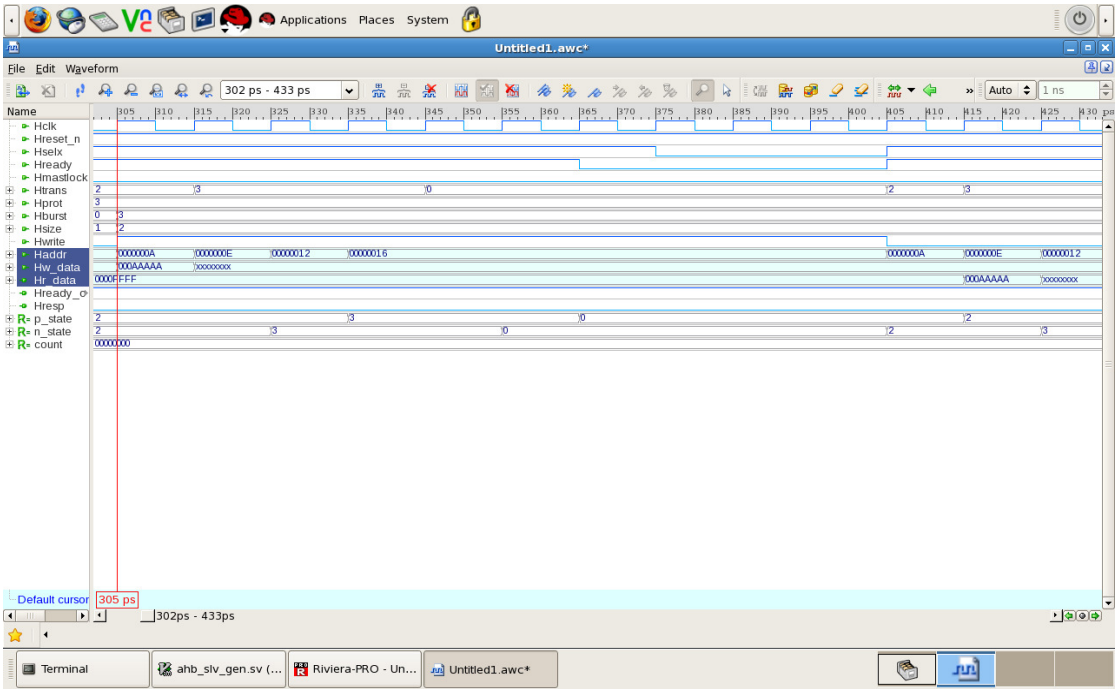

Figure 7. Write and read with inc_4

VIII. COVERAGE ANALYSIS

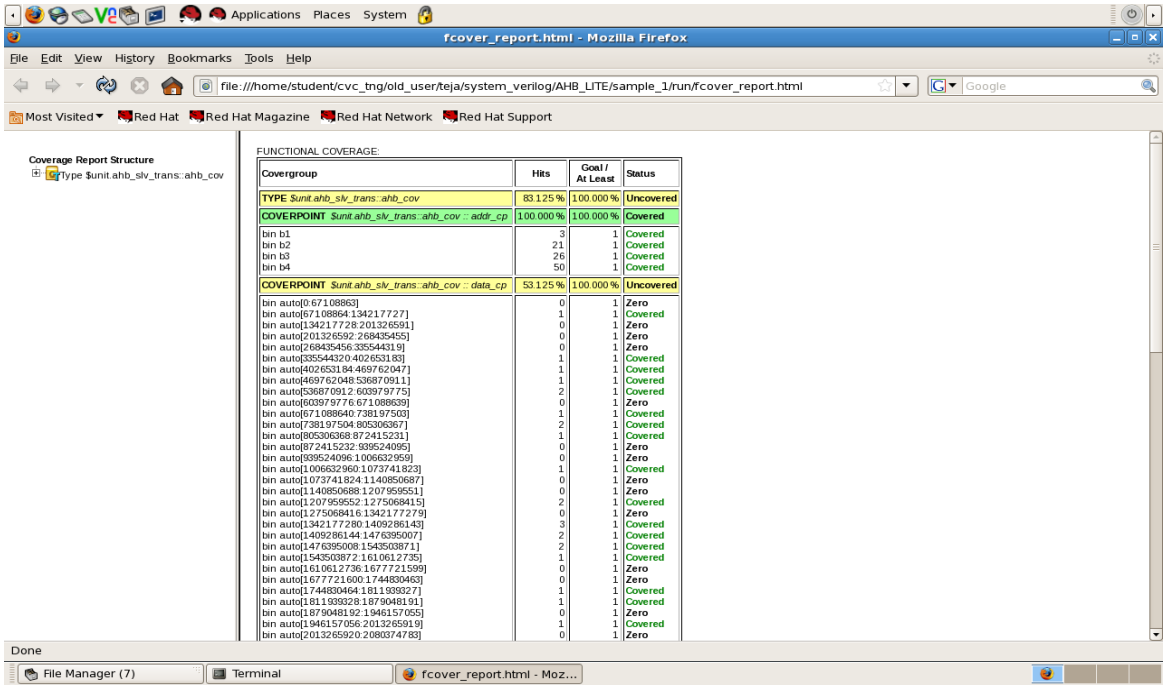

Figure 8. Coverage Analysis

The Coverage Report gives the details of the functional coverage when complete Analysis was done for the AHB-Lite and coverage report was generated as shown in Figure 8. It is found that the coverage is 100%.

IX. CONCLUSION

In the paper a general definition for AHB-LITE protocol which has high performance represents a significant advance in the capabilities of the ARM AMBA™ bus on-chip interconnect strategy, by providing a solution that reduces latencies and increases the bus bandwidth. AHB-Lite fully compatible with the current AHB specification. AHB-Lite increases the choice of architectures available to the AMBA bus-based designer, and is supported by a comprehensive range of products from ARM.

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