CALCULATION OF POWER CONSUMPTION IN 7 TRANSISTOR SRAM CELL USING CADENCE TOOL

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ABSTRACT

In this paper a new 7T SRAM is proposed. CMOS SRAM Cell is very less power consuming and have very less read and write time. In proposed SRAM an additional write bit line balancing circuitry is added in 6T SRAM for power reduction. A seven Transistor (7T) cell at 45 nm Technology is proposed to accomplish improvement in stability, power dissipation and performance compared with previous designs. Simulation result of proposed design using CADENCE TOOL shows the reduction in total average power consumption.

KEYWORDS:- Conventional SRAM, Low Power, Power Consumption.

I. INTRODUCTION

Advances in CMOS technology have made it possible to design chips for high integration density, fast performance, and low power consumption. To achieve these objectives, the feature size of CMOS devices has been dramatically scaled to very small features and dimensions [1]. Over the last few years, devices at 180nm have been manufactured; the deep sub-micron/nano range of 45nm is foreseen to be reached in the very near future.

Technology scaling results in a significant increase in leakage current of CMOS devices. As the integration density of transistors increases, leakage power has become a major concern in today's processors and SoC designs. Considerable attention has been paid to the design of low power and high-performance SRAMs as they are critical components in both handheld devices and high performance processors. Different design remedies can be undertaken; a decrease in supply voltage reduces quadratically the dynamic power consumption. However, with an aggressive scaling in technology as predicted by the Technology Roadmap, substantial problems have already been encountered when the conventional six transistors (6T) SRAM cell configuration is utilized at an ultra-low power supply; this cell shows poor stability at very small feature sizes[2]. A seven transistors (7T) SRAM cell configuration is proposed in this paper, which is amenable to small feature sizes encountered in the deep sub-micron/nano CMOS ranges. The schematic and Layout of proposed 7T SRAM Cell is shown in Figure 1.1 and figure 1.2 respectively.

The objective of this paper is to investigate the transistor sizing of the 7T SRAM cell for optimum power. An innovative precharging and bitline balancing scheme for writing operation of the 7T SRAM cell is also proposed for maximum standby power savings in an SRAM array[3]. CADENCE simulation results confirm that the proposed scheme achieves 45% of power savings compared to the conventional SRAM cell array based on the 6T configuration. The paper starts with introducing the proposed 7T cell and the design method used to find the optimal transistor sizing for the proposed SRAM cell[4]. Finally, the impact of process variation on the cell's stability and power consumption is analyzed to show that the 7T SRAM cell has a very good tolerance in the presence of process variations [5].

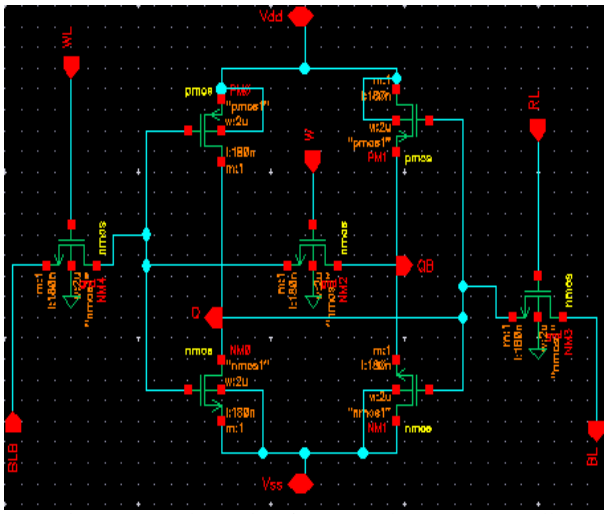

Figure 1.1 Schematic of Proposed 7T SRAM Cell

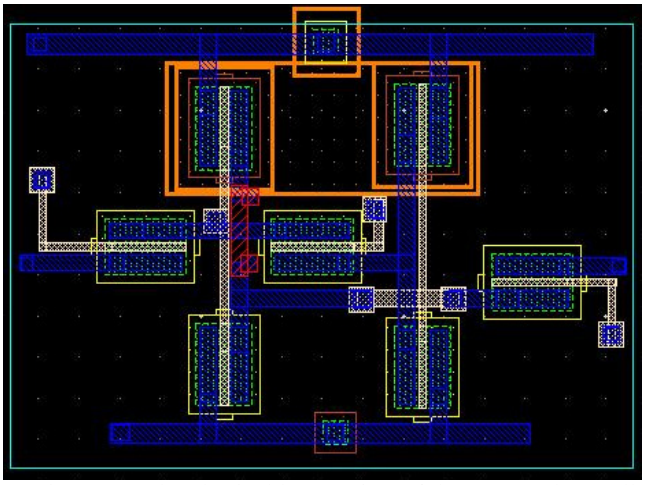
Figure 1.2 The physical layout view of the proposed 7T cell

II. LEAKAGE CURRENT OF 7T SRAM CELL

Gate length scaling increases device leakage exponentially across technology generations. Leakage current is the main source of standby power for a SRAM cell. In nano-scale CMOS devices, the major components of leakage current are the sub-threshold leakage, the gate direct tunneling leakage, and the reverse biased band-to- band tunneling junction leakage. The sub-threshold leakage, which is defined as a weak inversion conduction current of the CMOS transistor when $V_{gs} < V_{th}$, represents a significant leakage current component in the off-state.
The equation for the sub-threshold leakage current is given by (1)

$$Isub = I_o e^{(Vgs-Vth)/\eta kT/q} (1-e^{(-Vds)/kT/q}) \quad - (1)$$

Where,

$$Io = \mu_o C_o x (W/L)(kT/q)^2 (1-e^{1.8}) \quad - (2)$$

W and L are the transistor's channel width and length, μ0 is the low field mobility, *Cox* is the gate oxide capacitance, *k* is Boltzmann's constant, and *q* is the electronic charge.

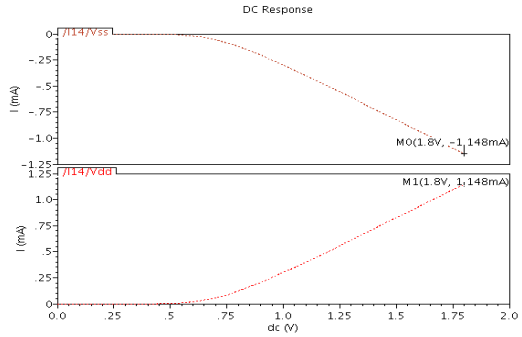

Figure 2 Leakage current of Proposed 7T SRAM

III. WRITE BITLINE BALANCING CIRCUITRY FOR POWER REDUCTION

The proposed write concept depends on cutting off the feedback connection between the two inverters, invl and inv2, before the write operation. The feedback connection and disconnection are performed through an extra NMOS transistor N5, as shown in Figure 1, and the cell only depends on BL_bar to perform a write operation [6]. The write operation starts by turning N5 off to cut off the feedback connection. BL_bar carries complement of the input data, N3 is turned on, and N4 is kept off. The SRAM cell looks like two cascaded inverters, inv2 followed by invl. BL_bar transfers the complement of input data to Q2 which drives inv2, P2 and N2, to develop Q, cell data, which drives invl and develops Qbar. Both BL and BL_bar are precharged "high" before and after each read/write operation [9]. When writing "0", BL_bar is kept "high" with negligible write power consumption.
To write "1", BL_bar is discharged to "0" with comparable power consumption to a conventional write. The write circuit does not discharge one of the bit lines for every write operation and the activity factor of discharging BL_bar is less than "1".
The proposed write bitline balancing circuitry, output waveform and power consumption graph is shown in the Figure 3.1, Figure 3.2 and Figure 3.3 respectively.

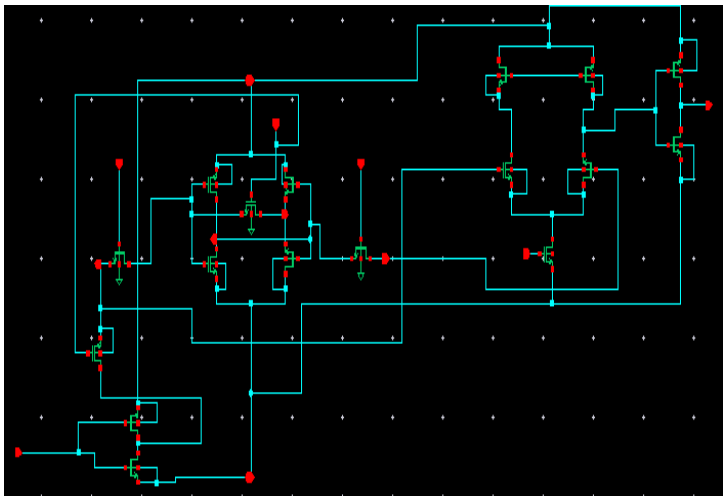

Figure 3.1 Proposed write bit line balancing circuitry

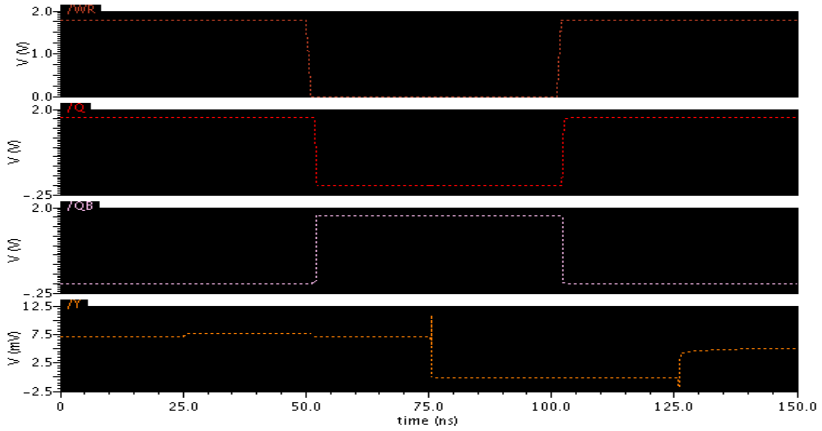

Figure 3.2 Output Waveform of 7T SRAM cell

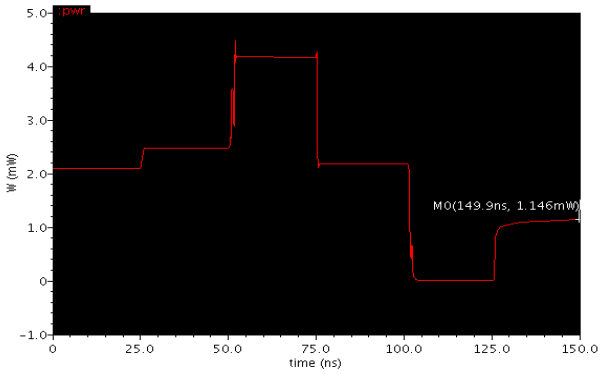

Figure 3.3 Power consumption of Proposed 7T SRAM.

IV. SIMULATION RESULTS

In this paper, a novel write methodology is proposed which depends on cutting off the feedback connection between the two back-to-back inverters in the SRAM cell and requires a 7T SRAM cell. The proposed technique reduces the number of times to charge and discharge the large bit lines capacitance to reduce the write power consumption. Simulation results show that the write circuitry scheme for the proposed 7T SRAM cell based array achieves a 45% reduction in power consumption at a 1.8V power supply voltage and typical process corner compared with a conventional 6T SRAM cell based array. The Figure 4.1 & Figure 4.2 also shows the waveform of leakage current and power consumption. The Results of leakage current and power consumption using Cadence Tool is given in TABLE I.

Table I: Simulation results of the 7T SRAM cell

Process Technology	45 nm
Power Supply Voltage	1.8 V
Precharge Voltage	1 V
Leakage Current	1.148 mA
Power Consumption	1.146 mW

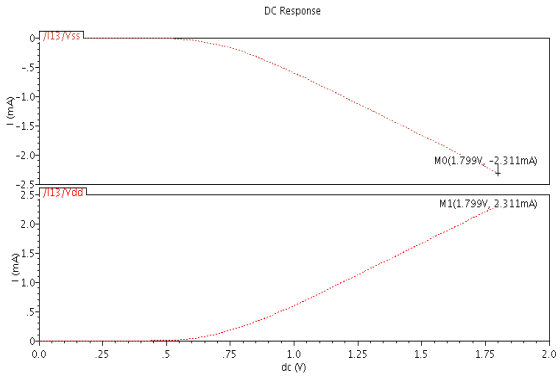

Figure 4.1 Leakage current of 6T SRAM

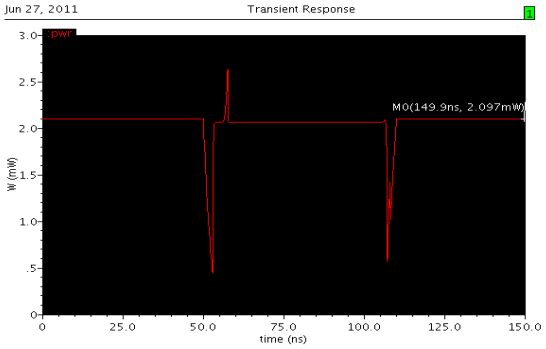

Figure 4.2 Power consumption of Proposed 7T SRAM

V. CONCLUSION

In this paper, a novel write methodology is proposed which depends on cutting off the feedback connection between the two back-to-back inverters in the SRAM cell and requires a 7T SRAM cell. The proposed technique reduces the number of times to charge and discharge the large bit lines capacitance to reduce the write power consumption. The simulation results using CADENCE TOOL show that much better tolerance to process variation is achieved using the proposed 7T SRAM cell.

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