ANALOG INTEGRATED CIRCUIT DESIGN AND TESTING USING THE FIELD PROGRAMMABLE ANALOG ARRAY TECHNOLOGY

Mouna Karmani, Chiraz Khedhiri, Belgacem Hamdi
Electronics and Microelectronics Laboratory, Monastir, Tunisia.

ABSTRACT

Due to their reliability, performance and rapid prototyping, programmable logic devices overcome the use of ASICs in the digital system design. However, the similar solution for analog signals was not so easy to find. But the evolutionary trend in Very Large Scale Integrated (VLSI) circuits technologies fuelled by fierce industrial competition to reduce integrated circuits (ICs) cost and time to market has led to design the Field-Programmable Analog Array (FPAA) which is the analog equivalent of the Field Programmable Gate Array (FPGA). In fact, the use of FPAAs reduces the complexity of analog design, decreases the time to market and allows products to be easily updated and improved outside the manufacturing environment. Thus, the reconfigurable feature of FPAAs enables real time updating of analog functions within the system using the Configurable Analog Blocks (CABs) system and appropriate software. In this paper, an interesting analog phase shift detection circuit based on FPAA architecture is presented. In fact, the phase shift detection circuit will distinguish a faulty circuit from a faulty-free one by controlling the phase shift between their corresponding outputs. The system is practically designed and simulated by using the AN221E04 board which is an Anadigm product. The Circuit validation was carried out using the AnadigmDesigner®2 software.

KEYWORDS

Analog integrated circuits, design, FPAA, test, phase shift detection circuit

I. INTRODUCTION

With the continuous increase of integration densities and complexities, the tedious and hard process of designing and implementing analog integrated circuits could often take weeks or even months [1]. Consequently, analog and mixed semiconductor designers have begun to move design methodologies to higher levels of abstraction in order to reduce the analog design complexity [2]. Also, the use of programmable circuits further facilitates the task of designing complex analog ICs and offers other advantages. In fact the use of field programmable devices decreases the time to market and allows the possibility of updating the considered circuit design outside of the manufacturing environment. Thus, field programmable devices can be programmed and reprogrammed not only to update a design but to offer the possibility of error correction [1-2].

"In the digital domain, programmable logic devices (PLDs) have a large impact on the development of custom digital chips by enabling the designer to try custom designs on easily-reconfigurable hardware. Since their conception in the late 1960s, PLDs have evolved into today's high-density FPGAs. In addition, most of the digital processing is currently done through FPGA circuits" [1]. However, reconfigurable analog hardware has been progressing much more slowly. In fact, the field programmable analog array technology appeared in 1980's [3-4]. The commercial FPAA did not reach the market until 1996 [1]. And the Anadigm FPAA technology was made commercially available just in 2000 [5].

An FPAA is an integrated circuit built in Complementary Metal Oxide Semiconductor (CMOS) technology that can be programmed and reprogrammed to perform a large set of analog circuit functions. Using the AnadigmDesigner®2 software and its library of analog circuit functions, a designer can easily and rapidly design a circuit that would previously have taken months to design

and test. The circuit configuration files are downloaded into the FPAA from a PC or system controller or from an attached EEPROM [6].

Modern FPAAs like Anadigm products can contain analog to digital converters that facilitate the interfacing of analog systems with other digital circuits like DSP, FPGAs and microcontrollers [1]. FPAAs are used for research and custom analog signal processing. In fact, this technology enables the real-time software control of analog system peripherals. It is also used in intelligent sensors implementation, adaptive filtering, self-calibrating systems and ultra-low frequency analog signal conditioning [6].

The paper is organised as follows. Section 2 introduces the FPAA architecture based on switched capacitor technology. We then present The AN221E04 Anadigm board in section 3. The testing importance in CMOS analog integrated circuits and the phase shifte defenition are discussed in section 4. The proposed test methodology using the FPAA technology is presented in section 6. The simulation results are given in section 6. Finally, we conclude in section 7.

II. THE FPAA ARCHITECTURE USING THE SWITCHED CAPACITOR TECHNOLOGY

"FPAA devices typically contain a small number of CABs (Configurable Analog Blocks). The resources of each CAB vary widely between commercial and research devices" [4-7]. In this paper, we focus on Anadigm's FPAA family based on switched capacitor technology. This technology is the technique by which an equivalent resistance can be implemented by alternatively switching the inputs of a capacitor. In fact, an effective resistance can be implemented using switched capacitors. Its value depends on the capacity but changes according to the sampling frequency **(f =1/T)**. Fig. 1 illustrates how switched capacitors are configured as resistors [5-6].

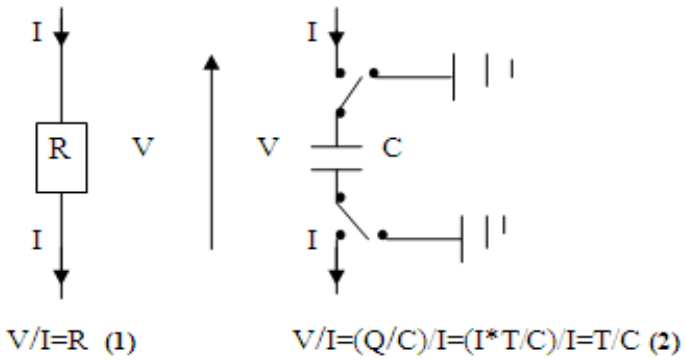

Figure 1: Switched capacitor configured as a resistor

The most important element in FPAA is the Configurable Analogue Block (CAB), which includes an operational amplifier and manipulates a network of switched capacitor technology. In the next section we present the Anadigm® AN221E04 FPAA device which is based on switched capacitor technology [6].

III. THE AN221E04 ARCHITECTURE

The AN221E04 device consists of a 2x2 matrix of fully Configurable Analog Blocks, surrounded by programmable interconnect resources and analog input/output cells with active elements. Configuration data is stored in an on-chip SRAM configuration memory. The AN221E04 device features six input/output cells. In fact, The AN221E04 devices have four configurable I/O cells and two dedicated output cells [6]. The architectural overview of the AN221E04 device is given by Fig. 2.

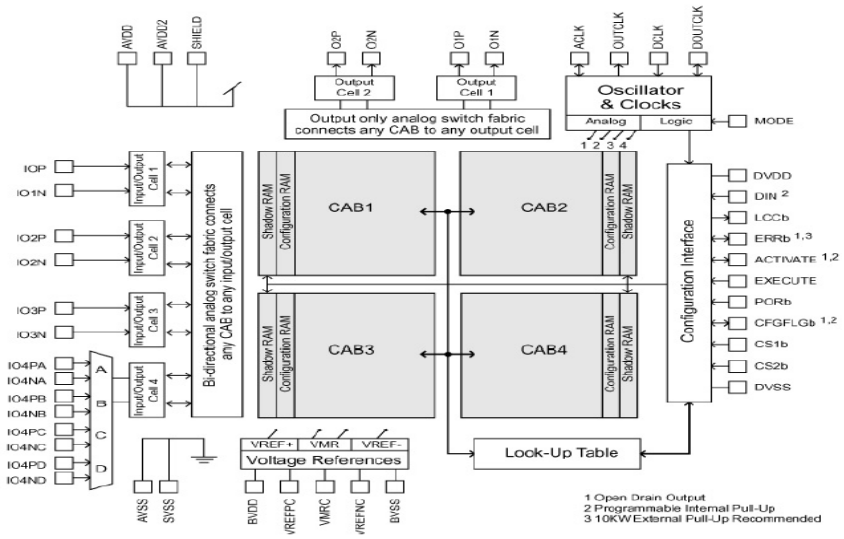

Figure 2: Architectural overview of the AN221E04 device [6]

The circuit design is enabled using AnadigmDesigner®2 software, which includes a large library of analog circuit functions such as gain, summing, filtering, etc... These circuit functions are represented as CAMs (Configurable Analog Modules) which are configurable blocks mapped onto portions of CABs. The circuit implementation is established through a serial interface on the AN221E04 evaluation board using the AnadigmDesigner®2 software, which includes a circuit simulator and a programming device. A single AN221E04 can thus be programmed and reprogrammed to implement multiple analog functions [6].

IV. THE TESTING IMPORTANCE IN CMOS ANALOG INTEGRATED CIRCUITS

Over the past decades, Complementary Metal Oxide Semiconductor (CMOS) technology scaling has been a primary driver of the electronics industry and has provided a denser and faster integration [8-9]. The need for more performance and integration has accelerated the scaling trends in almost every device. In addition, analog and mixed integrated circuit design and testing have become a real challenge to ensure the functionality and quality of the product especially for safety-critical applications [10-11].

In fact, safety-critical systems have to function correctly even in presence of faults because they could cause injury or loss of human life if they fail or encounter errors. The automobile, aerospace, medical, nuclear and military systems are examples of extremely safety-critical applications [12]. Safety-critical applications have strict time and cost constraints, which means that not only faults have to be tolerated but also the constraints should be satisfied. Hence, efficient system design approaches with consideration of fault tolerance are required [12]. In addition, in safety-critical applications, the hardware redundancy can be tolerated to provide the required level of fault tolerance.

In fact, incorrectness in hardware systems may be described in different terms as defect, error, fault and failure. These terms are quite a bit confusing. They will be defined as follows [10-13-14-15]:

Failure: A failure is a situation in which a system (or part of a system) is not performing its intended function. So, we regard as failure rates when we consider that the system doesn't provide its expected system function.

Defect: A defect in a hardware system is the unintended difference between the implemented hardware and its intended design.

Fault: A representation of a defect at the abstract level is called a fault. Faults are physical or logical defects in the device design or implementation.

Error: A wrong output signal produced by a defective system is called an error. Error is the result of the fault and can induce the system failure.

Defining the set of test measurements is an important step in any testing strategy. This set includes all properties and test parameters which can be monitored during the test phase. In the next case study section, we consider the phase shift obtained between the fault free circuit output and the faulty one.

The phase shift definition

Two sinusoidal waveforms having the same amplitude and the same frequency (**f=1/T**) are said in "in phase" if they are superimposed. Otherwise, if the two waves are of the same amplitude and frequency but they are out of step with each other they are said dephased. In technical terms, this is called a phase shift [16]. The phase shift of a sinusoidal waveform is the angle **φ** in degrees or radians that the waveform has shifted from a certain reference point along the horizontal zero axis. The phase shift can also be expressed as a time shift of **τ** seconds representing a fraction of the time period **T** [17]. The next figure illustrates two sinusoidal waveforms phase shifted by 90°.

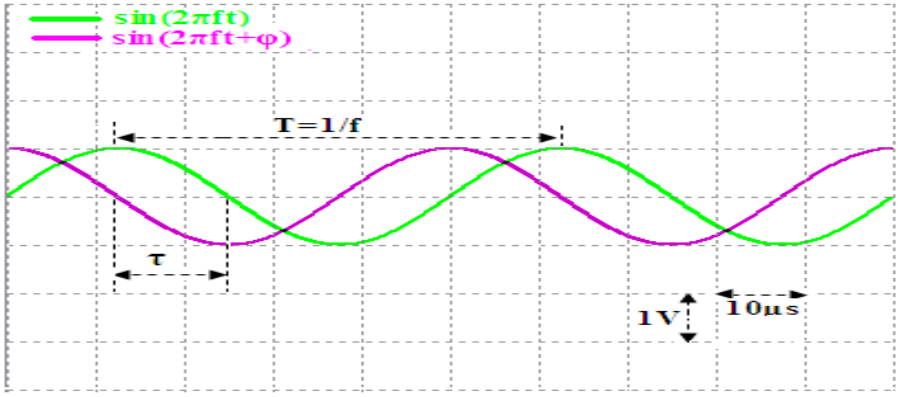

Figure 2: Two sine waves phase shifted by 90°.

The phase shift between the two sine waves can be expressed by:

$$\varphi = 2\pi\tau/T \text{ in radians} \quad (3)$$

And

$$\varphi = 360\tau/T \text{ in degrees} \quad (4)$$

Where T is the sine wave's period which is equal to 50µs and τ is the time lag between the two signals which is equal to 12.5µs. So, we can verify the phase shift value between the two signals shown above using the equation (2): $\varphi=360*12.5/50=90°$

V. THE PROPOSED TESTING METHODOLOGY USING THE FPAA TECHNOLOGY

The proposed testing methodology is base on hardware redundancy. In fact we will distinguish a faulty circuit from a fault-free one by controlling the phase shift between the two considered outputs. The general test procedure is presented by Fig. 3.

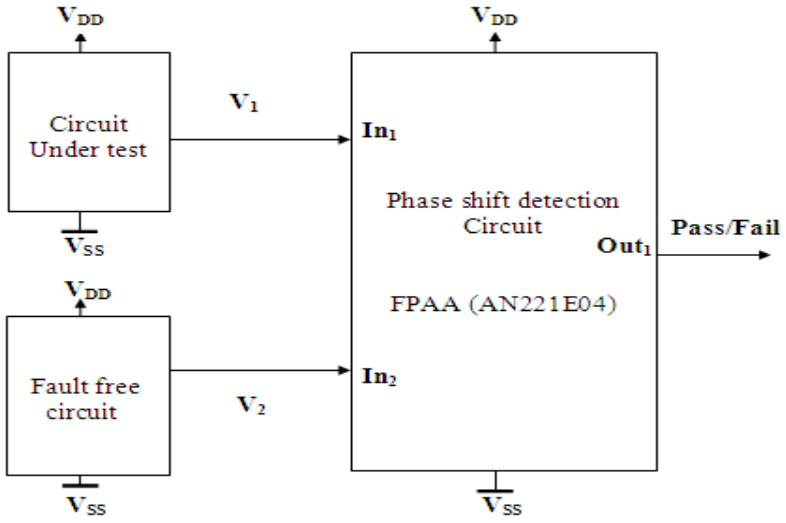

Figure 3: The proposed test approach using the AN221E04 FPAA device

Thereby, the fault detection is obtained through comparing the analog output voltage of the circuit under test (V_1) to a fault free one (V_2). If the testing circuit configured using the AN221E04 board detect a phase shift between the circuit under test output and the faulty free one we assume that the circuit under test gives a wrong signal output. Consequently, the Pass/Fail signal switches from low level (Pass) to high level (Fail) to indicate that the circuit probably contains faults.
Once the fault is detected, we precede to the correctness acts. In fact, the correctness act in our case can be done by replacing the output of the faulty circuit under test by the fault-free one. The hardware redundancy used to detect faults causing phase shift errors in the CUT can be used to correct these faults. Therefore, we have a fault tolerance architecture which assures a correct system functioning even in presence of faults. This fault tolerance mechanism is so important especially for safety-critical systems to avoid the system failure which can cause real damages.
The phase shift detection circuit is illustrated by the circuit diagram given by Fig. 4.

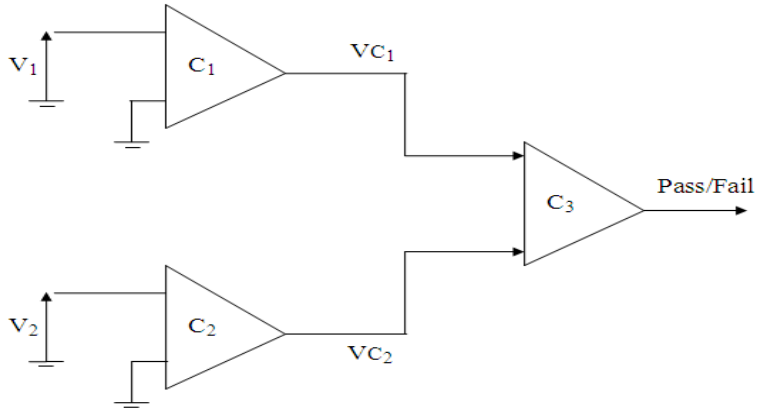

Figure 4: The bloc diagram illustrating the phase shift detection circuit

The two analog comparators C_1 and C_2 are used to compare to zero (ground) respectively the two signals V_1 and V_2. So, the output of each comparator is a digital signal which switches to the high level (VDD) when the correspondent signal is greater than zero. Otherwise it should switch to the low level (VSS). C_3 is a dual comparator used to compare the two digital comparators outputs VC_1 and VC_2. In fact, the Pass/Fail signal which is the output of the comparator C_3 switches from the low level to the high level when $VC_1 < VC_2$.

The Circuit design and implementation are enabled using AnadigmDesigner®2 software. The circuit design illustrating our test methodology is presented in Fig. 4.

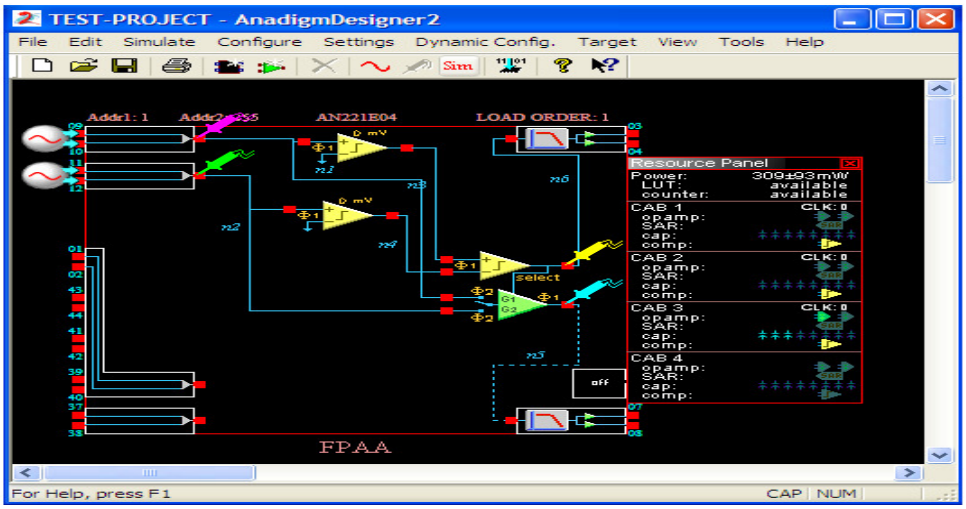

Figure 4: the phase shift detection circuit implemented using the AN221E04 FPAA device

From fig. 2, we note that the phase shift detection circuit implementation only needs the use of three CAM's which are two comparators (C_1 and C_2) and a Gain Stage with Switchable Inputs (C_3). As shown in the resource panel given by the same figure the circuit implementation requires the use of three CABs (CAB 1, 2 and 3).

VI. SIMULATION RESULTS

The fault-free (V_2) and the faulty (V_1) outputs simulation are given by Fig. 5. In this case the phase shift absolute value between the two signals is equal to 30°.

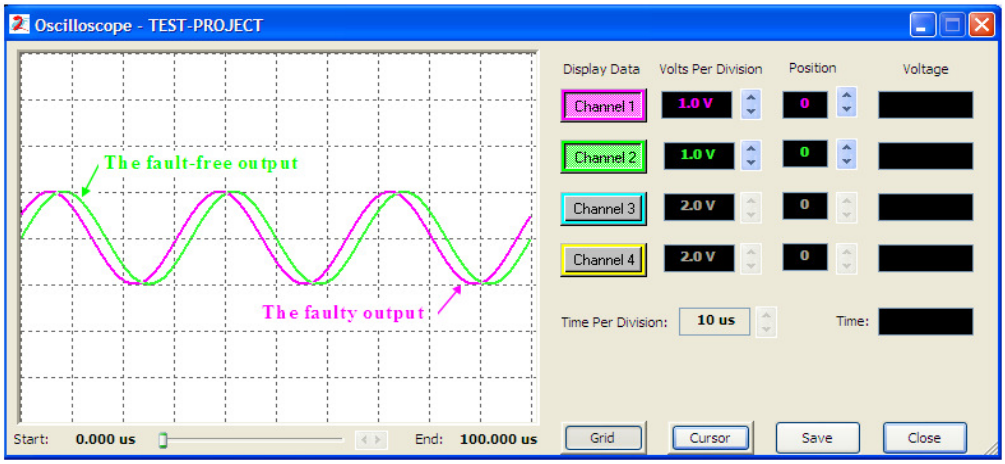

Figure 5: the fault-free and the faulty outputs simulation

Fig. 6 illustrates the fault-free and the first comparator (C_1) outputs simulation results. In fact, the first comparator compares the fault-free output (V_2) to the ground. If the considered output is higher than 0mv the comparator output switches to the high level (5V) otherwise it switches to the low level (-5V).

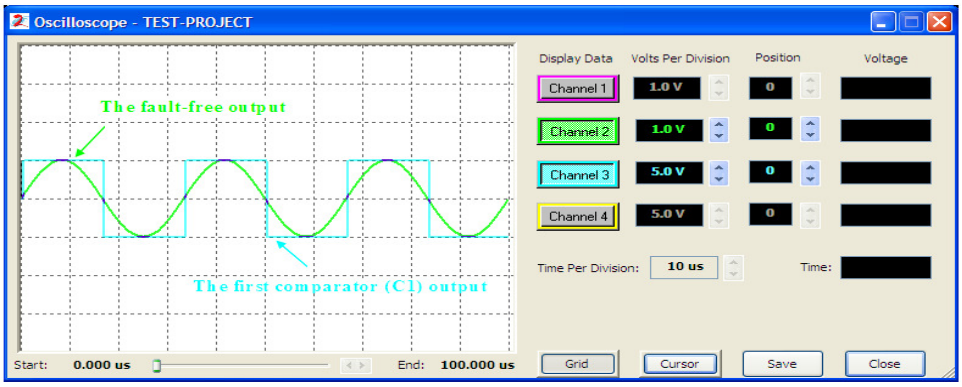

Figure 6: The fault-free and the first comparator outputs simulation results

Fig. 7 illustrates the faulty output of the circuit under test and the second comparator (C_2) output simulation results.

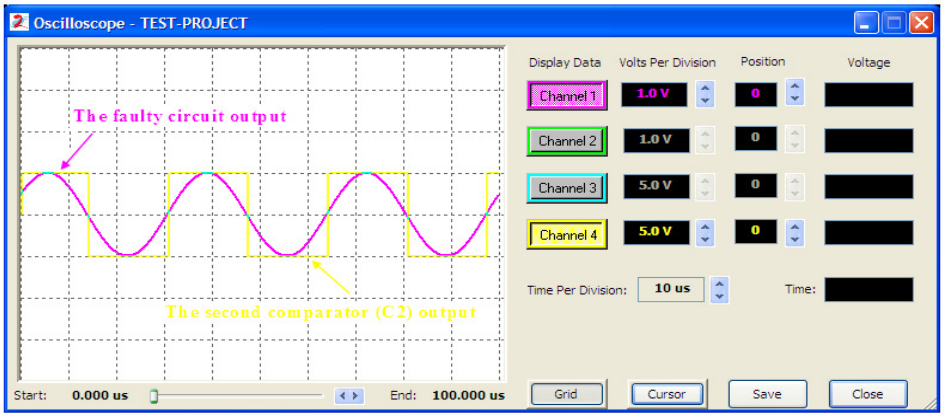

Figure 7: The faulty and the second comparator outputs simulation results

The second comparator (C_2) compares the output under test to the ground. If the considered output is higher than 0mv the comparator output switches to the high level otherwise it switches to the low level.
Fig. 8 presents the superposed comparator's outputs and the Pass/Fail signal which is the output of the Gain Stage with Switchable Inputs CAM (C_3) used as a dual comparator.

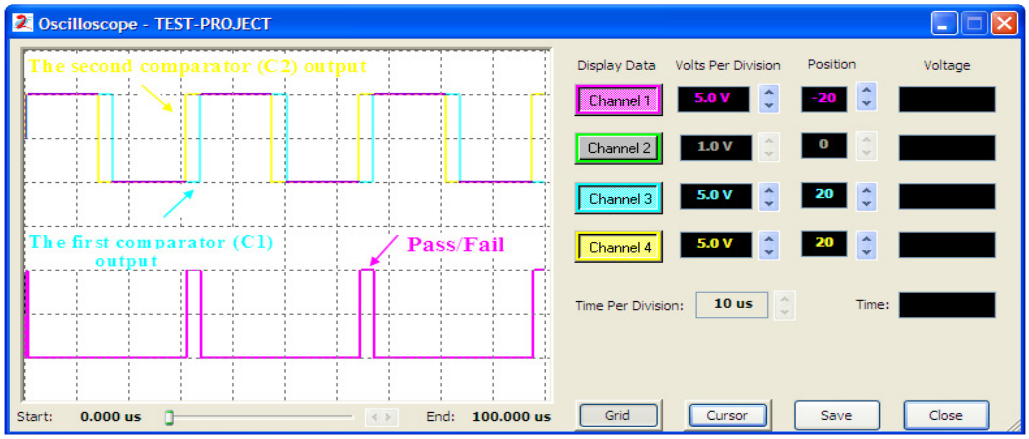

Figure 8: the comparators and the Pass/Fail outputs simulation results

Fig. 9 presents the fault-free, the faulty and the Pass/Fail outputs simulation results.

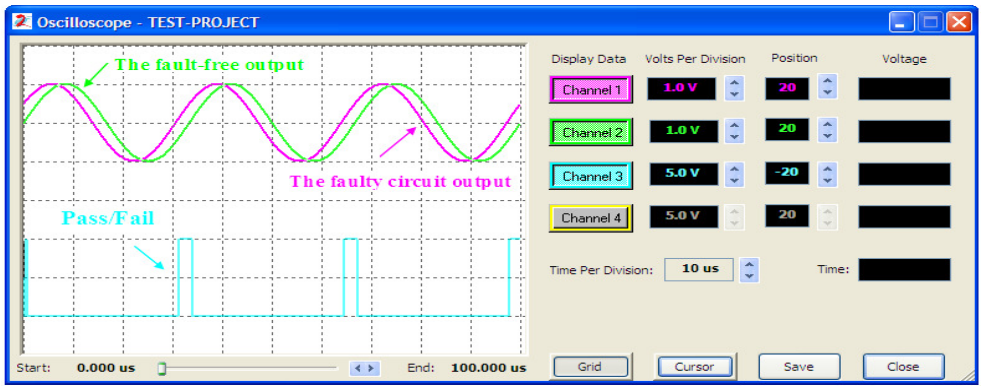

Figure 9: the fault-free, the faulty and the Pass/Fail outputs simulation results

Simulation results given by Fig. 9 ensure that the phase shift detection circuit behaves as intended. In fact, the phase shift existing between the fault-free and the faulty outputs is detected by the phase shift detection circuit. Thus, when the Pass/Fail signal passes to the high level, we assume that the output signal of the circuit under test presents a phase shift error. In addition, the information contained in the Pass/Fail signal enables us to know the exact value of the phase shift between the fault-free and the faulty outputs. Fig. 10 illustrates only the Pass/Fail signal.

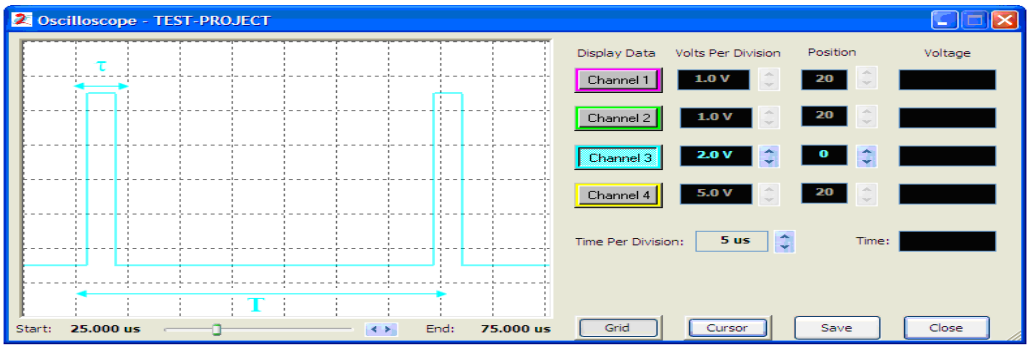

Figure 9: The Pass/Fail signal

In fact, τ and T are respectively the time high and the period of the Pass/Fail signal. The phase shift value in degree is equal to $360^* \tau /T$. In our case, the shift value obtained by simulation is equal to 360*(33.875-31.125)/(64.375-33.875)=32.45°.

VII. CONCLUSION

In this paper, we have presented the Field Programmable Analog Arrays technology which introduces new opportunities to improve analog circuit design and signal processing by providing a method for analog systems rapid prototyping. FPAAs elevate the design and implementation process of analog design to high levels of abstraction. This reduces integrated circuit test costs and time to market.
In fact, an FPAA-based approach phase shift detection circuit is designed and simulated using AnadigmDesigner®2 software. Simulation results show that the technique is effective and prove that the analog integrated circuit design and testing become easier using the Field Programmable Analog Array technology.

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Authors

Mouna KARMANI is with the Electronics & Microelectronics Laboratory, Monastir, Tunisia. She is Pursuing a PH.D in Electronics & microelectronics design and testing at Tunis University, Tunisia.
Email: mouna.karmani@yahoo.fr

Chiraz KHEDHIRI is with the Electronics & Microelectronics Laboratory, Monastir, Tunisia. She is Pursuing a PH.D in Electronics & microelectronics design and testing at Tunis University, Tunisia.
Email: chirazkhedhiri@yahoo.fr

Belgacem HAMDI is with the Electronics & Microelectronics Laboratory, Monastir, Tunisia. Ph.D in Microelectronics from INP Grenoble (France) & Assistant Professor at ISSAT Sousse, Tunisia.
Email: belgacem.hamdi@issatgb.rnu.tn