DESIGN OF HIGH EFFICIENT & LOW POWER BASIC GATES IN SUBTHRESHOLD REGION

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ABSTRACT

Numerous efforts in balancing the trade off between power, area and performance have been done in the medium performance, medium power region of the design spectrum. However, not much study has been done at the two extreme ends of the design spectrum, namely the ultra low power with acceptable performance at one end, and high performance with power within limit at the other. One solution to achieve the ultra low power requirement is to operate the digital logic gates in subthreshold region. We analyze both CMOS and Pseudo-NMOS logic families operating in subthreshold region. We compare the results with CMOS in normal strong inversion and with other known low power logic, delay.

KEYWORDS: *LOW POWER, SUBTHRESHOLD OPERATION, BASIC GATES*

1. INTRODUCTION

In the medium performance, medium power consumption design region, numerous optimization efforts have been made [1, 2, 3]. However, not much study has been done at the two ends of the design spectrum, namely ultra low power with acceptable performance at one end, and high performance design with power within specified limit at the other end. This paper focuses on design techniques for ultra low power dissipation where performance is of secondary importance. One way to achieve this goal is by running the digital circuits in subthreshold mode. The incentive of operating the circuit in subthreshold mode is to able to exploit the subthreshold leakage current as the operating drive current. The subthreshold current is exponentially related to the gate voltage. This exponential relationship is expected to give an exponential increase in delay. The simulation results show that the reduction in power outweighs the increase in delay, and thus, giving the overall reduction in energy consumption per switching. The paper is organized as follows. The application areas of subthreshold are in Section II. Subthreshold cmos logic is described in Section III. Observations of the logic gates in subthreshold region and in strong inversion region is described in Section IV. Finally concluded this paper in Section V.

2. APPLICATION AREAS

Subthreshold digital circuits will be suitable only for specific application which do not need high performance, but require extremely low power consumptions. This type of applications includes medical equipments such as hearing aids and pace maker [4, 5], wearable wrist watch computation [6], and self powered devices [7]. Subthreshold circuits can also be applied to application with bursty characteristics in which the circuits remain idle for an extended period of time. The original active time period T in strong inversion region (top off) is being extended throughout the idle time period T running in subthreshold region(bottom half). The same number of operations is performed in both cases, but with much lower power consumption in the subthreshold operation.

3. SUBTHRESHOLD CMOS LOGIC

Subthreshold logic operates with the power supply Vdd less than the transistors threshold voltage Vt. This is done to ensure that all the transistors are indeed operating in the subthreshold region. We use 90nm process technology for our circuit simulation with Vt of NMOS and PMOS transistor as 0.169v and 0.178V respectively. In subthreshold region, for Vds>3kT/q, Ids becomes independent of Vds for all practical purposes. In analog design, this favorable characteristic has been extensively exploited as

it provides an excellent current source that spans for almost the entire rail to rail voltage range. In digital design, circuit designers can take advantage of this characteristic by being able to use more series connected transistors. The 3kT/q drop is practically negligible compared to the Vt drop in the normal strong inversion region.

Static CMOS is the most common logic style used in sub-threshold due to its robustness. Pseudo-NMOS has also been proposed because some of its disadvantages in strong inversion are mitigated in sub-threshold [8]. The always-on PMOS pull up in pseudo- NMOS is less sensitive to changes in size, but more sensitive to process variations. As a result, the pseudo-NMOS logic style cannot function well in strong-PMOS technologies, because variations in the pull-up device can cause it to overpower the pull-down network despite efforts to counteract this by sizing. Specifically, the distribution of the output low logic level (VOL) can reach nearly to VDD [9]. This sensitivity dramatically reduces the yield of pseudo- NMOS logic for strong-P processes. Static CMOS logic is more robust across different process balances in terms of functionality. However, different metrics applied to static CMOS will vary broadly as process balance changes. This has strong implications for standard cells designed to operate in sub-threshold. Characterization of standard cell libraries will vary dramatically with technology.

3.1 Noise margin

Process variations cause noise margins in static CMOS subthreshold logic to vary [10]. The impact of these variations will change depending on the process balance. Figure 7 shows how the VTC of a sub-threshold inverter changes with process balance. The balanced process has a switching threshold VM, that occurs at VDD/2. This maximizes the high and low noise margins and sets them equal. For processes that are imbalanced toward strong-P or strong-N, either the noise margin low or high will degrade, respectively. As the figure indicates the change in VM and noise margins in subthreshold region.

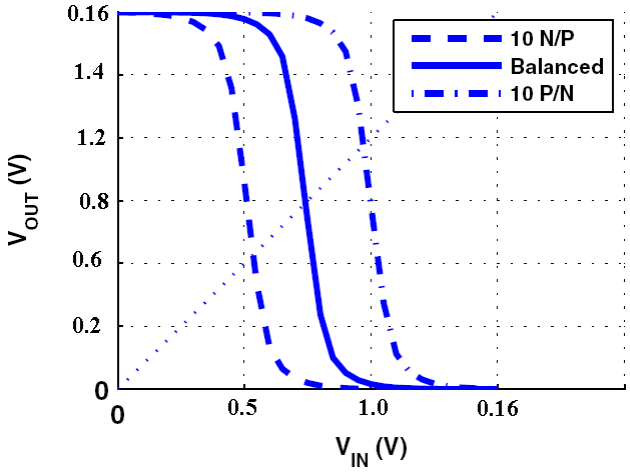

Figure 1. VTC characteristics of an Inverter at different PMOS widths

In this paper basic gates are simulated at subthreshold region. The threshold voltage of nmos transistor is 169mv in 90nm technology. So the voltage Vdd is given 160mv which is below the threshold voltage of the nmos transistor in order to operate the inverter in subthreshold region. The schematic circuit of the inverter is shown in the figure2.

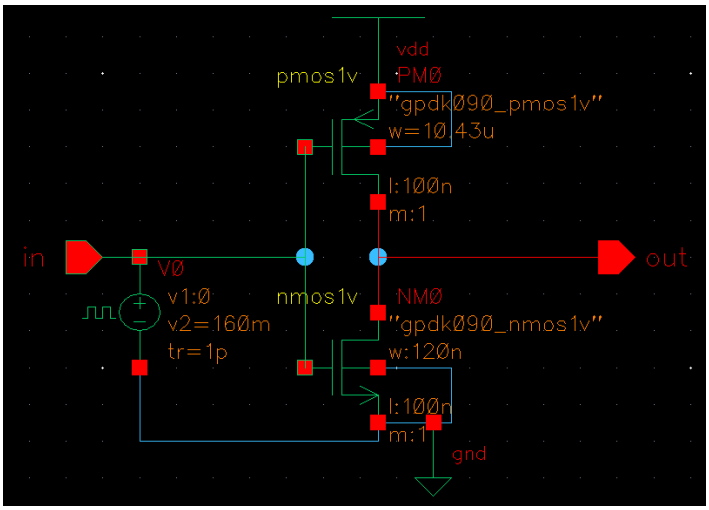

Figure 2. Schematic circuit of inverter

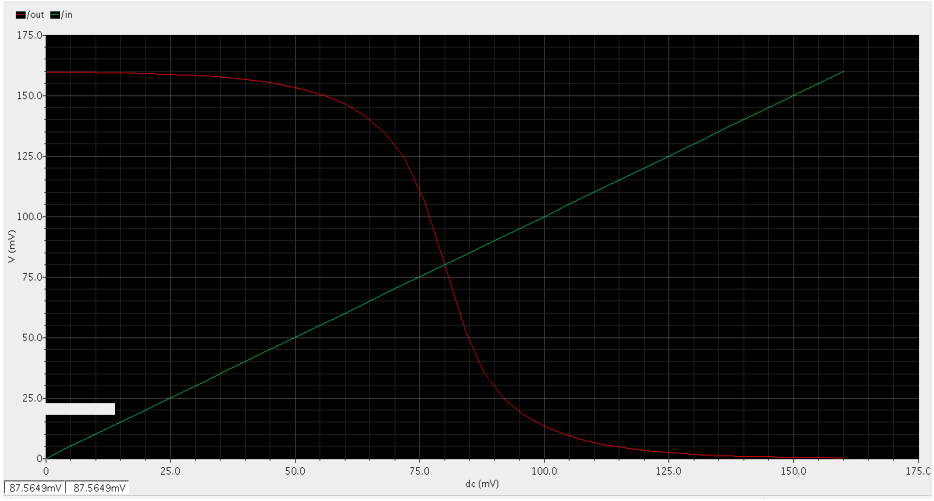

Figure 3. VTC of inverter, switching threshold V_M occurs at Vdd/2 (80mv)

The schematic circuit of the basic NAND gate is shown in figure 4 where the nand gate is operated in subthreshold region. The sizing of the pmos to nmos is done by using some spice calculations. In the subthreshold region of operation the the pmos to nmos ratio is high in order get proper outputs. The capacitance of the drain and source plays a major role in effecting the outputs. In subthreshold region of operation the power consumption is reduced by increasing the delay of the circuit. The output of the nand gate is in figure 5.

Similarly the schematic circuit of the basic NOR gate is shown in figure 6 and output of the NOR gate in subthreshold operation is in figure 7.

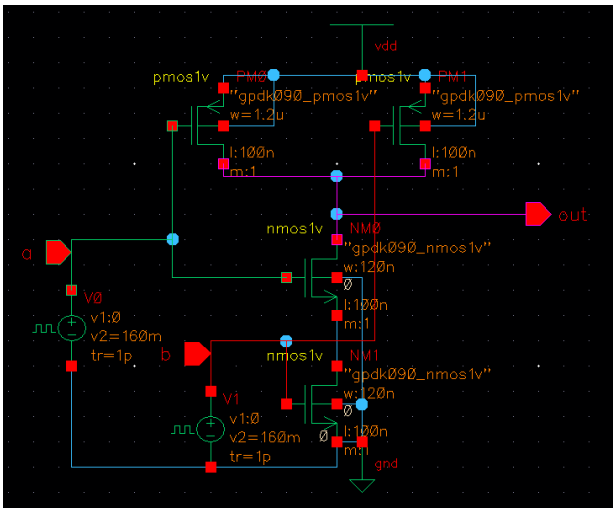

Figure 4. Schematic diagram of nand gate

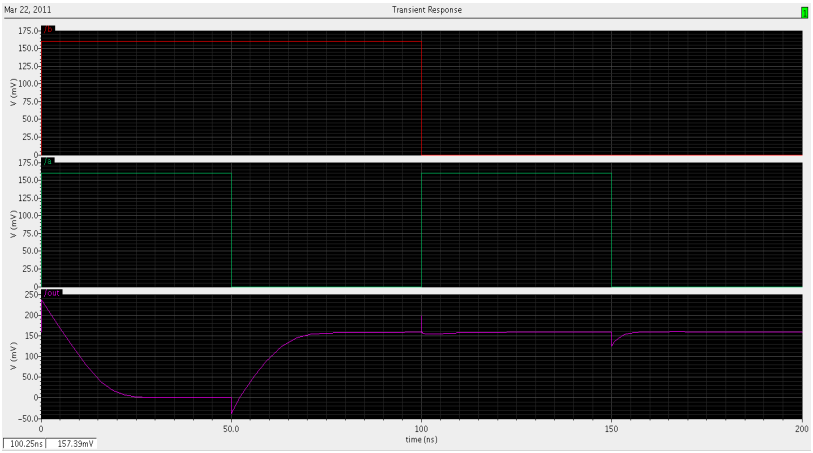

Figure 5. outputs of nand gate in subthreshold region

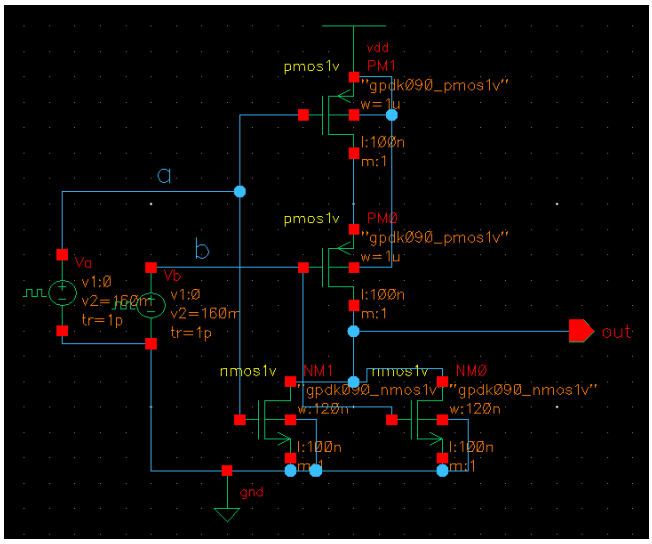

Figure 6. schematic diagram of NOR gate

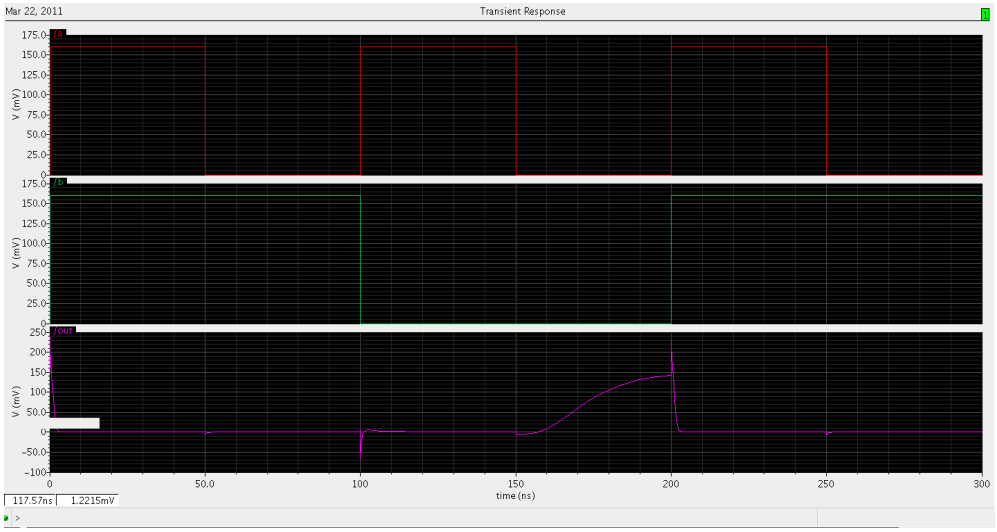

Figure 7. outputs of nor gate in subthreshold region

4. OBSERVATIONS:

The main focus of this paper is the study of basic gates in subthreshold operation. All the gates are simulated in subthreshold region. The power consumption and the delay of the gates for strong inversion region (table I) and subthreshold region (table II) are tabulated.

TABLE I. POWER CONSUMPTION AND DELAY OF BASIC GATES IN STRONG INVERSION REGION

	Inverter	NAND gate	NOR gate
Power (W)	13.05 E-9 W	37.86 E-9 W	46.32 E-9 W
Delay(Sec)	10.1E-13	10.08E-13	10.26E-13

TABLE II. POWER DISSIPATION AND DELAY OF BASIC GATES IN SUBTHRESHOLD REGION

	Inverter	NAND gate	NOR gate
Power (W)	0.59 E-9 W	1.78 E-9 W	1.86 E-9 W
Delay (Sec)	0.352 E-12	1.02E-12	1.13E-12

TABLE III. POWER DELAY PRODUCT COMPARISION

	Inverter	NAND gate	NOR gate
CONVENTIONAL	131.805 E-22W-S	381.6288E-22 W-S	475.2432E-22 W-S
SUBTHRESHOLD	0.20768E-22 W-s	1.8156E-22 W-S	2.1018E-22 W-S

5. CONCLUSION

In order to achieve ultra low power applications, circuits should be operated in subthreshold region without degrading the performance of the circuits. In this paper, we have operated the basic gates both in strong inversion region and in subthreshold region. Power consumption of the gates in strong inversion region and in subthreshold region is tabulated. It is observed that the power consumption of the basic gates in subthreshold region is very much less than in strong inversion region. The delay of

the gates in subthreshold is negligible more than in strong inversion operation. By observing the power delay component when the gates are operated in subthreshold region, the speed can be enhanced.

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