FPGA BASED IMPLEMENTATION OF RATIO HISTOGRAM

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ABSTRACT
Now days, in field of image processing revolutionary changes are taking place. Therefore, it is fascinating to the researchers to undertake the research work in this field. Image processing has jargon of applications with wide scope. Ratio histogram is one of the easiest ways to recognize modifications in the image. This paper presents the facets of deployment of FPGA to develop a system to investigate ratio histogram. FPGA features re-configurability with very less execution time. Moreover, Artrix7 FPGA family comprises of block RAMs, DSPs, Giga-byte transceivers. In the beginning a histograms of consequent images are evaluated and then ratio of those histograms is calculated. Ratio histogram provides information about undesirable changes, the noise, in images. Hardware description language (VHDL) environment is used to develop the firmware for this dedicated system and implemented to obtain the ratio histogram using structural architecture. The ratio histogram produced by the system shows good agreement with that of obtained from MATLAB.

KEYWORDS: *Artrix7FPGA, Image Processing, Ratio histogram, re-configurability, RTL Schematics.*

I. INTRODUCTION

It is aimed to design an algorithm for External Hazard Detection due to terrain, Air traffic, and Runway obstacles. Within this project, in order to process the successive frames, FPGA platform is preferred due to its reconfigurability feature. This article presents a design method for a real-time processing system based on Field Programmable Gate Array (FPGA). A ratio histogram algorithm is implemented in reconfigurable hardware. In real time scenario such as use of mobile phones while driving, No Smoking Zones, etc, there are some rules and regulations, which must be followed[1]. However, wittingly or unwittingly person may lead to break these rules. In such circumstances, there should be automated monitoring system[2]. For example, Cucchiara et al [3] proposed a probabilistic posture classification scheme for classifying human behaviors. Moreover, in case of robbery, an object, which is picked up from the victim to the robber, should be precisely identified. For terrorism, the carried package may be kept deliberately at a typical location of terrorist interest. The detection and identification such objects is the need of the hour to avoid catastrophic phenomenon. To indentify the object, its features should be first detected. Chi-Hung Chaung et al [4] proposed a system, which can be used for detection of suspicious objects. The response time of system designed to indentify such object must be significantly less. Therefore, with the view to increase the speed, a system is designed by using configurable hardware to optimize the reliability and preciseness in the image processing.

Present system is the realization of use of VLSI device, the field programmable gate arrays, to design and implement intensive algorithms. Detection of undesired objects from given image needs to design strong algorithm. Before reproducing the image, it needs to be statistically processed. To maintain real-time feedback to the pilot, use dedicated hardware along with software is the suitable solution. This paper presents a design of real-time processing system, based on Field Programmable Gate Array (FPGA), and Digital Signal Processing (DSP) facilities. Section –II describes the co-development of the hardware and firmware. Section – III is devoted to the interpretation of the results of design and implementation. The work is concluded in section –IV.

II. DESIGNING OF THE SYSTEM

The Ratio histogram, wherein intensity of the pixels is graphically represented, is most powerful technique of image processing. It can be defined as ratio of histograms of two captured continuous frames. Ratio histogram helps to recognize position of pixel, pointing to object which is transiently added in the image. This paper shows the implementation of ratio histogram at high processing speed. Image loader loads image then important processing task begins. Image has to be converted into two dimensional array of pixels. For that MATLAB commands are preferred. MATLAB gives pixel intensities. Then these pixel intensities are stored in Block RAM of FPGA using coefficient file. Main advantage of coefficient is that it is synthesizable. Present design ensures the use of VLSI device to design hardware and the IDE for development of the firmware. Therefore, it is the realization of design on an embedded system for image processing. The designing issues are described through following points.

- Hardware
- Firmware

As discussed earlier, the MATLAB is deployed to code the image.

2.1 Hardware Description:

For present embedded system design, the FPGA from Artrix7 family is employed. A device ID is XC7A100TCSG324-1. It is promisingly featured configurable device, wherein the system design is ensured with the use of Hardware description Language (VHDL). The IDE used for development of the firmware is Xilinx VIVADO. This IDE is facilitated with various smart tools such as design entry, simulation, synthesis, bit stream generation and programming the device etc. These steps will guarantee the essential methodology to get the code for present system. Xilinx VIVADO gives support to provide entry level design using Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL). This computer aided design tool support the synthesis of the system and routing, floor planning and simulation as well. The features of the development board are highlighted as below.

Features of Artrix7 FPGA:

- Nexys 4 board development Board
- Device name : Artrix7 FPGA
- Device ID : XC7A100TCSG324-1
- IDE supported : Xilinx VIVADO
- Extended memory RAM and Flash as well.
- Low power consumption
- Sub-watt performance in 100,000 logic cells
- 2x logic, 2.5x BRAM, 5.7x DSP more slices than Spartan-6 FPGAs
- New Levels of Performance
- Total 63400 LUTs are available
- Single and double differential I/O standards with speeds of up to 1.25 Gb/s

Deploying this development board an embedded system is designed.

2.2 Firmware Description:

An IDE VIVADO 2014.4 version is used to configure XC7A100TCSG324-1 to implement desired logic. It offers best user interface to program the FPGA. Floor planner, timing summary, power report, resource utilization summary can be easily accessed. This IDE is also facilitated with the soft IP cores, deployment of which the firmware can be designed within given time domain. Algorithm of the firmware developed for investigation of the Histograms is as given below.

Get pixel intensities from MATLAB using **imread('path of image')**function**.**

1. Add IP of block memory generator and customize it. Width and depth of block RAM depends on size of the image.
2. Create new .COE file and insert pixel intensities.
3. Repeat step 1 to 3 for second image also.
4. Read the pixel intensities from block memory for both images.

5. Increment array value at index specified by pixel intensities.
6. After reading all pixel intensities, store contents of array(image1) and array(image2) in respective files.
7. Store Computed ratio in separate file.
8. Verification results of ratio histogram with results obtained from MATLAB.

III. RESULTS AND DISCUSSION

Following above described algorithm and Artrix7 FPGA device a system is designed to investigate the histograms of the images. Procedure adopted to obtain the intensities of the pixels of the images under investigation is depicted in figure 1. For present investigation two images are considered. These images are loaded into MATLAB and converted into pixels of the variable intensities. The files bearing information regarding images are produced by the MATLAB. These files are then loaded in the memory of the FPGA device.

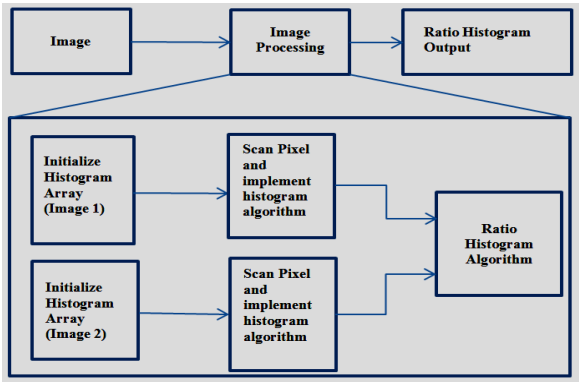

Figure 1 Procedure to obtain histograms of the images under investigation

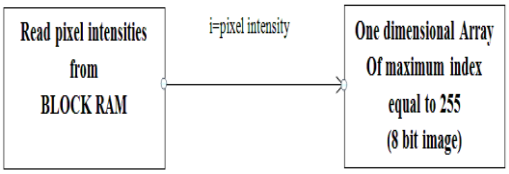

Figure 2 Reading of the pixel intensities from RAM

As presented in figure 3, images are of same person, first image depicts the face of the man. Moreover, a slight change is found in second image. In second image the same person is engaged in cigarette smoking. Now according to the images, second image reveals slight change in the histogram, at the pixels where the cigarette is appearing.

3.1 Rtl Schematics

Using VIVADO these RTL schematics are generated. On successful synthesis, it is ported into the FPGA. These RTL schematics help to identify the flow of data from one component to other. Figure 4 shows the design and implementation RTL for histogram for the image shown in figure 3a of size (239x215). Moreover, the RTL design for histogram of image 2 is also designed and presented in Figure 5.

(a) **(b)**

Figure 3 Images under investigation

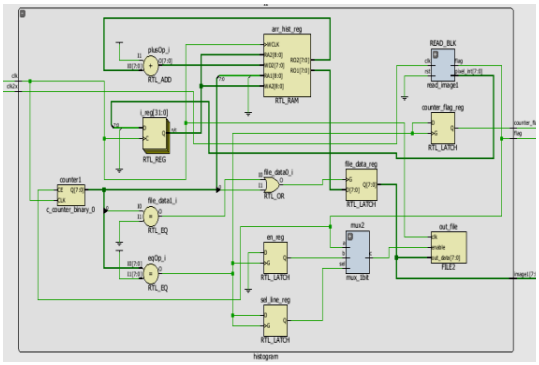

Figure 4 Schematic for histogram for image 1

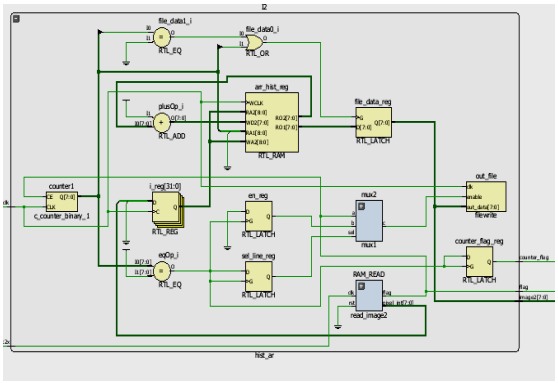

Figure 5 Schematic for histogram for image 2

3.2 Simulation :

The circuit schematic is designed on chip by using FPGA from Artrix7. The information regarding intensities of the pixels, which is already stored in the data memory of the device, is called and processed to ensure the histogram. The results of this VLSI design are validated by employing the process of the simulation. Simulation results, demonstrated in figure 6, incorporate following signals:

a. clk: Half of the system clock is used for computing two histograms and their ratio.
b. clk2x: System clock (100MHz), reads pixel intensities from block memory.
c. dimage1: Shows histogram of first image.
d. dimage2: Shows histogram of second image
e. ratio_out: ratio of dimage1 and dimage2.

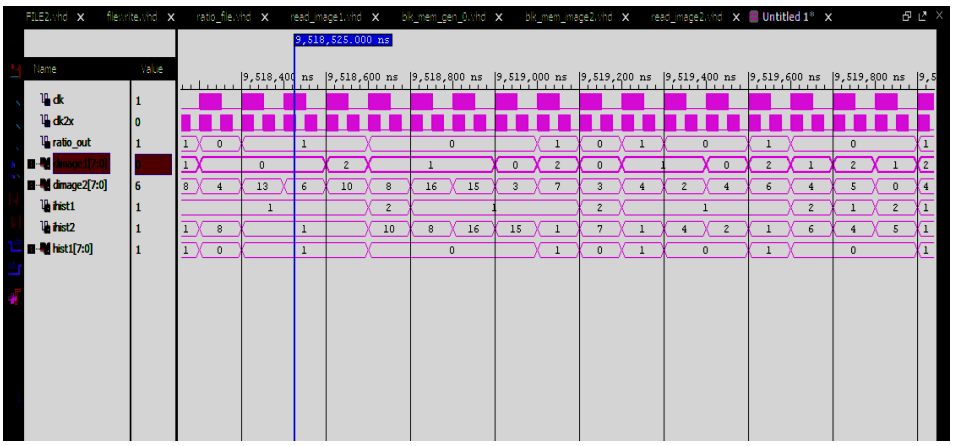

Figure 6 Simulation results of RTL design

Employing the histogram of two images, the ratio of histogram is calculated. It is just pixel wise intensity ratio. The maximum intensity of the pixel is reference to 255. According intensities and hence intensity ratios are calculated. The ratio histogram is now displayed on the monitor and presented in the Figure 7. On intensive investigation of the figure 7, it is found that, the ratio hystogram varies uniformly about one. Moreover, some exceptions are also observed. As shown in the figure 7, the value of the ratio suddenly increases at typical pixels. This can be attributed to the existance of the cigarette in the second image, which is absent in the first image. From this ratio histogram, the position of the cigarette can be immdiately identified. The system works with frequency about 100MHz. Therefore, fast acquisition of the images and processing of the same can be realized. Hence, present system could applicable to the identification of movable object as well. The ratio histogram obtained from MATLAB is also depicted in figure 8. Close agreement of these ratio histograms reveals the preciseness in the design.

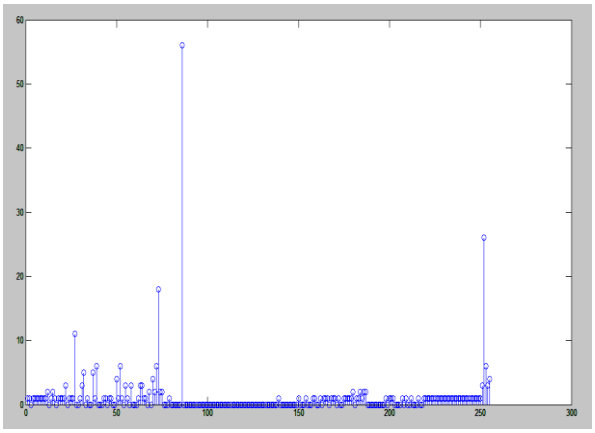

Figure 7 Ratio histogram output from FPGA

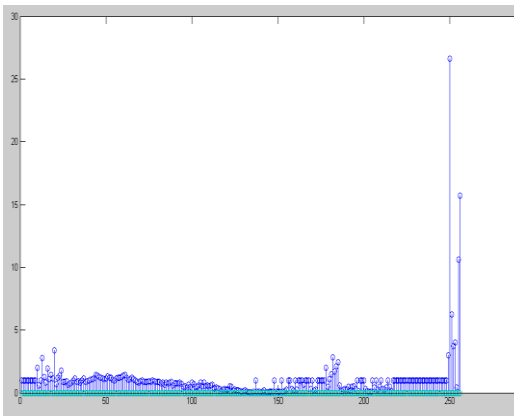

Figure 8 Ratio histogram output from MATLAB code

While working with the system, it was also found that, at a typical pixels the intensity is less than one or zero. In fact, these are exceptions. But, when it occurs, then the ratio histogram depicts indetermined quantity. Therefore, it is essential to overcome such exeptions. To overcome the exceptions, the significant level of the intensity of the pixel is considered as 1 for darkness and 255 for bright pixel. Thus, occurrence of the exeptions in this data processing is removed.

IV. CONCLUSION

It can be concluded that, hardware processing is very fast because of processing time required is in nano seconds. Ratio histogram is very strong tool to recognize variation in two successive frames. FPGA implementation is complex but processing is faster than MATLAB for large size images.

REFERENCES

[1] Stephanie Parker, "Implementing a Histogram Equalization Algorithm inReconfigurable Hardware" Undergraduate Student, Stephanie_parker1987@yahoo.com
[2] J. Kemi Ladeji-Osias, Associate Professor, Jumoke.Ladeji-Osias@morgan.edu.Morgan State University, Department of Electrical and Computer Engineering, 5200 ring Parkway, Baltimore, MD 21251.
[3] R. Cucchiara, C. Grana, A. Prati, and R. Vezzani, "Probabilities posture classification for human-behavior analysis," IEEE Trans. Syst., Man Cybernetics-Part A: Syst. and Humans, vol. 35, no. 1, pp. 42–54,Jan. 2005.
[4] Chi-Hung Chuang, Jun-Wei Hsieh, Luo-Wei Tsai, Sin-Yu Chen, and Kuo-Chin Fan, "Carried Object Detection Using Ratio Histogram and its Application to Suspicious Event Analysis," IEEE Transactions On Circuits And Systems For Video Technology, Vol. 19, No. 6, June 2009

BIOGRAPHY

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