COMPARATIVE ANALYSIS OF MATERIAL PROPERTIES FOR HETEROSTRUCTURES

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ABSTRACT

In this paper, after a description of the techniques used to realize heterostructures, we present a comparative analysis of the properties of materials used, in order to identify those that best adapt to the different fields of application. At last we present, as an example, a simulation study of a TFET (Tunneling Field Effect Transistor) inverter, whose performances are compared with those of a typical MOS inverter.

KEYWORDS: *Heterostructure, Materials, Technology, TFET, CMOS, Advanced Design System (ADS).*

I. INTRODUCTION

When a contact is made between different semiconductors, i.e. having different values of the band gap, we speak of heterojunctions or heterostructures. The diversity of the band gap leads, in thermal equilibrium conditions, to the formation of particular profiles of the conduction band and the valence band, which can be used for the manufacture of electronic and optoelectronic devices with very advanced performances.
The $Al_xGa_{1-x}As$ family of ternary semiconductors is widely used to manufacture heterojunction electronic and optoelectronic devices. By varying x (0 ÷ 1), which id the mole fraction of aluminium, different values of the band gap and therefore different semiconductors are obtained.
In the case in which x = 0 we obviously obtain gallium arsenide, with a band gap of 1.42 eV and a lattice constant of 5.653 Å at 300 K. For x = 1 we have aluminum arsenide, with a band gap of 2.17 eV and a lattice constant of 5.66 Å.
The band gap of the ternary compound $Al_xGa_{1-x}As$ therefore grows with x, while the lattice constant essentially does not vary; even in the two extreme situations, at x = 0 and x = 1, the lattice mismatch, i.e. the relative difference between the lattice constants, is only 0.1%.
From a technological point of view it is convenient to create heterojunctions only between materials having very similar reticular characteristics so that the contact surfaces are as non-defective as possible. In fact, the interfaces of the junctions between the various semiconductors must be of high purity and quality in order to obtain satisfactory performance from the manufactured devices.
Furthermore, heterostructure devices present many manufacturing difficulties linked above all to the need to fabricate junctions between layers of different semiconductors, with doping levels varying sharply and with thicknesses even in the order of tens of angstroms.
Current technology, thanks to the improvement achieved in epitaxial growth techniques such as MBE and MOCVD, allows the creation of excellent quality heterostructure devices even if the costs are far higher than those of planar technology [1-4].

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In this paper, after a description of the techniques used to realize heterostructures, we present a comparative analysis of the properties of materials used, in order to identify those that best adapt to the different fields of application. At last we present, as an example, a simulation study of a TFET (Tunneling Field Effect Transistor) inverter, whose performances are compared with those of a typical MOS inverter.
The presentation is organized as follows. In Section 2 we describe the techniques used to realize an heterostructure. The comparative analysis of materials used to realize heterostructures with a simulation study of a TFET inverter is presented and discussed in Section 3. The conclusions are described in Section 4.

II. FABRICATION TECHNIQUES

In order to realize an heterostructure, it is necessary to use two or more layers of different materials growth one on top of the other.
This result is obtained by two techniques: Molecular Beam epitaxy (MBE) or Metal Organic Chemical Vapor Deposition (MOCVD), described in following sub-Sections.

2.a MBE

MBE is the most versatile growth technique and consists of use a high-vacuum chamber whit a semiconductor substrate. Different materials, like Ga, Al, As for example, are stored and heated in different chambers or cells whit an opening. The selected material escapes from the cell thanks to the opening and form a molecular beam which is directed forward the substrate, according the schematic reported in Fig. 1.

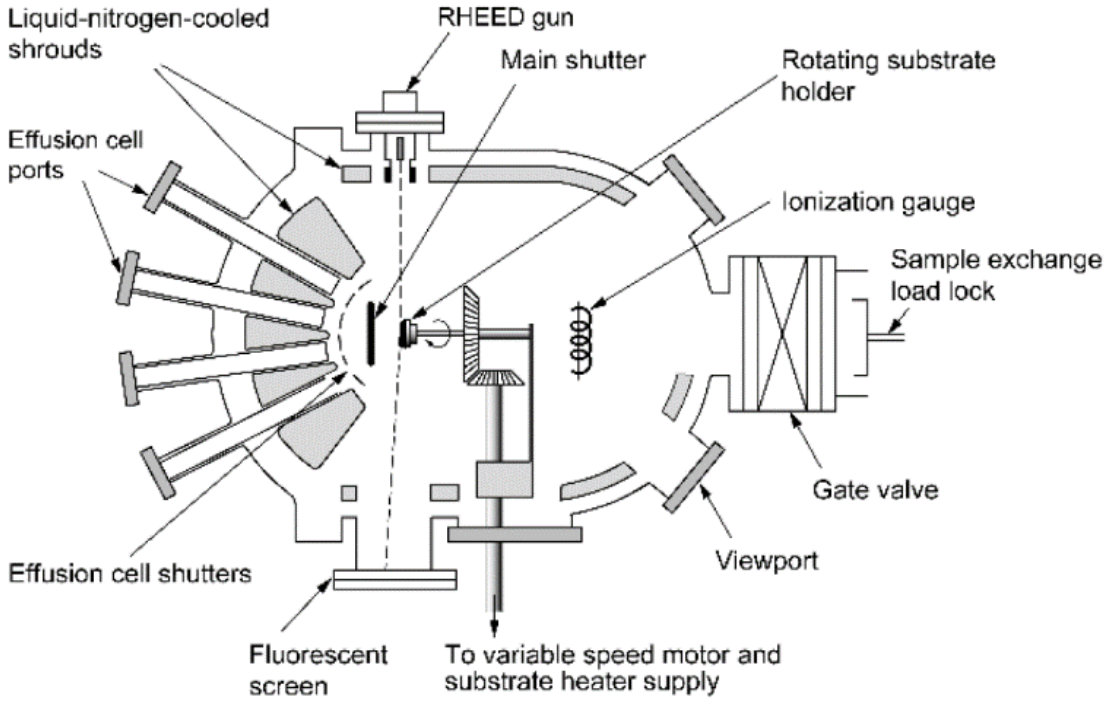

Figure 1. MBE schematic.

It is possible to obtain ad high-quality crystal by selecting a low temperature growth and a slow growth rate for the substrate.
MBE allows the best control of the material composition and of the epitaxial layer thickness. This techniques is used to growth semiconductors like AlGaAs , InGaAs, InAlAs.
The principal limitation is represented by the lattice parameter of the element selected for the process, because they must match to minimize the number of defects in the epitaxial layer [5]. That is because the morphological defects can affect to the smoothness of the semiconductor wafer and the yields.

Another important limitation of this technique is the cost: MBE is expensive for high-volume production and that is the reason why the MOCVD is preferred respect to MBE.

2.b MOCVD

This technique consists in chemical reaction thanks to gas at moderate pressure, that depends on the elements uses in the processes and other characteristics, like the growth rate or the concentration.

Pure gasses are injected into a chamber made in material which do not react with the elements and condition of temperature. Gasses fall on a semiconductor wafer and made a thin layer of atoms (see Fig. 2).

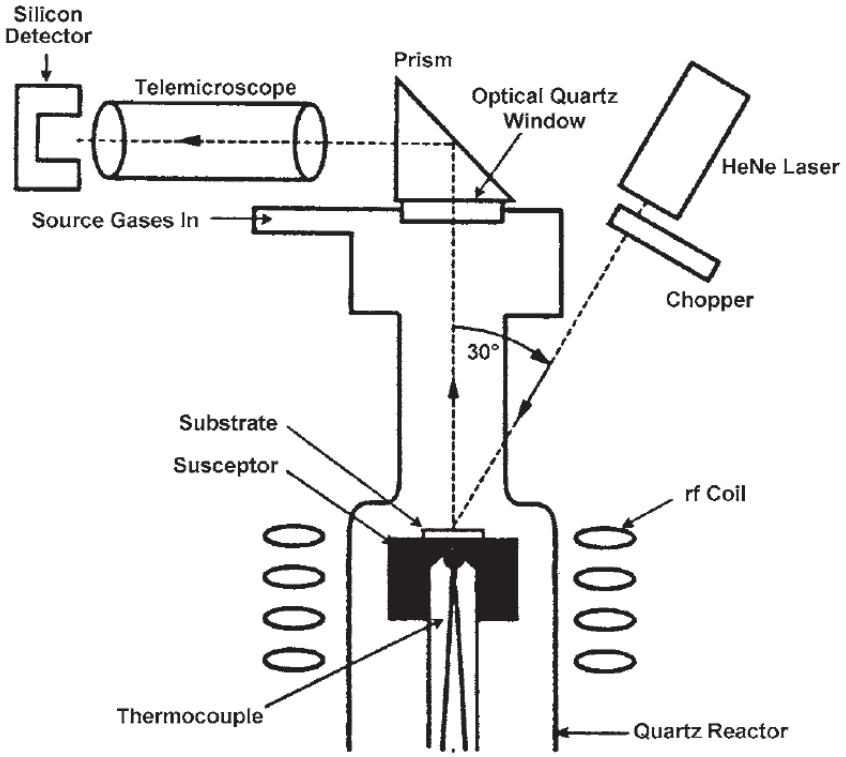

Figure 2. MOCVD schematic.

MOCVD offers the possibility to growth materials that are difficult to obtain by other techniques, for example material as P, which has a high vapor pressure, or Al-bearing alloys which presents problem in combination with chloride in vapor phase due to the thermodynamic constraints [6].

The principal filed of application of this technique is in optoelectronics, for light emitting devices in the 540 nm to 1600 nm range, lasers and photodetectors. In this field are used GaAs or InP substrates, that require thin doped layer made with combination of In, Ga, Al, As.

The mismanage of MOCVD is in the precision of the process. Electronics devices and some photodetector require high level of precision in intra-and inter-wafer uniformity during the process, which is obtained in MBE technique.

III. MATERIALS USED TO REALIZE HETEROSTRUCTURES

3.a Energy band diagram for an ideal heterojunction: a brief review [2] [7]

In [2] and [7] we have already shown the rules to build the energy band diagrams of an ideal heterojunction (i.e. with a negligible number of traps and centers of generation-recombination at interface) before and after the forming the junction, and therefore we advice the reader to consult these references.

The hypothesis of ideality is verified for semiconductors with a low relative difference between the lattice constants. Moreover in [2] and [7] we shown that the potential barriers that electrons and holes

must overcome to move are different and this is the main property of heterostructures, which led to the realization of Heterojunction Bipolar Transistor (HBT) [7].

3.b Comparison among material properties

To achieve particular requirements for different applications, the Table 1 shows several of the most used materials for optical and electronics applications.

Table 1. Results of extraction procedure at room temperature.

Application	Requirements	Substrate Materials Doping	Attributes of the materials
Telecommunication lasers	High optical efficiency, High doping and control of the p-n junction	InP/InGaAsP, InGaAs InP Zn(p) Si or S (n)	High luminescence and Controlled lattice match
Tlc fiber pump lasers	High optical efficiency, High doping and control of the p-n junction	GaAs/AlGaAs InGaAs InGaP Zn or Mg (p) Si(n)	High luminescence, Interfacial abruptness and lattice match
High speed Cd lasers for storage	High optical efficiency, High doping and control of the p-n junction	GaAs/AlGaAs GaAs Zn (p) Si(n)	High luminescence, Interfacial abruptness and lattice match
PIN photodiodes at 900-1600nm	Low dark current High responsivity	InP/InGaAs	High purity
Far infrared photodetectors	High responsivity, Low dark current	GaAs/HgCdTe ZnTe	Low background doping Bandgap control
Solar cell	High conversion efficiency	GaAs/AlGaAs InGaP, GaAs	Low deep level concertation
Heterostructure transistor	Uniform controlled gain	GaAs/AlGaAs InGaP GaAs	Precise, uniform and controlled doping at high levels

Table 2 shows difference in term of Valence Band offset in heterostructures, measured in eV.

Table 2. Valence Band in different heterostructures.

Heterojunction material	ΔEv(eV)
$GaAs/Al_xGa_{1-x}As$	0.46x
GaAs/AlAs	0.31
GaAs/InAs	0.35
$AlAs/Al_{0.37}Ga_{0.63}As$	0.34
AlAs/InAs	0.35
$InP/Ga_{0.47}In_{0.53}As$	0.32
GaAS/ALSb	0.40
$GaSb/InAs_{0.95}Sb_{0.05}$	0.67
CdTe/HgTe	0.34
CdTe/ ZnTe	0.40
ZnTe/HgTe	0.30
GaN/AIN	0.7±.24
AlN/GaN	0.57±0.22
InN/AlN	1.81±0.2
InN/GaN	1.051
$Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.47}As$	0.75
GaSb/InAs	0.51
AlN/InN	1.32±0.14
$Ga_{0.5}In_{0.5}P/GaAs$	0.32

As you can see, equals heterostructures can have dissimilar value of the offset. Same consideration for the similar combination of materials that are different for one only element.

Regards to **$GaAs/Al_xGa_{1-x}As$**, as shown in Table1, a lot of devices are made with this heterostructure. x is variable from 0 to 1 and represent the molar fraction of the Aluminium, which have consequence on the Energy Gap of the new material.
The band alignment has a very important role on the electrics characteristic of the material and there are many types of them.
The determination of the band alignment is not a simple task: theoretical and experimental models are use at first and the second step is to make the heterostructure and measure the effective band alignment. Fig. 3 shows some experimentally determine band alignments of different type, straddling, staggered and broken gap alignments.

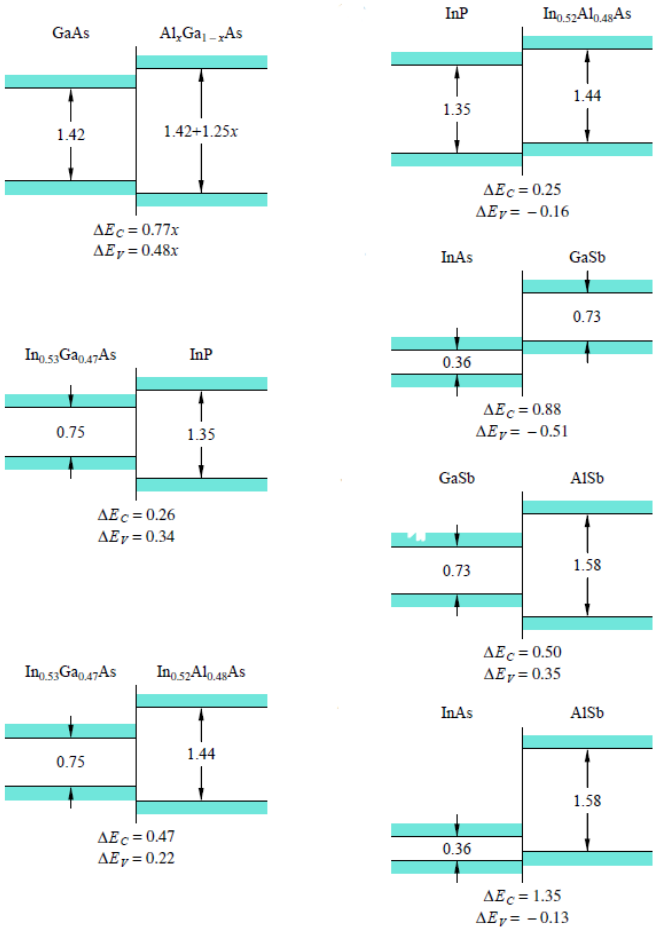

Figure 3. Different type of Bands alignments.

Regards to **GaN**, it is a semiconductors compound by III-V elements with a high Energy Gap equal to 3.4 eV and therefore was used in optoelectronics. Currently it is used also in electronics devices which require wide band and high power because respect the GaAs, GaN offer more resistance at high temperature and hard condition of work [8].

With reference to **InAs** and **GaSb**, their broken-gap band line-up makes possible to create both semiconducting and semi metallic heterostructures with tuneable virtual band gaps.
As long as the confinement energy of the carriers in the effective electrostatic potential of the heterostructure is small, electrons can lower their energy by dropping from the GaSb valence band to the InAs conduction band until the Fermi level E_F is equal in both layers and the system is in equilibrium, as shown in Fig. 4 [2].

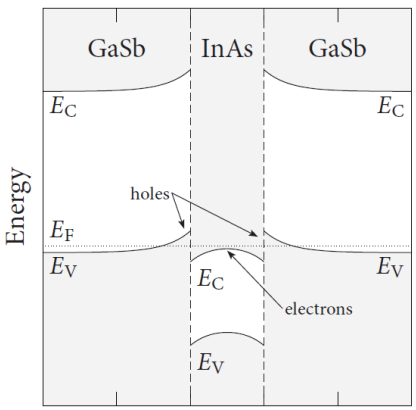

Figure 4. Band Alignments in GaSb-InAs [2].

3.c Design example a NOT gate based on TFET

Fig. 5 shows the TFET structure [9], whose analysis is made by the MIT TFET Model [10].

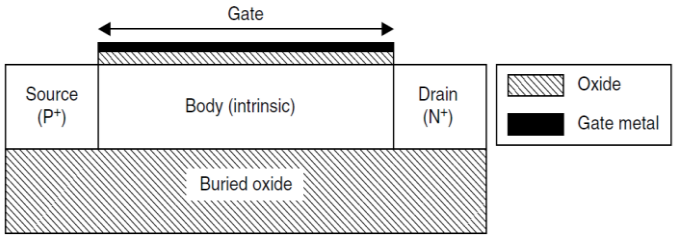

Figure 5. TFET structure.

The basic principle of TFET is the tunnel effect [1-2], and, in order to occur this effect, it is necessary to introduce a p-i-n (p-type, intrinsic, n-type) structure, as shown in Fig. 6, in which the green dot on the channel represents the trap states.

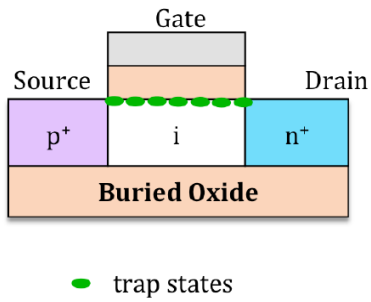

Figure 6. MIT TFET structure [10].

Thanks to this structure in a TFET the electrons can pass through the source-channel junction with a lower energy and with a lower subthreshold swing respect the conventional MOSFET [1-2].
As an example, we simulate a TFET inverter (Fig. 7), using ADS software [11] and comparing its performance with those of a MOSFET inverter.

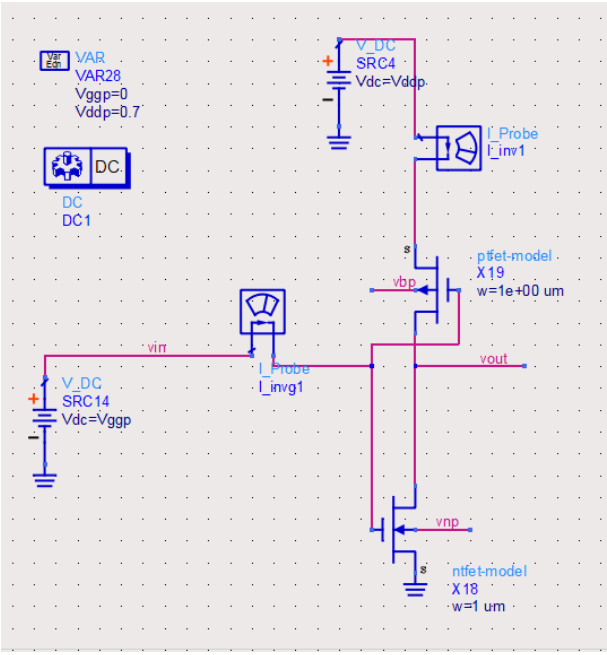

Figure 7. Schemtic of TFET Inverter.

The obtained DC characteristics are plotted in Fig. 8.

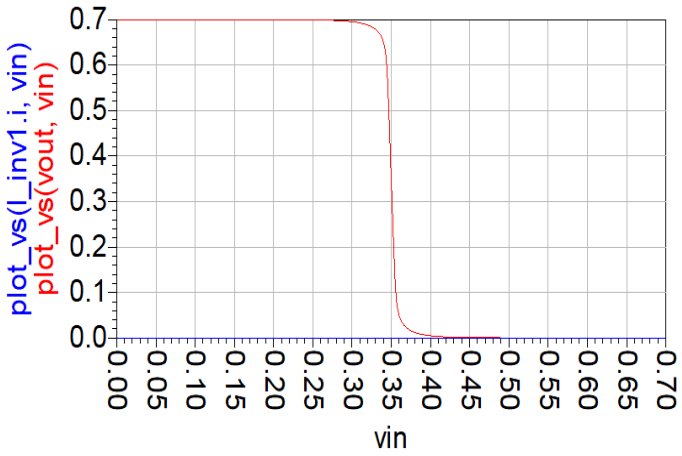

Figure 8. Characteristics of TFET Inverter.

As you can easily see from Fig. 8, the vertical characteristic for TFET inverter is at 0.35 V, while for MOSFET inverter, in the same condition of work, we have obtained 0.8 V, resulting in an increase in immunity noise for MOSFET inverter.
Regards to the transient analysis, the output for TFET inverter, reported in Fig. 9, presents an overshoot (Fig. 10) and a delay propagation.

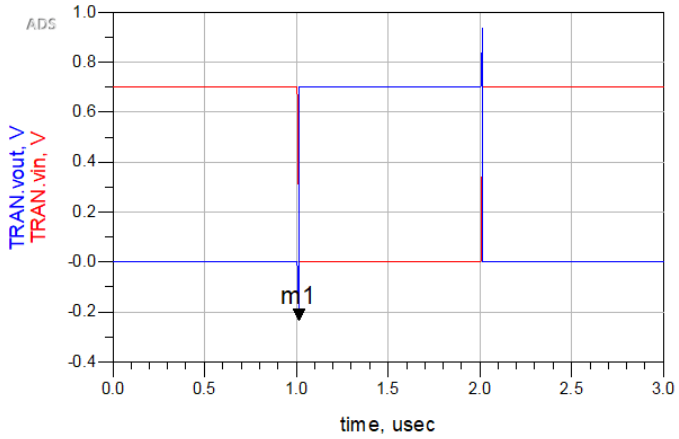

Figure 9. Transient analysis of the circuit of Fig. 7.

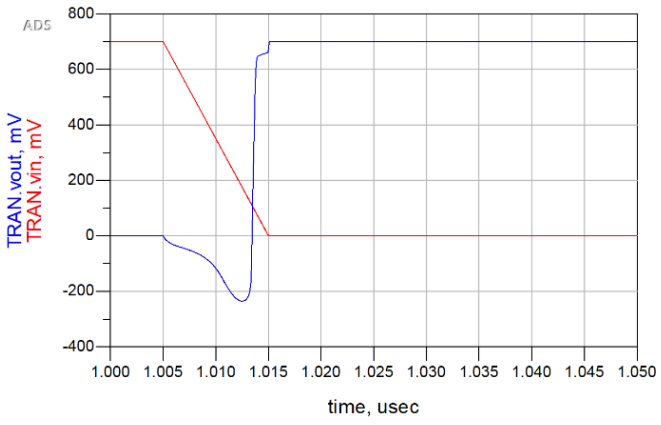

Figure 10. Focus on the overshoot.

The comparison with the MOS inverter showed that at 100 MHz there are problem on the lower level of the output. This situation becomes more critical in presence of electromagnetic interference or another type of disturb, because a 0 logic can be confuse as 1 logic.

IV. CONCLUSIONS

We have analyzed at first the main techniques used to realize heterostructures.
Then we have shown a comparative analysis of the properties of materials used, in order to identify those that best adapt to the different fields of application.
At last, as example, we presented a simulation study of a TFET inverter, whose performances have been compared with those of a MOS inverter.
Ultimately we can say that, thanks to the improvement of the modern growth technologies, materials that at beginning were difficult and expensive to obtain, are cheaper and efficient and therefore currently used for the realization of electronic and optoelectronic devices.

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Prof. Perri is the Head of the Electron Devices Laboratory of the Polytechnic University of Bari and is author of over 350 journal articles, conference presentations, twelve books and currently serves as a Referee and Editorial Board Member of a number of international journals.
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