FLEXIBLE DIFFERENTIAL FREQUENCY-TO-VOLTAGE AND VOLTAGE-TO-FREQUENCY CONVERTERS USING MONOLITHIC ANALOGUE RECONFIGURABLE DEVICES

Ivailo Milanov Pandiev
Department of Electronics, Technical University of Sofia, Sofia, Bulgaria

ABSTRACT
This paper presents differential frequency-to-voltage (F/V) and voltage-to-frequency (V/F) converters employing single CMOS Field Programmable Analog Array (FPAA) device. The proposed electronic circuits are based on charge-balance conversion method. The F/V converter basically consists of analogue comparator, differentiator that detects the rising and falling edges of the shaped waveform, voltage-controlled switch and output low-pass filter, working as an averaging circuit. The V/F conversion circuit includes the same modules. The input signal for the V/F circuit is applied to an integrator (realized with low-pass filter) through two-position voltage-controlled switch and the positive feedback is closed by external electrical connections. The proposed converters can be redesigned during operation, in dependence on the amplitude, frequency range and noise level of the input signal, without using of external components or applying of external current or voltage. The functional elements of the converters are realized by employment of the available configurable analogue modules (CAMs) of the FPAA AN231E04 from Anadigm. The converters have wide-band frequency response and can operate with single supply voltage of 3.3V. The experimental results show that the linearity error is less than 0.5% at the frequency range of 0 to 20…25kHz and differential input range operation of 0 - 3V.

KEYWORDS: *Mixed-signal circuits, Charge-balance voltage-to-frequency conversion method, Frequency-to-voltage converter (FVC), Voltage-to-frequency converter (VFC), FPAA, System prototyping.*

I. INTRODUCTION

The voltage-to-frequency converters (VFC) are voltage-controlled oscillators whose frequency is linearly proportional to a control input voltage. The VFCs are useful devices for variety of mixed-signal (analogue and digital) processing systems, such as A/D conversion systems with a microcontroller, temperature meters, long-term integrators with infinite hold and telemetry systems [1-4]. The dual process of the voltage-to-frequency (V/F) conversion is the frequency-to-voltage (F/V) conversion. Besides, its independent applications to a speed indicator and motor speed control system (tachometer), the FVC paired with the VFC is used for high noise immunity data transmission systems and FSK generation and decoding.

The basic electrical parameters that define the quality of the F/V and the V/F converters are maximum working frequency, sensitivity and linearity error. For the commercial monolithic F/V and the V/F converters, such as AD650 (from Analog Devices), LM2907 (from Texas Instruments) and LM331 (from Texas Instruments) the transfer function and the related electrical parameters are formed by the internal active building blocks and a group of external passive components. Moreover, the accuracy of the electrical parameters is largely determined by the manufacturing tolerances and the temperature drift of the values of the external passive components. A variety of F/V and the V/F converter prototype circuits for mixed-signal signal processing, are available in the literature [5-15]. Furthermore, some of them realize only V/F conversion or F/V conversion, while others implement both functions of conversion [5]. The majority of the published circuits of F/V and the V/F converters have fixed value of the sensitivity and possibility for modification of this value is not demonstrated. In many cases the amplification of small signals (such as bio-signals) requires modification of the

sensitivity according to the variation of the amplitude, the bandwidth or the noise level. To solve this problem, it can be used Field Programmable Analog Array (FPAA) devices. The FPAA are programmable CMOS analogue integrated circuits based on SC technology, which can be configured not only in the design process of a device, but also during the operation. As well as FPGA the programmable analogue arrays provide cost-efficient and relatively fast design of complex electronic circuits.

The use of these reconfigurable analogue devices provides the F/V and the V/F converters with ability to modify the electrical parameters according to the parameters of the input signals. Furthermore, by using of FPAAs the noise level can be obtained with significantly lower values due to the differential inputs and outputs. Among different devices and technologies in the market [16-18], Anadigm [19] offers dynamically programmed FPAAs (or dynamically programmed analogue signal processors - dpASPs), in particular the AN231E04 that is a reconfigurable programmable analogue device based on switched-capacitor technology. The AN231E04 device consists of a 2 2 matrix of fully configurable analogue blocks (CABs), surrounded by programmable interconnect resources and analogue input/output cells.

The VFC in [10] is realized by using single FPAA AN221E04 and convert the input voltage from 0 to 3*V* into square waves within frequency range from 0 to 7k*Hz*. Thus, the sensitivity of [10] is 2k*Hz/V* and the achieved relative linearity error is approximately equal to 2%. As a flexible differential building block, however, it is desirable to realize the V/F converter in a form of compatible with the F/V converter. With this in mind, novel FPAA-based circuits are developed for F/V and V/F conversion.

The organization of the paper is as follows: the structures and the principles of operation of the F/V and the V/F converters are described in section II; for the proposed electronic circuits in section II the transfer functions and methods for modification of the transmission coefficients are given; in section III are illustrated the experimental test of the proposed converters based on AN231K04-DVLP3 – development board [20], which is built around the AN231E04 device and finally in section IV the concluding remarks and directions for future work are discussed.

Nomenclature

t_{os}	Pulse with duration, determined by the master clock frequency for all CAMs
f_{in}	Frequency of input signal
f_c	Corner frequency of low-pass filter
K_2	Transmission coefficient of the *SumFilter1* CAM
U_{ref}	Reference voltage
K_V	Sensitivity of F/V converter
f_{out}	Frequency of output signal
U_{in}	Input voltage
t_{int}	$\frac{1}{f_{out}} - t_{os}$ - amount of time required to reach comparator threshold
K_f	Sensitivity of V/F converter
dc	Direct current

II. CIRCUITS DESCRIPTION

2.1. F/V converter

The circuit diagram of the F/V converter is shown on Fig. 1. It is built by selection among the available configurable analogue modules (CAMs) of the AN231E04, shown in Table 1. The differential input signal is applied between terminals 11 and 12 and average output voltage is obtained between terminals 15 and 16. After shaping of the input signal by a *Comparator1*, the *Differentiator1* detects the rising and falling edges of the shaped waveform in synchronism with the non-overlapping two phase clocks 1 (Phase 1) and 2 (Phase 2). The clocks 1 (Phase 1) and 2 are obtained by the master clock quartz stabilized signal, used for the proper work of the whole FPAA. The

differentiator produces short pulses with duration t_{os}, determined by the master clock frequency for all CAMs, and the polarity depending on the direction of change of the comparator's output voltage. When the output of the differentiator is equal to zero, the voltage steering switch *GainSwitch1* diverts differential voltage equal to $0V$ to the output of the gain stage; this is called the integration period. When the differentiator produces short pulse with negative value, the switch *GainSwitch1* diverts the voltage $K_2 \times U_{ref}$ (U_{ref} produces by the voltage source *Voltage1* CAM with fixed value equal to $+2V$) from the *SumFilter1* CAM to the output of the gain stage; this is called the reset period. The output low-pass filter implemented by *FilterBilinear1* CAM works as an averaging circuit ($f_{in} >> f_c$, where f_c is the corner frequency). As the frequency f_{in} of the input signal increases, the amount of charge injected into the averaging circuit increases proportionally.

The average output voltage $U_{o,av}$, obtained between terminals 17 and 18, that is proportional to the input frequency is given as

$$(1) \qquad U_{o,av} = \frac{1}{T_{in}} \int_0^{t_{os}} K_2 . U_{ref}\, dt = K_2 t_{os} U_{ref}\, f_{in},$$

where $T_{in} = 1/\, f_{in}$ is the period of the input signal.

Therefore, based on the formula (1), the sensitivity of the proposed F/V converter is obtained as

$$(2) \qquad K_V = K_2 t_{os} U_{ref}.$$

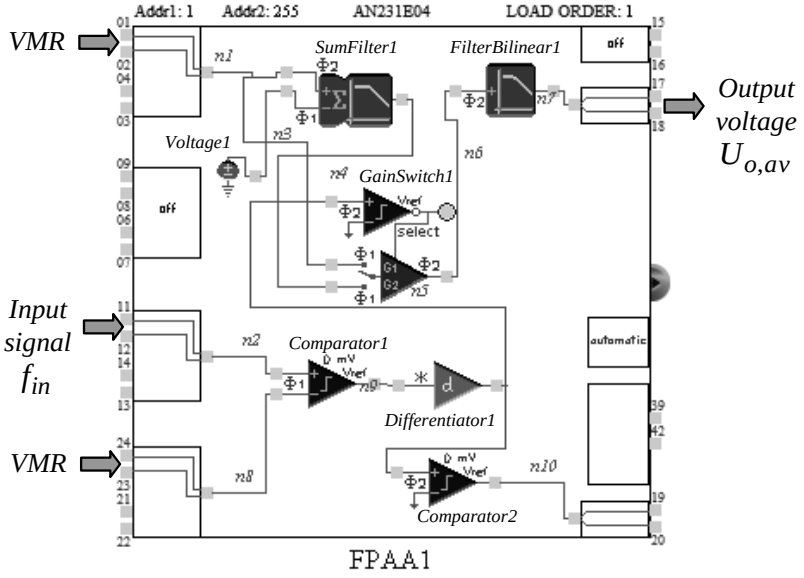
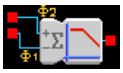
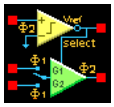
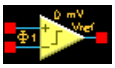
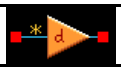
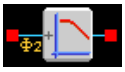
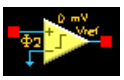


Figure 1. FPAA configuration of F/V converter.

The analysis of equation (2) shows that the change of the F/V converter's sensitivity can be accomplished in two ways. First, for a fixed value of t_{os}, for example equal to $20\mu s$ (at master clock frequency equal to $50kHz$), for modification of the transmission coefficient K_2 from 0.1 to 1 the sensitivity will vary from $4mV/kHz$ to $40mV/kHz$. Second, for a fixed value of the K_2, for example equal to 0.5 when change the clock frequency from $10kHz$ ($t_{os} = 100\mu s$) to $100kHz$ ($t_{os} = 10\mu s$) the sensitivity varies from $100mV/kHz$ to $10mV/kHz$. Moreover, the change of the coefficients of the CAMs can be implemented in the operating mode of the F/V converter.

Table 1. FPAA CAMs for F/V and V/F conversion.

Name		Options	Parameters	Clocks
SumFilter1		Output changes On: Phase 1 Input 1: non-inverting Input 2: inverting	Corner frequency [kHz]: 1 Gain1 (Upper input): K_1=1 Gain 2: (Lower input): K_2	Clock A: 50kHz (Clock 3)
Voltage1		Polarity: Positive (+2V)	-	-
GainSwitch1		Compare control to: Signal ground Select input 1 when: Control low Comparator sampling phase: Phase 2 Gain stage: half cycle	Gain1 (Upper input): 1.00 Gain 2: (Lower input): 1:00	Clock A: 50kHz (Clock 3)
Comparator1		Compare to: Dual input Input sampling: Phase 1 Output polarity: Non-inverted Hysteresis: 0mV	-	Clock A: 50kHz (Clock 3)
Differentiator1		-	Differentiation constant [us]: 1	Clock A: 50kHz (Clock 3)
FilterBilinear1		Filter type: Low pass Input sampling phase: Phase 2 Polarity: Non-inverted	Corner frequency [kHz]: 0.055 Gain: 1.00 C_{int1}=C_{int2}=C_{int}=7.9pF	Clock A: 50kHz (Clock 3)
Comparator2		Compare to: Signal ground Input sampling: Phase 2 Output polarity: Non-inverted Hysteresis: 0mV	-	Clock A: 50kHz (Clock 3)

The stability of the K_V in equation (2) is determined by the stability of the master clock frequency, which is derived from the crystal oscillator and the accuracy of the parameters of the CAMs, whose values are derived from the same clock frequency. Therefore, the variation of the sensitivity K_V of the proposed F/V converter will not cause changing of the nonlinearity error.

For normal operation of the F/V converter the inverting input (terminals 23 and 24) of the comparator and the input (terminals 01 and 02) of the *SumFilter1* are connected to voltage mid-rail (VMR) equal to $+1.5V$.

2.2. V/F converter

The circuit diagram of the V/F converter is shown on Fig. 2. As can be seen, for the implementation of the V/F converter is used the F/V converter shown on Fig. 1. For this purpose, the input voltage U_{in} is applied between terminals 01 and 02, terminals 11 and 12 are connected to a VMR and the voltage between terminals 17 and 18 is applied directly to the terminals 24 and 23. Thus it closes the positive feedback between the output of the averaging circuit and the inverting input of the *Comparator1*. The output differential signal with frequency f_{out} is formed by the *Comparator2* and can be obtained between terminals 19 and 20.

When the circuit operated as a V/F converter, the transformation from voltage to frequency is based on a comparison of the input voltage's value U_{in} to the internal voltage equal to $+2V$, implemented by *Voltage1* CAM.

The principle of operation of the circuit shown on Fig. 2 can be described as follows. At the beginning of a cycle, the input voltage is applied to the input of the *FilterBilinear1* and its output voltage decreases. This is the integration period. When the *FilterBilinear1* output voltage (terminals 17 and 18) crosses signal ground, the Comparator1 triggers a one-shot whose time period t_{os} is determined by the clock frequency. During this period, a voltage of $(U_{in} - K_2 U_{ref})$ is applied to the input of the *FilterBilinear1* and the output voltage starts to increase. This is the reset period of the circuit. After the reset period has ended, the circuit begins another integration period, and starts ramping downward again. The amount of time required to reach the comparator threshold is given as

(3) $$t_{\text{int}} = \frac{\Delta U_{17-18}}{\frac{dU_{17-18}}{dt}} = \frac{\frac{t_{os}}{C_{\text{int}}}(U_{in} - K_2 U_{ref})}{-\frac{U_{in}}{C_{\text{int}}}},$$

where the $C_{\text{int}} = 7.9\,pF$ is the internal capacitor of the *FilterBilinear1*.

The output frequency can be found as

(4) $$f_{out} = \frac{1}{t_{os} + t_{\text{int}}} = \frac{U_{in}}{t_{os} K_2 U_{ref}}.$$

The integration capacitor C_{int} has no effect on the transfer function, but merely determines the amplitude of the sawtooth signal out of the averaging circuit.

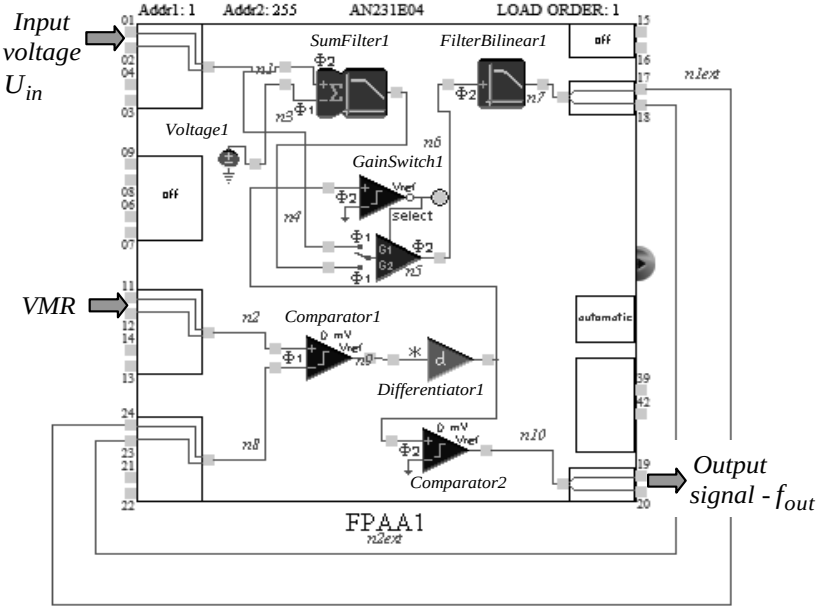


Figure 2. FPAA configuration of V/F converter.

From (4) for the instability of output frequency is found

(5) $$\frac{\Delta f_{out}}{f_{out}} = \frac{\Delta U_{in}}{U_{in}} - \frac{\Delta t_{os}}{t_{os}} - \frac{\Delta K_2}{K_2} - \frac{\Delta U_{ref}}{U_{ref}}.$$

The first term in formula (5) is the regulating effect. The second, third and fourth term reflect confusing influence in the circuit. The output frequency is linearly dependent on the input voltage. The transmission coefficient K_2 is interrelated with the corner frequency value of the CAM and the ratios of the two switched capacitors with values $C_{in} = C_{out} = 7.9\,pF$. The voltage U_{ref} is produced by a dc voltage source, which making a connection to the on-chip voltage references. There are no capacitors or dynamic switches. It produces a dc output so that the output is continuous and valid during the both phases of the clock signals [20].

According to the formula (4), it is concluded that the sensitivity of the proposed V/F converter is governed by the following equation

(6) $$K_f = 1/K_2 t_{os} U_{ref}.$$

Similar to equation (2), the analysis of equation (6) shows that the variation of the sensitivity can be achieved by changing the value of the K_2 or by changing the master clock frequency of the circuit.

III. EXPERIMENTAL RESULTS AND DISCUSSION

The experimental test that has been used for validation of the proposed converters is based on AN231K04-DVLP3 –Development board [20], which is built around the AN231E04 device. The power supply voltage of the AN231E04 is equal to +3.3*V*.

The measured average output voltages of the prototype V/F converter are plotted on Fig. 3 against the frequency of the output signal at two values of the conversion sensitivity. The conversion sensitivities K_{V1} and K_{V2} are obtained for gain K_2 equal to 0.5 and 1, respectively. The clock frequency of the circuit is chosen to be 50k*Hz*. However, for the frequency change from 0 to 25k*Hz* the average output voltage varies from 0 to 0.5 *V* (or 1*V*). In this operating range an error of less than 0.5% is achieved. In comparison with the F/V converters, presented in [5] and [7], the proposed converter has higher operating frequency and greater sensitivity. The F/V converters reported in [6] and [8] has a wider bandwidth (> 1M*Hz*) and good linearity, but the sensitivity is a fixed value and the modification of the electrical parameters required redesigning of the electronic circuits. Also the F/V converter presented in [6] can use only digital input signals, while the created F/V converter can operate with both analogue and digital signals.

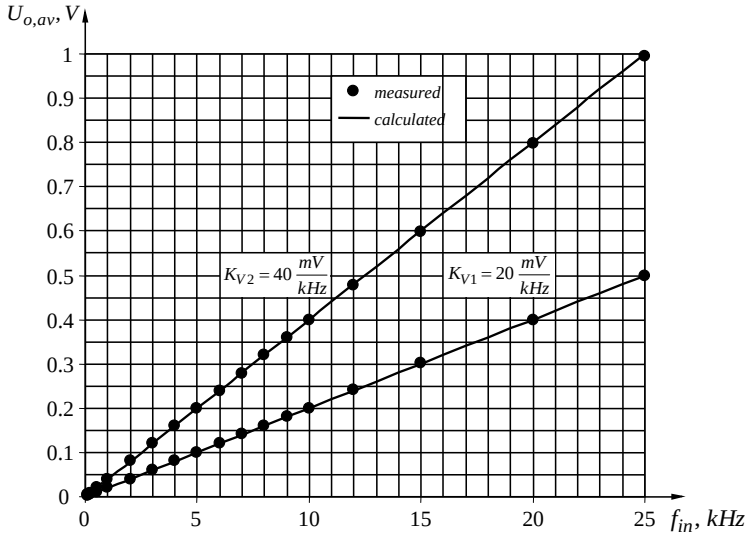


Figure 3. Average output voltage versus the frequency of the input signal at two values of the conversion sensitivity obtained by the F/V converter.

The oscillation frequency f_{out} of the prototype V/F converter against the input voltage is plotted on Fig. 4. The gain K_2 is set to 0.5 and 1, respectively. The clock frequency of the circuit is set equal to 50k*Hz*. When the input voltage changes from 0 to 0.4 *V* (or 0.8 *V*) the oscillation frequency varies from 0 to 20k*Hz*, the linearity error is again not higher than 0.5%. Thus, a figure of merit (FOM = sensitivity (M*Hz*) / error (%)) is equal to 0.1. The result is in a good agreement with the calculated by (4). Fig. 5 and 6 present the measured output waveform at the input voltage equal to $20mV$ and $400mV$, respectively. The clock frequency is set equal to $50kHz$ and the sensitivity is $K_f = 25kHz/V$. The output frequencies at these input voltages are 500.572*Hz* and 10.0013k*Hz*, respectively. For the both waveforms to channel 2 (CH2) the output signal from the inverting output is applied (terminal 19 of the FPAA) and to the channel 1 (CH1) the signal from the non-inverting output is applied (terminal 20 of the FPAA). The differential output signal (M) is the difference of the voltages applied to the both channels. Notably, that with variation of the input voltage the output frequency varies proportionally, as the pulse duration is unaffected ($t_{os} = 20\mu s$) and the error is less than 0.2%.

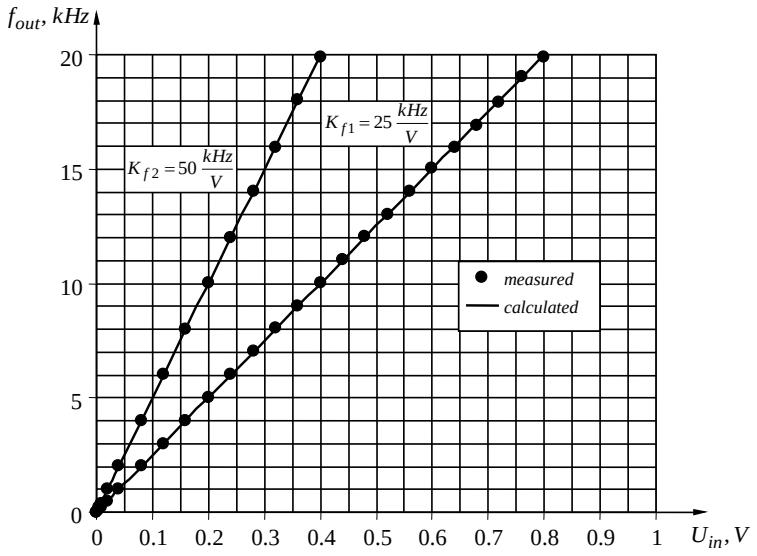


Figure 4. The oscillation frequency versus the input voltage at two values of the conversion sensitivity obtained by the V/F converter.

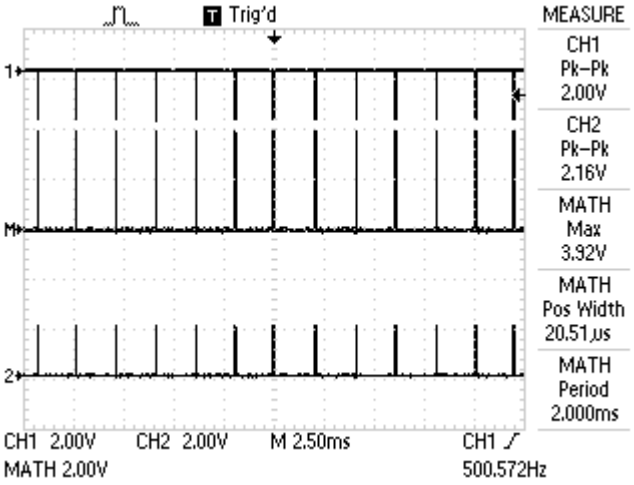


Figure 5. The output waveform of the V/F converter at $K_f = 25kHz/V$ and $U_{in} = 20mV$.

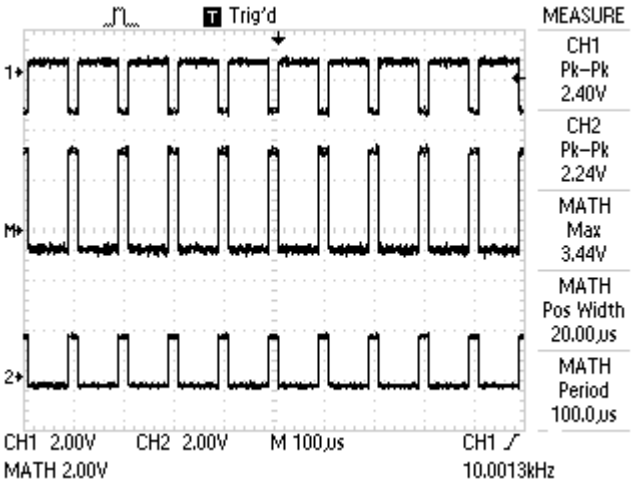


Figure 6. The output waveform of the V/F converter at $K_f = 25kHz/V$ and $U_{in} = 400mV$.

Table 2. Comparison with prior designs of V/F converters.

	This work	[5]	[9]	[10]	[11]	[13]	[14]	[15]
Technology	CMOS	CMOS	CMOS	CMOS	N/A	CMOS	CMOS	CMOS
Max. f_{out}	20k*Hz*	20k*Hz*	8k*Hz*	7k*Hz*	3.5k*Hz*	52.95M*Hz*	260k*Hz*	100M*Hz*
U_{in}	0-3*V*	0-1*V*	0.1-10*V*	0-3*V*	0-5*V*	0-0.9*V*	0-2*V*	0-10*V* in 100m*V* steps
Sensitivity	25…250k*Hz/V*	1k*Hz/V*	0.8k*Hz/V*	2k*Hz/V*	0.7k*Hz/V*	58M*Hz/V*	130k*Hz/V*	-
Error	≤ 0.5%	N/A	0.02%	1.95%	< 1%	< 8.5%	< 7%	within ±5ppm
FOM	0.05…0.5	N/A	0.04	0,00102	0.0007	6.28	0.019	-
Power at max f_{out}	65m*W*	N/A	N/A	95m*W*	N/A	0.218m*W*	N/A	N/A
Year	2014	1986	1997	2004	2005	2007	2010	2013

The measured results compared with several prior works are summarized in Table 2. In comparison with the V/F converter, presented in [9], the proposed V/F converter has higher error (≤ 0.5%), but the maximum frequency is higher and the sensitivity with significantly greater value can be obtained. The V/F converter presented in [13] is characterized by higher operating frequency and sensitivity, but the error accept relatively large value (equal to 8.5%), which may affects to the conversion of weak signals from various sensors. Obviously, the error for the converters reported in [5], [10], [11] and [14] are higher than the proposed V/F converter, while the input voltage range for the most circuits is from 0 to several volts. For V/F converter reported in [15] the operating frequency bandwidth is higher and the error is relatively small (within ±5ppm), but the sensitivity is with fixed value and under a step equal to 100m*V* are obtained 100 discrete values for the frequency of the output signal in the range up to 100M*Hz*.

IV. CONCLUSION AND FUTURE WORK

In this paper a differential F/V and V/F converters by using of a charge-balance method was proposed. The selected FPAA is an Anadigm AN231E04, where the mixed-signal processing is implemented. Moreover, for the created V/F converter the linearity error not exceeding 0.5% was achieved at sensitivity changes from 25k*Hz/V* to 250k*Hz/V*. In comparison with prior works the variation of the sensitivity depending on the parameters of the input signal could be done by changing the parameters of configurable analogue blocks without changing the structure of the circuit or without adding of external passive components. The stability of the sensitivity was determined by the stability of the master clock frequency, which is derived from the external quartz crystal oscillator and the accuracy of the parameters of the configurable blocks, whose values are derived from the same clock frequency. Therefore, these converters can be used as flexible mixed-signal building blocks in extracting weak differential signals from transducers and other signal sources.
Future work will be focused on implementation of the proposed F/V and V/F converters in programmable systems-on-chips (PSoCs), which combine analogue and digital functions. Furthermore, the development of the proposed electronic circuits will be oriented to modelling and design of PLL-based frequency synthesizers and synchronizers.

REFERENCES

[1]. Kester, W., & Bryant J. (2004). *Analog-digital conversion*, USA Analog Devices.
[2]. Paiva, M. (2002) "Voltage-to-frequency/frequency-to-voltage converter (AN795)". Retrieved from Microchip website: http://ww1.microchip.com/downloads/ en/appnotes/00795a.pdf.
[3]. Bryant J. (1989) "Voltage-to-frequency converters (AN-361)". Retrieved from Analog Devices website: http://www.analog.com/static/imported-files/application_notes/84860375AN361.pdf

[4]. Klonowski, P. (1990) "Analog-to-digital conversion using voltage-to-frequency converters (AN-276)". Retrieved from Analog Devices website: http://www.analog.com/static/imported-files/application_notes/185321581AN276.pdf.
[5]. Matsumoto, H., & Fujiwara, K. (1986) "Switched- capacitor frequency-to-voltage and voltage-to-frequency converters", *IEEE Transactions on Circuits and Systems*, Vol. 33 (8), pp 836–838.
[6]. Djemouai, A., Sawan, M., & Slamani, M. (2001) "New frequency-locked loop based on CMOS frequency-to-voltage converter: design and implementation", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol. 48 (5), pp 441–449.
[7]. Gupta, K., Bhardwaj, M., & Singh, B. (2012) "Design and analysis of CMOS frequency to voltage converter using 0.35μm technology", *International Journal of Scientific & Engineering Research*, Vol. 3 (5), pp 1–9. Retrieved from www.ijser.org/researchpaper%5CDesign-and-Analysis-of-CMOS-Frequency- to-Voltage-Converter.pdf.
[8]. Singh, M., & Sahu P.P. (2013) "A wideband linear sinusoidal frequency to voltage converter with fast response time", Procedia Engineering, Vol. 64, pp 26-35.
[9]. Trofimenkoff, F.N., Sabouri, F., Jichang, Qin & Haslett, J.W. (1997) "A square-rooting voltage-to-frequency converter", *IEEE Transactions on Instrumentation and Measurement*, Vol. 46 (5), pp 1208–1211.
[10]. Yakimov, P., Manolov, E., & Hristov, M. (2004) "Design and implementation of a V-f converter using FPAA", *27th International Spring Seminar on Electronics Technology: Meeting the Challenges of Electronics Technology Progress*, Vol. 1, pp 126-129.
[11]. Stork, M. (2005) "Sigma-delta voltage to frequency converter with phase modulapossibility", *Turkish Journal of Electrical Engineering & Computer Sciences*, Vol. 13 (1), pp 61–67.
[12]. Wang, C.-C, Lee, T.-Je, Li C.-C. & Hu, R. (2006) "An all-MOS high-linearity voltage-to-frequency converter chip with 520-kHz/V sensitivity", *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 53 (8), pp 744–747.
[13]. Wang, C.-C, Lee, T.-Je, Li C.-C. & Hu, R. (2007) "Voltage-to-frequency converter with high sensitivity using all-MOS voltage window comparator", *Microelectronics Journal*, Vol. 38 (2), pp 197–202.
[14]. Valero, M.R., Aldea, C., Celma, S. Calvo, B., & Medrano, N. (2010) "A CMOS differential voltage-to-frequency converter with temperature drift compensation", 2010 *European Workshop on Smart Objects: Systems, Technologies and Applications (RFID Sys Tech)*, Ciudad, Spain.
[15]. Hino, R., Clement, J. M., & Fajardo, P. (2013) "A 100MHz voltage to frequency converter", *Journal of Physics: Conference Series*, Vol. 425 (21), pp 1-4.
[16]. Lattice ispPAC-POWR1014/A (2012). Retrieved from http://www.latticesemi.com/ documents/DS1018.pdf.
[17]. Cypress PSoC® Mixed-Signal Array (2012). Retrieved from http://www.cypress.com
[18]. Zetex TRAC-S2 (2012), Retrieved from http://www.datasheetcatalog.org/datasheets/ 208/306841_DS.pdf.
[19]. Anadigm dpASP (2013). Retrieved from http://www.anadigm.com/dpasp.asp
[20]. AN231K04-DVLP3 – AnadigmApex Development Board (2013). Retrieved from http://www.anadigm.com/_doc/UM231000-K001.pdf.

AUTHOR

Ivailo Pandiev received his M.Sc and Ph.D. degrees in Electronic Engineering from Technical University of Sofia (TU-Sofia), Bulgaria, in 1996 and 2000, respectively. He is currently an associate professor in the Department of Electronics at the TU-Sofia. His research interests include analysis and design of analogue and mixed-signal circuits and systems.