DESIGN OF ADDERS USING QCA

[1]Kodam. Latha, [2]M. Nanda Maharshi
[1]Assistant Professor, Department of ECE,
Vardhaman College of Engineering, Hyderabad India
[2] Research Student, Department of ECE,
Vardhaman College of Engineering, Hyderabad, India

ABSTRACT
Quantum-dot cellular automata (QCA) is considered as an advanced technology compared to complimentary metal-oxide-semiconductor (CMOS) due to QCA's merits.Many logical circuits are designed using QCA which consume low power.Therfore our interest is on desiging of adders using QCA. In this paper we present a number of new results on adders.Thus we design adders and detailed simulation using QCAD designer is presented.The performance of proposed adder gives the better Delay performance compared to Ripple carry adder(RCA).Thus we show that Brent-kung Adder has lower Delathen most of the proposed advanced adders.

Keywords: *Majority gate, Quantum-dot cellular Automata (QCA), Area, Brent Kung Adder, Cell count, Ripple Carry Adder*

I. INTRODUCTION

Quantum Dot cellular Automata (QCA) donot use transistors.QCA design addresses the issue of device density and interconnection.The basic element of QCA is a quantum cell.Each quantum cell has electrons in them.where electron transimission occurs on the columbic interaction of the electrons.QCA is an advanced research program and efforts are made to reduce the complexity of the circuits.When featured size is reduced to nanometers than Quantum effects such as Tunneling takes place[1].QCA circuits can be directly obtained from conventional designs with addition of special clocking system.This provides very easy transmission of conventional circuits to get transformed into QCA structures.

QCA structures are designed as an array of quantum cells.where every cell has electrons in them where electrostatic interaction with its neighbouring cells takes place.QCA uses a new technique for computation.It uses polarization effect rather than conventional current for the transmission of information which contains the digital information.Thus a cell is responsible for the transfer of information throughtout the circuit.The basic operators used in QCA are three input majority gates and invertor.This study proposes the design of different types of adders.Hence the proposed design is used to minimize the area and complexity.

This paper is organised as fallows begining with the Introduction of QCA in Section (I).Design Architecture of QCA in Section (II).Generalization of different adders in Section (III) and then Simulation Results of that adders using QCA in Section (IV) and Finally Future Work in Section (V)

II. QCA DESIGN ARCHITECTURE

2.1 Basics of QCA:

The basic elements of QCA are QCA cell, Majority gate and Invertor.These is important elements.In QCA cell each cell is having four quantum dots and is having two free electrons.The locations of the electrons determine the binary states.Fig.1 shows the QCA cell diagram.

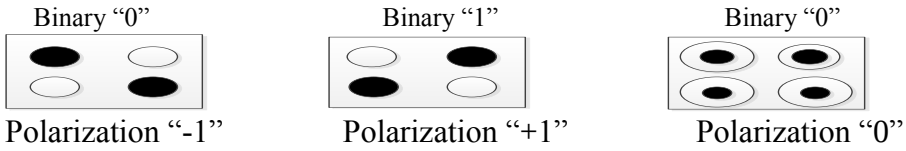

Fig.1 QCA Cell Polarization.

2.2 QCA Cell:

A quantum-dot cellular automata (QCA) is a square nanostructure of electron wells having free electrons.Each cell has four quantum dots[2].The four dots are located in the four corners .The cell can be charged with two free electrons.By using the clocking mechanism,the electrons tunnel to proper location during the clock transition.Thus there exist two equivalent energetically arrangements of the two electrons in the QCA cell as shown in Fig.1.These two arrangements can represent logic 1 and logic 0 respectively so that binary information can be encoded.Invertor is represented in Fig.2 and Majority gate in Fig.3.

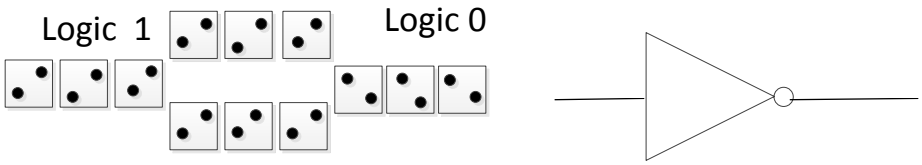

Fig.2. Invertor

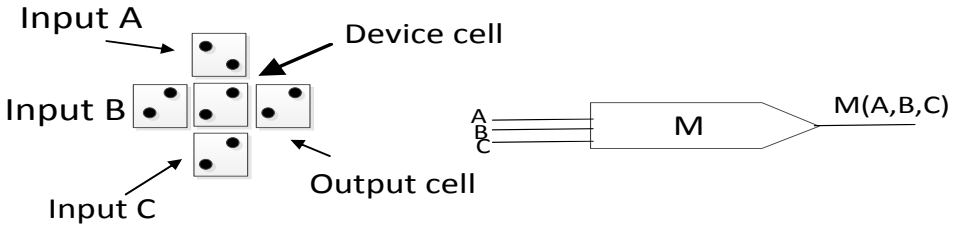

Fig.3. Majority gate

A QCA design permits two options for crossover, termed coplanar crossover and multilayer crossover. While the coplanar crossover uses only one layer but involves usage of two cell types (termed regular and rotated), the multilayer crossover uses more than one layer of cells (analogous to multiple metal layers in a conventional IC). The multilayer crossover is used in this paper for wire crossings since we can effectively cross signals over on another layer and the extra layers of QCA can be used as active components of the circuit.Further, multilayer QCA circuits can potentially consume much less area as compared to planar circuits.Moreover, some studies indicate that coplanar crossover is difficult to fabricate in the molecular implementation.

2.3 QCA Clocking Scheme:

QCA circuits use clock signals for transimison of signals and clock signals control the QCA circuits.It has four different phases[3].The four diferent phases are switch,hold,release and relax.Due to the tunnel barrier between the dots the clock signal stops tunneling and at the same time allowing the electrons to tunnel in the other clock phase Fig.4. shows the clocking scheme when an individual cell is affected with clock signal.During the switch phase electron tunneling is stoped as the tunnel barrier between the dots rising,electrons thus tunneling is stoped and due to the polarization of its input the electron in the cell become localized Switching occurs by refreshing the it's state.

During the hold phase as the barrier remains high thus no electron tunneling takesplace.The polarized cells is latched.Therefore,using these cells as the input to he next clock zone.During Release phase the electrons becomes free and the cell starts to lose it's polarizationdue to the lowering of electron barrier.During the relax phase,the barriers are low,the electrons are free to tunnel and delocalize

themselves and the cells have no polarization i.e P=0.Thus to control data flow four identical clock signals shifted in phase by 90 are applied to adjacent groups of cells.

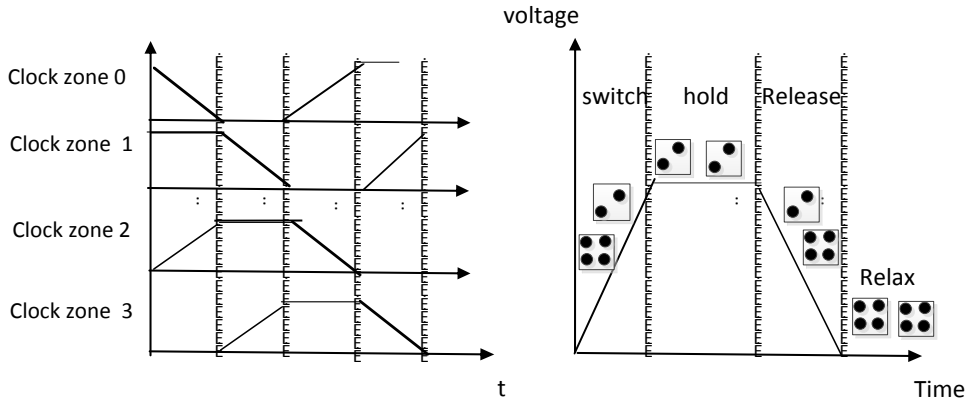

Fig.4. QCA clock zones and QCA clock with four phases.

2.4 Simulation Tool

A QCAD Designer is a well known simulation tool used to create QCA circuits and verifying it's functionality.This tool provides two simulation engines they are bistable engine and coherence vector engine[4].By performing simulation,the bistable is more accurate than the coherence vector engine usually produces more acccurate results than the bistable engine[5].Hence,all the designs presented in this paper were simulated by employing the coherence vector engine and its parameter values.The diameter of the quantum dot is 5nm,the cell size is 18*18nm and the cell distance is 2nm.

III. GENERALIZATION OF DIFFERENT ADDERS

3.1 Ripple Carry Adder (RCA):

The ripple carry adder (RCA) provides a slow and efficient method for adding two binary numbers.The comparitive study of these adders gives better scope thus by cascading n-full adder we get n-bit RCA [6].For high speed operation two types of full adders are used [13].The carryout of Jth full adder is used as the carry in the (J+1)th full adder as shown in the Fig.5..The carry propagation delay for each full adder is the times from the application of the input carry until the output carry is valid.

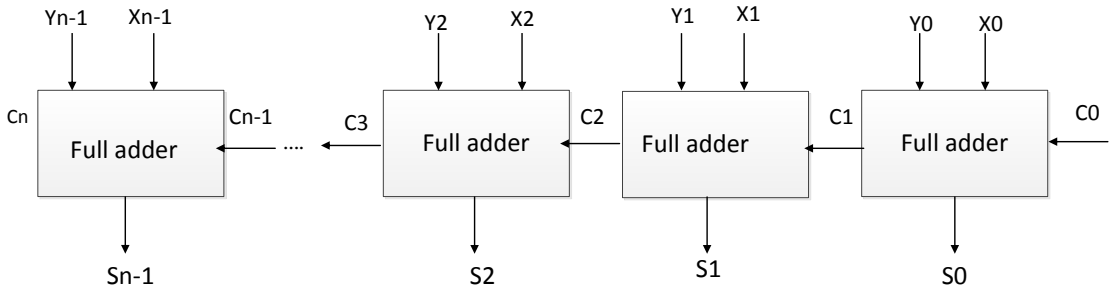

Fig.5. n-bit Ripple Carry Adder

3.2 Brent Kung Adders:

The Brent kung adder uses an associative operator called as dot operator (0).The dot operator implies the associative property.The associative property is given as a.(b.c)=(a.b).c
By applying these conditions combining "n" arguments using the dot operator can be executed.Thus this property can be applied to n-bit adders [6]. The dot operator establishes the relationship between the two tuples(g,p) where "0" is the fundamental carry operator.In particular for radix-2 operation the

operator "0" is a function that takes two inputs (g,j,pj)and (gi,pi) and produces output (g{,p{}}) at each bit the carry is given by

$$C=GjcPij-0+0.c\_1$$

Where c_1 is the primary carry input if there is no primary carry input then Cj is simply C this is illustrated in fig(3b) filled circles implement the fundamental carry equation empty circles are buffers and empty squares compute first order propagate and generate signals the number of stages to implement a Brent kung adder is 2.[log2n].Fig.6 shows the representation of Brent kung adder and equations used in calculating[8].

3.2.1. Advantages:

1. Maximum logic depth in PP adders (implies longer calculation time).
2. Minimum number of nodes (implies minimum area)

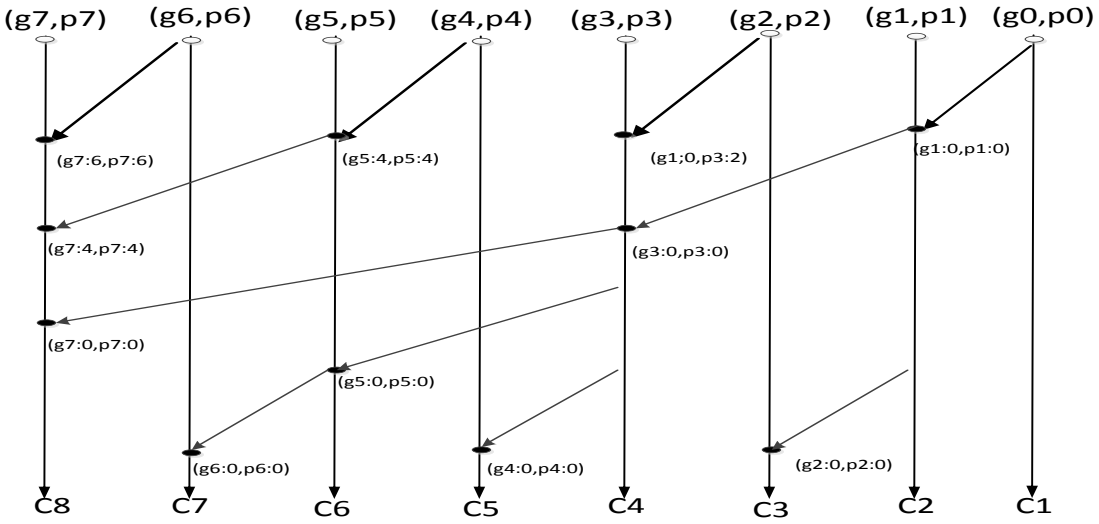

Fig.6. Brent kung adder representation.

3.3 Carry Look Ahead Adder:

The carry lookahead adder(CLA) has a regular structure.It achieves high speed.In this paper we design a 4 bit CLA.This design employes 4 bit slices for the lookahead logic[9].These adders avoid feedback signals that are used in regular CMOS.By the nature of QCA cells the carry lookahead adder is pipelined.In the PG block we have a generated output that indicates that a carry is "generated "at bit position and a propagate output that indicates that a carry entering bit position will propogate to the next bit position.Thus these are used to produce all the carries in parallel at the successive blocks.Due to the pipeline diagram all sum signals are available at the same clock period.In Fig.7 we represent QCA design of CLA.

$$Ci=Gi+Pi.C\_1$$

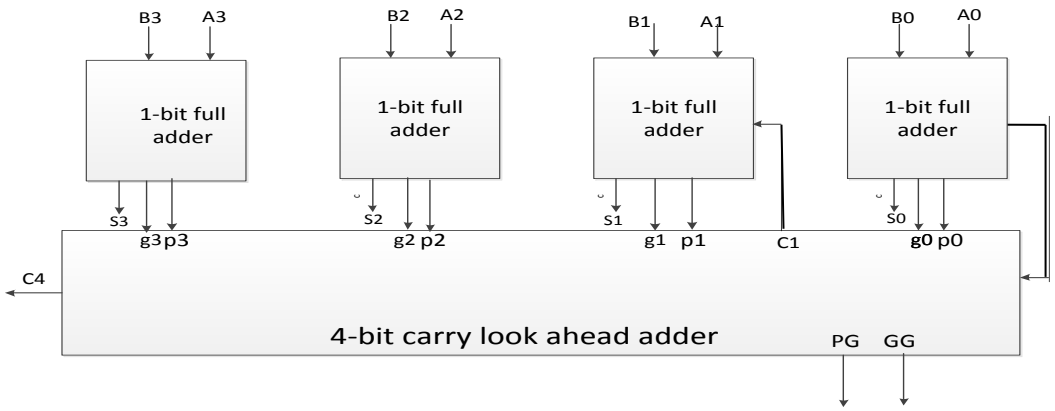

Fig.7. Carry look ahead adder using QCA

3.4. Kogge-Stone Adder:

The number of majoriy gates required for an n-nbit koggee-stone adder is given by

$$I(n)=n(3\log 2n-1)+5.$$

The computation of carries of an n-bit koggee-stone adder requires log2n stages.The number of majority gates rquired for a n-bit koggee–stone adder is also obtained via recursive formulation[10].The numner of majority gates required for carries from n2+1 to n.Each stage in kogge-stone requires n2 assosiative operations.Except last stage.Each assosiative operation requires only three majority gates.In last stage each associative operation requires only two majority gates.Fig.8.shows 8 –bit Koggestone adder.

3.4.1. Advantage:

1. The Kogge-Stone adder has Low depth and High node count (implies more area).
2. Minimal fan-out of 1 at each node (implies faster performance

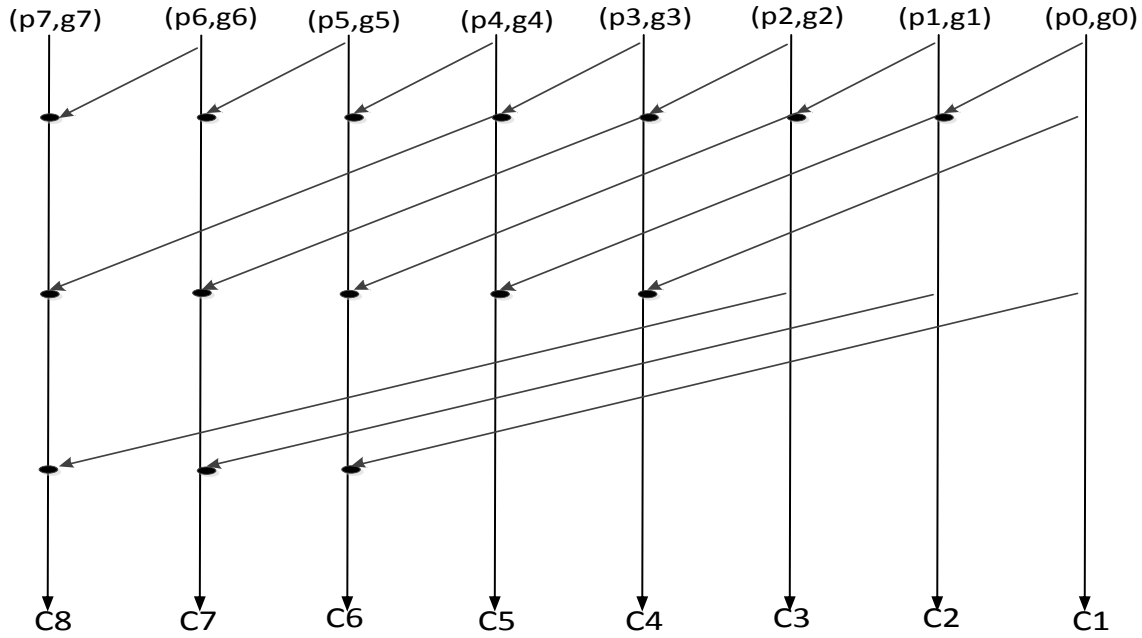

Fig.8. Kogge-stone adder.

3.5 Ladner-Fisher Adder:

The number of majoriy gates required for an n-nbit koggee-stone adder is given by

$$I(n) = n/2(3 \log 2\ n + 4) +2$$

The computation of carries of an n-bit Ladner Fisher adder requires log2n stages[6].The number of majority gates rquired for a n-bit Lnder-Stone adder is also obtained via recursive formulation.Each stage in Lander-Fisher requires n/2[logn] assosiative operations.Fig.9.shows the 8-bit Lander-Fisher adder[11].

3.5.1. Advantage:

1. Low depth
2. High fan-out nodes

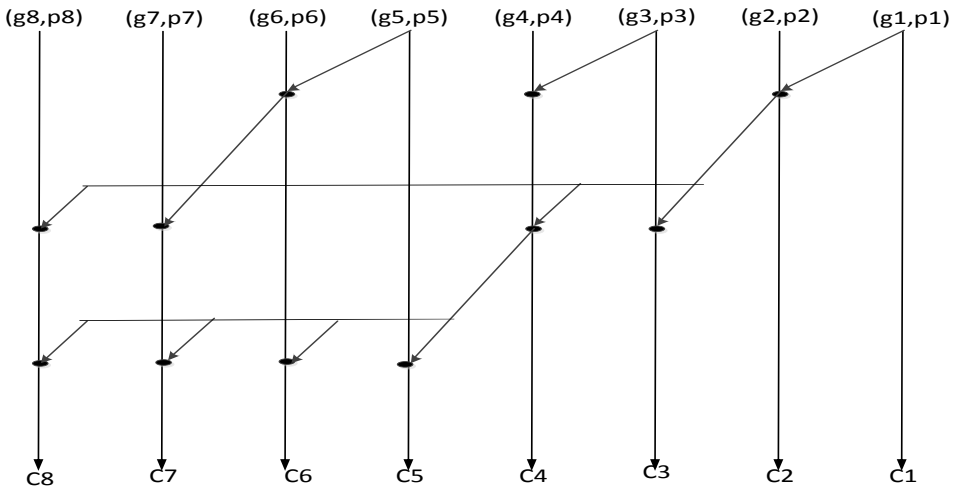

Fig.9. Shows the 8-bit Lander-Fisher adder.

IV. QCA IMPLEMENTATION AND TABLES

The prefix operation has three stages:
1. Pre caculation f pi,gi in each stage.
2. Calculation of carry ci for each stage.
3. Combine ci,pi to generate the sum bit and the carry bit "Si" and Cout

Operational parameters of a prefix adders are very important as these help in the designing of the adders in the QCA.Thus the operational parameers such as number of majority gates,number of levels,number of associative operations…etc play a key role in designing the QCA adders and also the clocking scgheme plays a key role in simulation of the circuit

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4.1 Implementation of Adders using QCA:

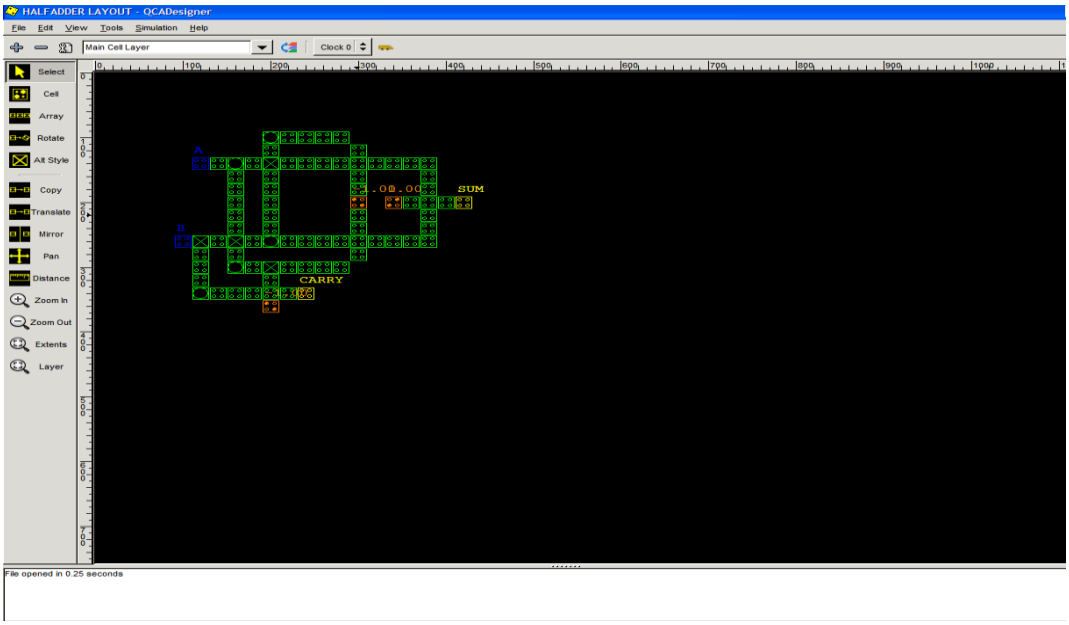

Fig.10 Design of Half Adder using QCA

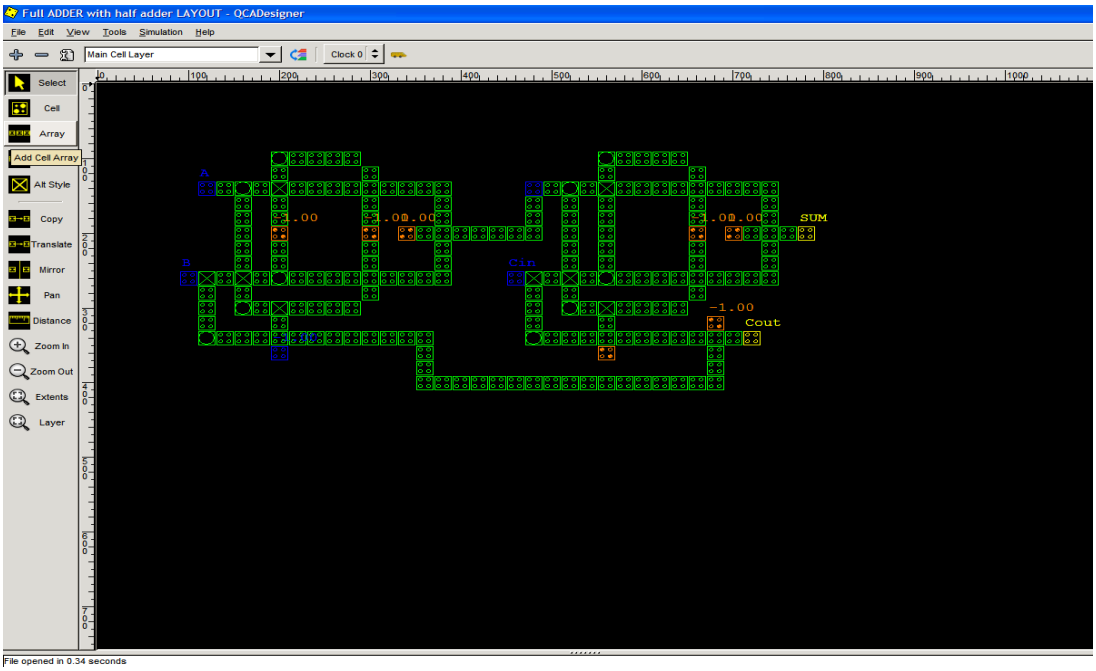

Fig.11. Design of Full adder using two half adder in QCA.

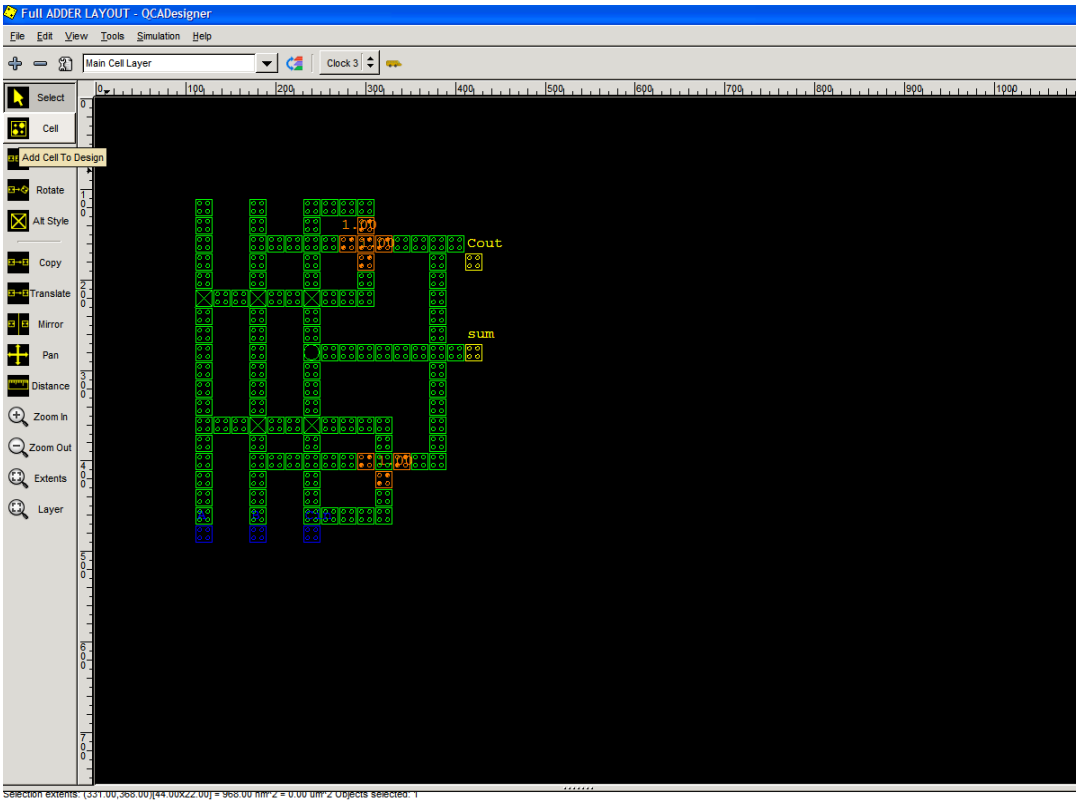

Fig.12. Design of Full adder using QCA.

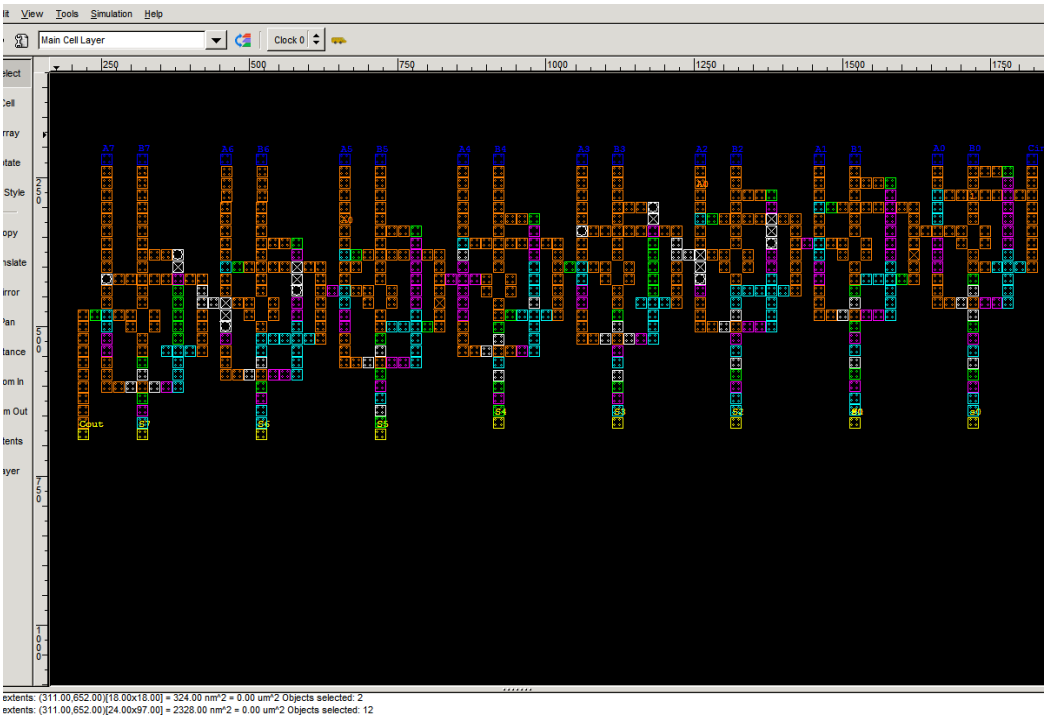

Fig.13. Design of 8-bit Ripple Carry Adder using QCA**.**

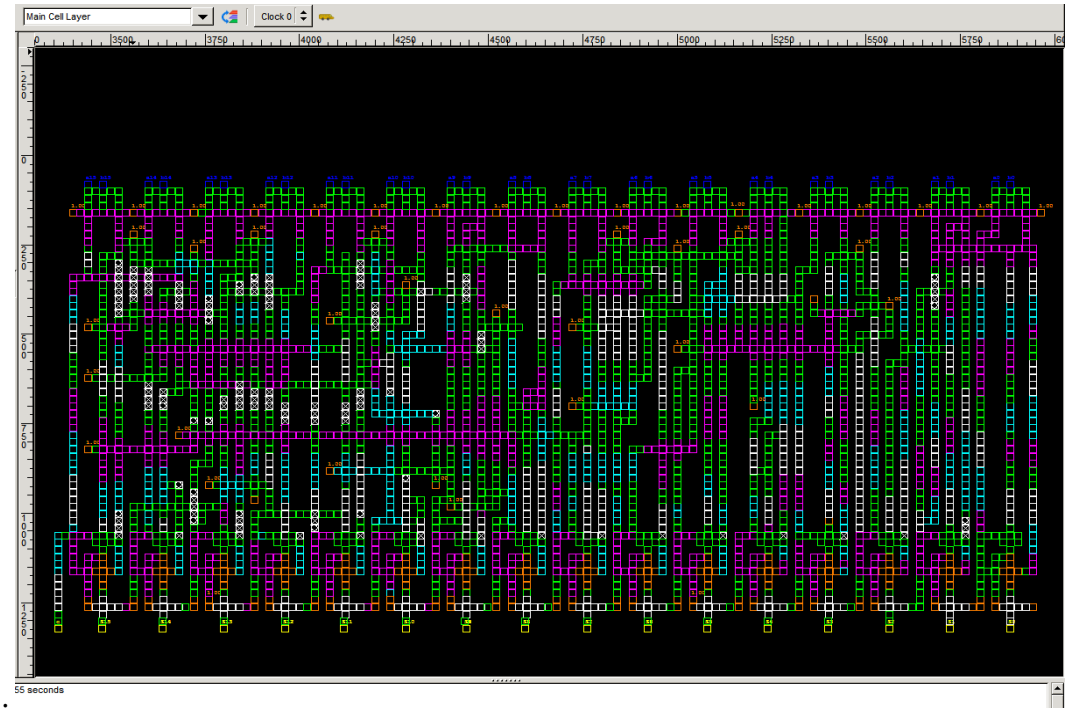

Fig.14. Design of 16-bit Brent Kung Adder using QCA.

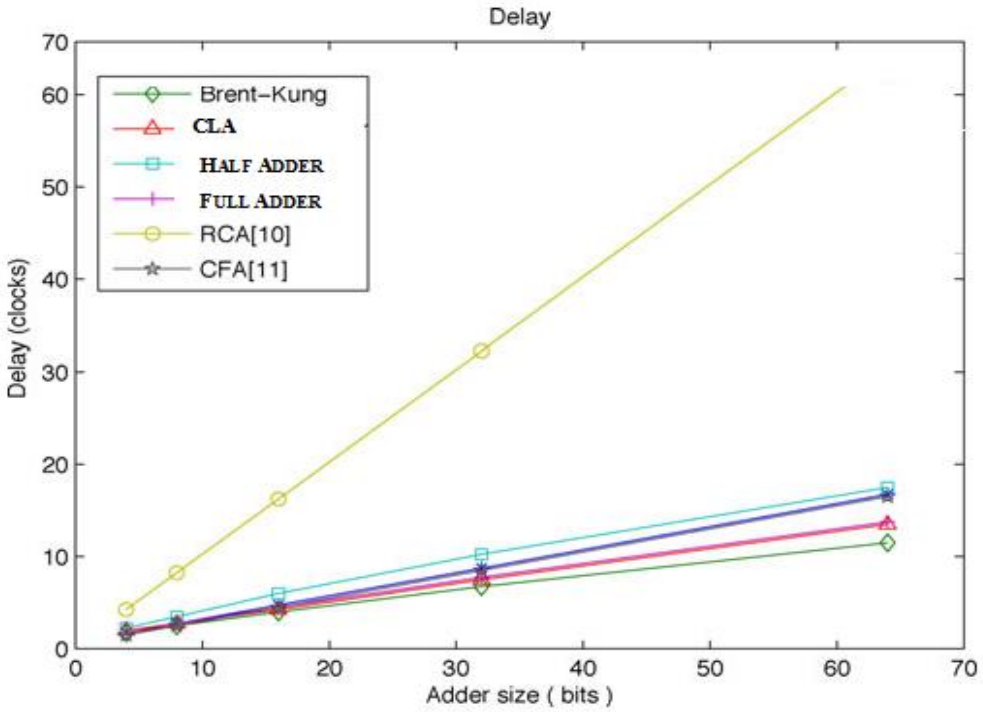

Fig.15 Graph comparing different adders.

4.2 Simulation Results:

Table.1. shows the details of Cell count, delay, area of the above circuits.

Adder name	Number of cells	Area (nm x nm)	Number of clock phases
Ripple carry Adder	339 cells	820 x 310	7
Half Adder	77 cells	297 x 280	4
Full Adder	122 cells	381 x 300	4
Carry look ahead adder	6508 cells	650 x 900	6
Brent-kung Adder	12530 cells	650 x 800	7

V. CONCLUSION

In this paper, we have considered primitives in QCA and have presented an efficient QCA design for an *n*-bit ripple carry adder and various prefix adders.We have also shown that the Brent–Kung adder has lower delay than all other adder designs Further, the Brent–Kung adder performs best among the prefix adders in terms of delay.

VI. FUTURE SCOPE

As we dealt with only Adders these are fundamental requirements of logic gates once logic gates are designed we can design all different kind of circuits with QCA-LG the design flow for QCA technology is almost complete. Combinational VHLD/Verilog circuits can be mapped into logic netlists with existing synthesis tools. These netlists can be transformed into QCADesigner compatible layout using QCA-LG, and validated by physical simulation.QCA-LG is still under development.

REFERENCES

[1]. G. W. Hanson, Fundamentals of Nanoelectronics. Englewood Cliffs, NJ: Prentice-Hall, 2008.
[2]. Cho and Swartzlander, 2007; Walus etal., 2004b; Reza and Vafaei 2008
[3]. H. Cho and E. E. Swartzlander, "Adder designs and analyses for quantumdot cellular automata," IEEE Trans. Nanotechnol., vol. 6, no. 3, pp. 374–383, May

[4]. Uni. of Calgary ATIPS Laboratory. Qcadesigner on www, http://www.qcadesigner.ca. World Wide Web, 2007.
[5]. K. Walus and G. Jullien. Design tools for an emerging soc technology: quantum-dot cellular automata. Proceedings of the IEEE, 94(6):1225–1244, June 2006.
[6]. R. Zhang, K. Walus, W. Wang, and G. Jullien. Performance comparison of quantum-dot cellular automata adders. In IEEE International Symposium on Circuits and Systems, 2005, pages 2522–2526, 2005
[7]. K. Kim, K. Wu, and R. Karri. The robust qca adder designs using composable qca building blocks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 26(1):176–183, January 2007.
[8]. Brent Kung, "A regular Layout for Parallel Adders", IEEE, 1982
[9]. Beaumont-Smith, Cheng-Chew Lim, "Parallel Prefix Adder Design", IEEE, 2001
[10]. Kogge Stone, "A Parallel Algorithm for the Efficient solution of a General Class of Recurrence equations", IEEE, 1973.
[11]. Ladner Fischer, "Parallel Prefix Computation", ACM, 1980.
[12]. Venkataramani, P., Srivastava, S., Bhanja, S., 2008. Sequential Circuit Design in Quantum Dot Cellular Automata. 8th IEEE Conf. on Nanotechnology, p.534-537. [doi:10.1109/NANO.2008.159].
[13]. H. Cho and E. Swartzlander. Pipelined carry lookahead adder design in quantum-dot cellular automata. In Conference Record of the Thirty-Ninth Asilomar Conference on Signals, Systems and Computers, 2005, pages 1191–1195,2005.
[14]. S. Srivastava, S. Sarkar and S. Bhanja, "Estimation of upper bound of power dissipation in QCA circuits," IEEE Trans. Nanotechnol., vol. 8,no. 1, pp. 116–127, Jan. 2009.
[15]. S. Bhanja and S. Sarkar, "Probabilistic modeling of QCA circuits using Bayesian networks," IEEE Trans. Nanotechnol., vol. 5, no. 6, pp. 657–670, Nov. 2006.
[16]. A. Chaudhary, D. Z. Chen, X. S. Hu, M. T. Niemier, R. Ravichandran and K.Whitton, "Fabricatable interconnect and molecular QCA circuits,"IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 26, no. 11,pp. 1978–1991, Nov. 2007.

AUTHORS

Nanda Maharshi received B.Tech degree from Sri Sai Jyothi Engineering College,Hyderabad,India in 2010 and I am Presently Pursueing Master degree from Vardhaman College of Engineering,Hyderabad,India. My areas of interest are on Optical Technology.

Latha Kodam received M.Tech from VAAGDEVI College of Engineering, Warangal in 2011 and B.Tech from Mother Theresa College of Engineering and Technology in 2008 and presently working as Assistant Professor in Vardhaman College of Engineering.