4-BIT RCA FOR LOW POWER APPLICATIONS

Riya Garg, Suman Nehra and B. P. Singh
Department of Electronics and Communication,
FET-MITS (Deemed University), Lakshmangarh, India

ABSTRACT

This paper presents low power 4-bit ripple carry adder (RCA) using 1-bit full adder. The main objective of this paper is to provide low power solution for VLSI designers. All pre-layout and post-layout simulations have been performed at 45nm technology on Tanner EDA tool version 12.6. An Adder is one of the significant hardware blocks in most digital systems such as digital signal processors and microprocessors etc. Therefore, binary adders are basic building blocks in VLSI circuits and efficient implementation of these adders affects the performance of entire system.

KEYWORDS: *2T (2 transistors), 3T, 8T, RCA, PDP.*

I. INTRODUCTION

Addition is the fundamental arithmetic operations in the VLSI systems such as microprocessors and digital signal processing (DSP) systems. Most of such arithmetic operations are based on the adder cells. The adder cell not only lies in the critical path, but also consumes significant power. In mobile systems and portable computers, there is only limited amount of battery power. So we must pay more attention to the low power circuit design to increase the battery life. Most of all, the low-voltage, low power design is our particular concern because the power consumption is proportional to the square of supply voltage. Demand for power sensitive, high speed, small area and low cost designs are increasing every day [1]. This tremendous demand is due to fast growth of battery-operated portable applications such as personal computing devices (portable computers and real time audio and video based multimedia products), wireless communication systems (personal digital assistants and mobile phones), medical applications and other portable devices.

With the development of CMOS technology, the minimum gate length of transistors continues to decrease, and the characteristic frequency also will be rising. With the lowering of threshold voltage in ultra deep submicron technology, supply voltage scaling is among the most efficient ways to reduce the power consumption of digital circuitry due to the quadratic relationship between dynamic power consumption and supply voltage [2]. This technique will however degrade the performance due to the inverse relationship between circuit delay and power consumption. Power-delay product (PDP) is a quantitative measure of the efficiency of the trade off between power consumption and delay and is particularly important when low power operation is needed.

The role of full adder in arithmetic circuits can be classified into two categories. The first category involves chain structured such as ripple carry adders (RCA) and array multipliers. In these applications, the critical path often traverses from the carry-in to the carry-out of the full adders. It is demanded that the generation of the carry-out signal is fast. Otherwise, the slower carry-out generation will not only extend the worst case delay, but also create more glitches in the later stages, hence, dissipate more power. The other category involves the tree structured, which is frequently used in multipliers [3]. Full adders in these applications form a tree of several layers to compress the partial products to a carry-saved number before a final carry propagation adder converts it to a normal binary number. Hence, addition is a fundamental operation in digital systems and can significantly influence the overall performance of the system [4]. For this reason, low power and high speed adders are highly desirable.

The paper is organized as follows: Section II describes an overview of 1-bit full adder and 4-bit RCA. Section III introduces the 4-bit RCA using existing and proposed 1-bit full adder. Simulation results and their comparisons are included in Section IV and finally Section V concluded the paper.

II. ADDERS

2.1. One bit full adder

A 1-bit full adder is a combinational circuit that performs the arithmetic sum of three bits. It consists of three inputs a, b and c_{in} and two outputs sum and carry as shown in Figure 1 [5]. Expressions for sum and carry are;

Figure 1. Block diagram of 1-bit full adder

$$sum = a \oplus b \oplus c_{in} \quad (1)$$

$$carry = (a \oplus b)c_{in} + ab \quad (2)$$

The block diagram of 1-bit full adder is used as a basic building block in many VLSI circuits and systems such as comparators, parity checkers, ripple carry adder (RCA), carry skip adder, carry select adder, array multiplier, 4:2 compressor and microprocessors etc. Thus, by enhancing the performance of 1-bit full adder, the overall performance of the system will increase.

2.2. Ripple Carry Adder (RCA)

A ripple carry adder (RCA) is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with 1-bit full adders connected in cascade, with the carry output from each full adder connected to the carry input of the next full adder in the chain.

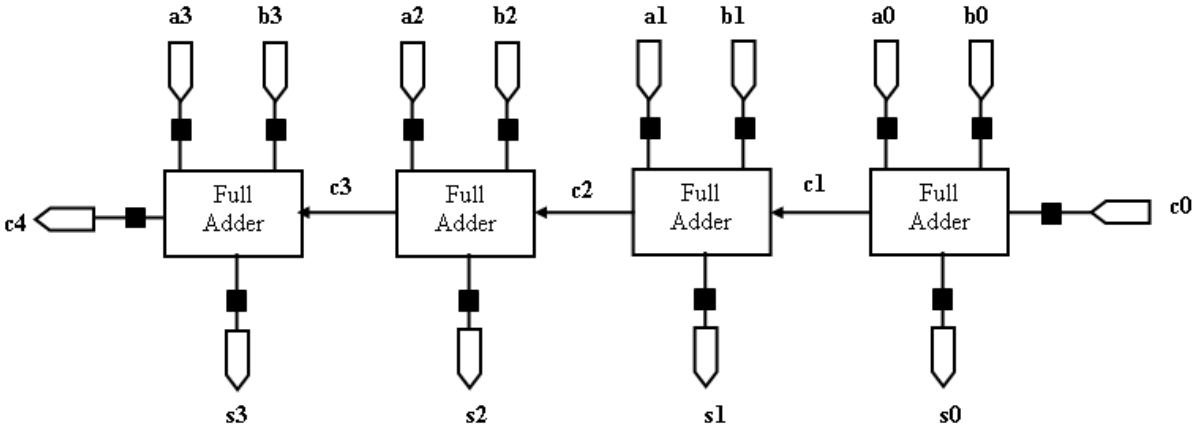

Figure 2. Block diagram 4-bit ripple carry adder

An n-bit ripple carry adder requires 'n' numbers of full adders with the carry output from each full adder connected to the carry input of the next full adder [5], [6]. Block diagram of 4-bit ripple carry adder is shown in Figure 2. Notice that the input is from the right side because the first cell traditionally represents the least significant bit (LSB). Bits a0 and b0 represent the least significant bits of the numbers to be added and c0 represents the carry-in bit. The sum output is represented by the bits s0-s3. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any full adder stage is not valid until the carry in of that stage occurs. Thus, the main problem with this type of adder is the delay needed to produce the carry out signal and the most significant bit (MSB) s3. The delay increases with the increase in the number of bits to be added.

III. DESIGN OF RIPPLE CARRY ADDER

RCA has been designed using two different 1-bit full adders in which the sum output has been implemented using two number of 3T XNOR gate in cascade and the carry output has been implemented using 3T XNOR gate and 2T multiplexer. Figure 3 shows the 4-bit RCA using existing 1-bit full adder as building block and Figure 4 shows its layout design [7], [8].

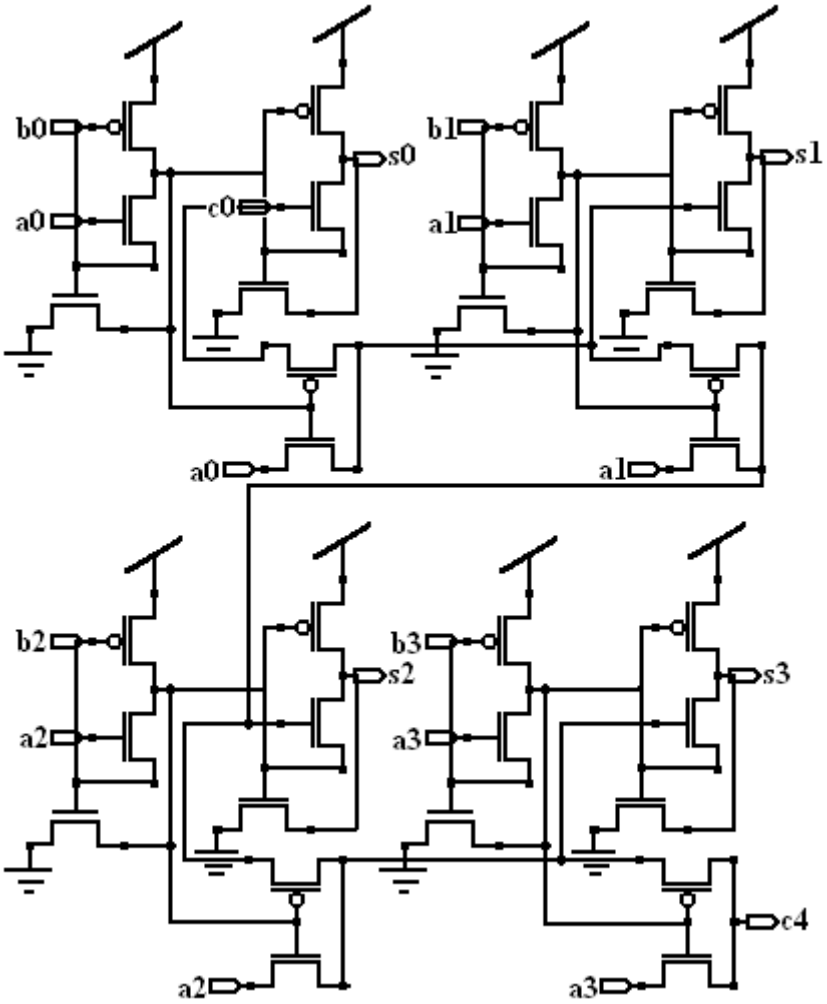

Figure 3. Circuit diagram of 4-bit ripple carry adder using existing 1-bit full adder

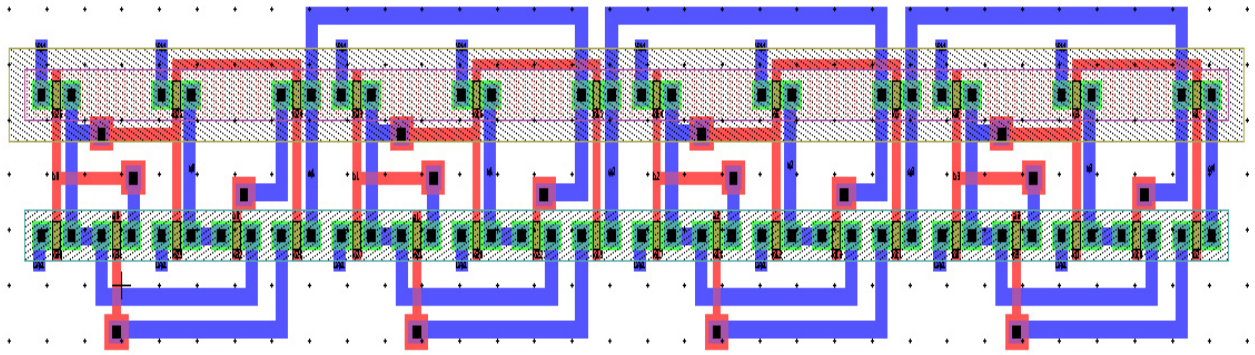

Figure 4. Layout of 4-bit ripple carry adder using existing 1-bit full adder

Figure 5 shows the schematic of 4-bit RCA using proposed full adder. Layout design of 4-bit RCA using proposed full adder is shown in Figure 6 [8-11].

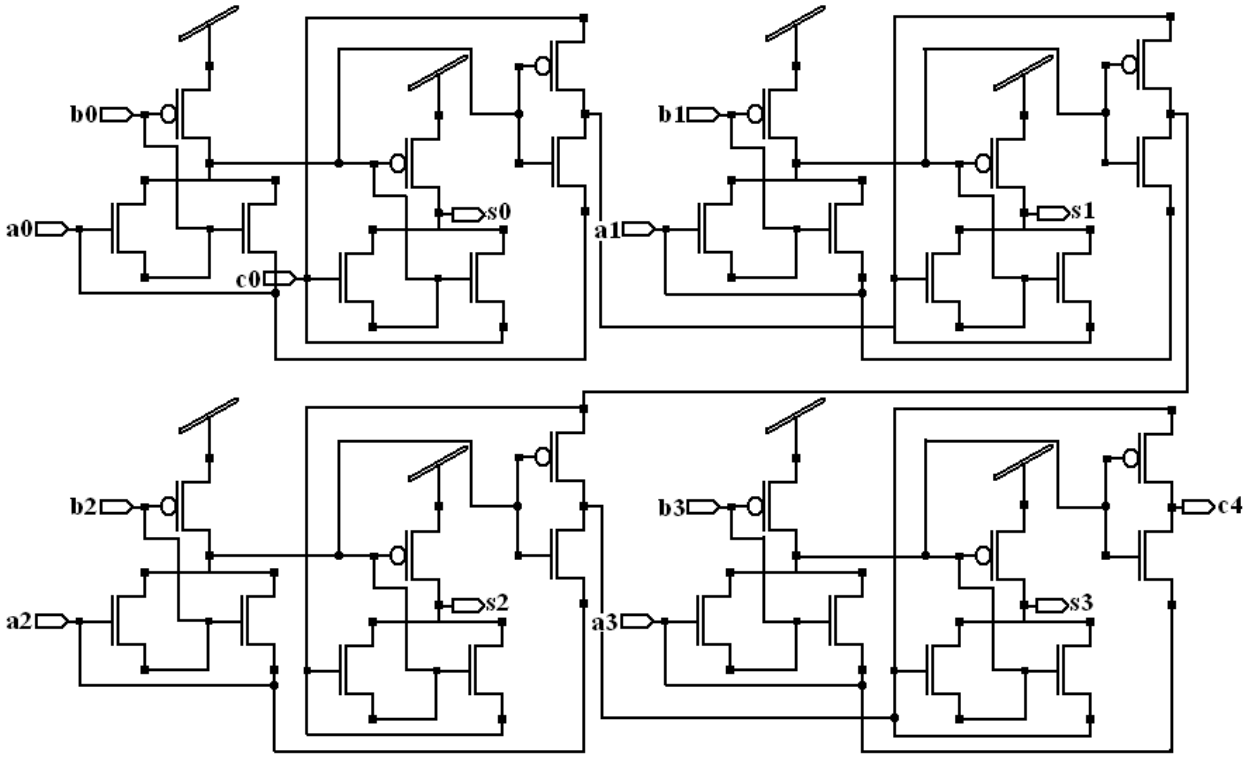

Figure 5. Circuit diagram of 4-bit ripple carry adder using proposed design of 1-bit full adder

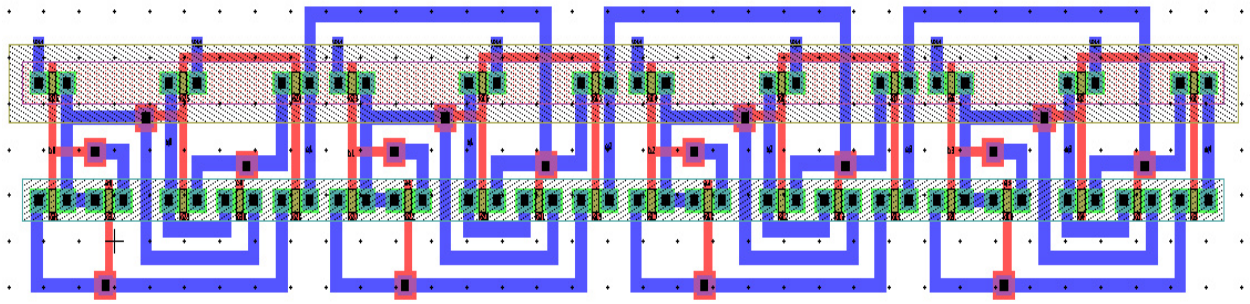

Figure 6. Layout of 4-bit ripple carry adder using proposed design of 1-bit full adder

IV. SIMULATIONS AND COMPARISON

The proposed 1-bit full adder based 4-bit ripple carry adder has been analyzed and compared with existing ripple carry adder in terms of power consumption and power-delay product at varying input voltages, frequencies and temperatures. To establish an impartial testing environment both circuits were simulated on same input patterns which covers each and every combination of the input stream. All schematic simulations are performed on Tanner EDA tool version 12.6 at 45nm technology. Figs. 7 and 8 reveals that the power consumption and PDP of RCA using proposed full adder with varying input voltage is less as compare to the existing one.

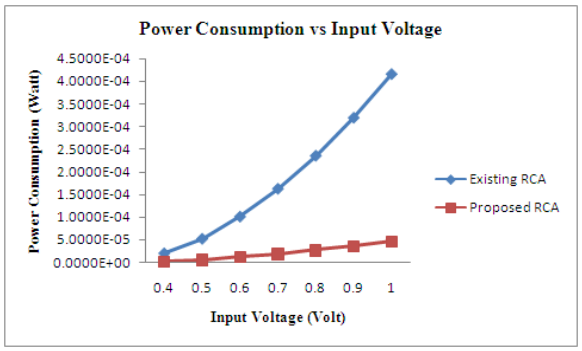

Figure 7. Power consumption over varying input voltage

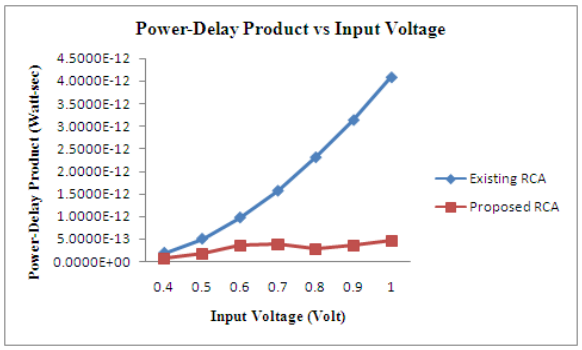

Figure 8. PDP over varying input voltage

Comparison in terms of power consumption and PDP of RCA using proposed full adder and existing full adder with varying temperature are shown in Figs. 9 and 10. The results shows that the RCA using proposed 8T full adder has better temperature sustainability which remains constant over large range of temperature than RCA using existing 8T full adder.

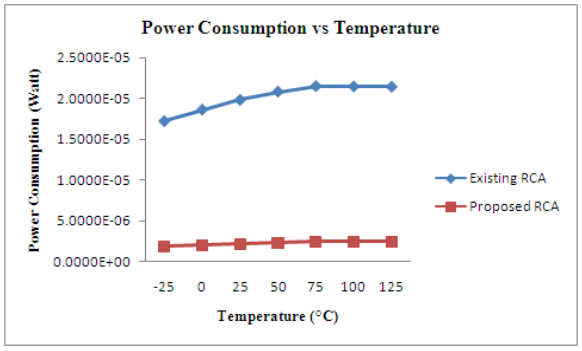

Figure 9. Power consumption over varying temperature

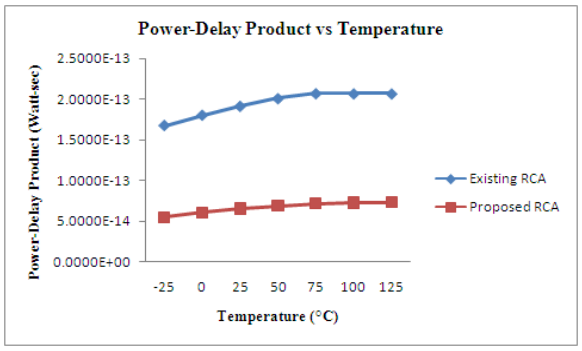

Figure 10. PDP over varying temperature

The performance of RCA using proposed full adder and existing full adder in terms of power consumption and PDP with varying frequency are shown in Fig. 11 and fig. 12 respectively which depicts that the proposed full adder based RCA has better performance as compare to the RCA using existing full adder.

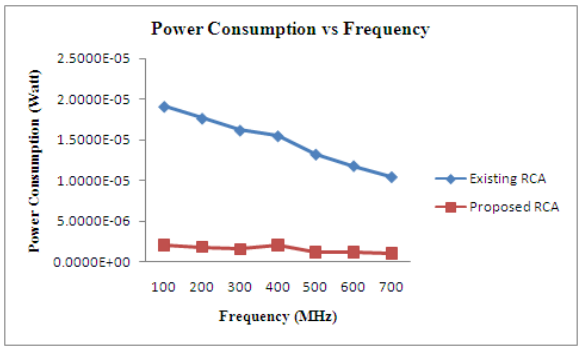

Figure 11. Power consumption over varying frequency

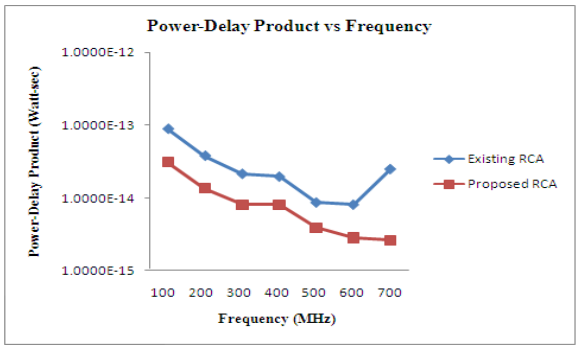

Figure 12. PDP over varying frequency

Figs. 7 through 12 reveal that the second design of RCA proves its superiority in terms of power consumption, power delay product at various input voltages and frequencies, and temperature sustainability over the first one.

V. CONCLUSION & FUTURE WORK

All pre-layout and post-layout have been designed and simulated using 45nm technology on Tanner EDA tool version 12.6 and proposed RCA proved itself to be a better option for low power applications. The proposed design shows 64-89% improvement with varying input voltage, 64-67% with varying temperature and 56-89% with varying frequency in term of PDP in comparison to existing design. The simulation results demonstrate that the proposed RCA proves to be an easier solution for significant improvement in power consumption, power-delay product at various input voltages and frequencies as well as temperature sustainability compared with the existing RCA. The proposed designs have proven to work efficiently in terms of various performance parameters. We can

further use these designs for the implement of multiplier accumulator (MAC) which is an important block of DSP and other complex circuits. These designs also form the basis of ALU.

ACKNOWLEDGEMENTS

The authors are very grateful to Mody Institute of Technology and Science, Faculty of Engineering and Technology for their support and encouragement and also for providing a good infrastructure and laboratory facility.

REFERENCES

[1]. N. Weste and K. Eshraghian, "Principles of CMOS Digital Design, A System Perspective," MA: Addison Wesley, 1993.

[2]. Chip-Hong Chang, Jiangmin Gu and Mingyan Zhang, "A Review of 0.18um Full Adder Performances for Tree Structured Arithmetic Circuits," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 13, No. 6, pp. 686-695, June 2005.

[3]. M. Alioto and G. Palumbo, "Analysis and comparison on full adder block in submicron technology," IEEE Trans. Very Large Scale (VLSI) Syst., vol. 10, no. 6, pp. 806–823, Dec. 2002.

[4]. Mariano Aguirre-Hernandez and Monico Linares-Aranda, "CMOS Full-Adders for Energy-Efficient Arithmetic Applications," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 4, April 2011.

[5]. John P. Uyemura, "Introduction to VLSI Circuits and Systems," John Wiley and Sons, Inc., 2002.

[6]. Sung Mo Kang and Yusuf Leblebici, "CMOS digital integrated circuits-analysis and design," Tata McGraw-Hill, third edition, 2003.

[7]. Manoj Kumar, Sandeep K. Arya, Sujata Pandey, "Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate," International Journal of VLSI design & Communication Systems, Vol. 2, pp. 47-59, December 2011.

[8]. Nayereh Ghobadi, Rabe'eh Majidi, Mahdieh Mehran, and Ali Afzali-Kusha , "Low Power 4-Bit Full Adder Cells in Subthreshold Regime," Proceedings of *International Conference on Emerging Electronics* (ICEE), pp. 30-34, May 2010.

[9]. Riya Garg, Suman Nehra, and B. P. Singh, "1-bit Full Adder using 9T Structure," International Conference on Technical and Executive Innovation in Computing and Communication (TEICC), pp. 560-564, Dec. 2012.

[10]. Riya Garg, Suman Nehra, and B. P. Singh, "Low Power Full Adder using 9T Structure," International Journal on Recent Trends in Engineering and Technology, Vol. 8, No. 2, pp. 52-55, Jan. 2013.

[11]. Riya Garg, Suman Nehra and B P Singh, "A New Design of Full Adder based on XNOR-XOR Circuit", International Journal of Computer Applications Vol. 66 No. 13, pp. 7-10, March 2013.

AUTHORS

Riya Garg was born in Aklera, Rajasthan, INDIA on 13/01/1991. She has done B.Tech in Electronics and Communication Engineering from the Faculty of Engineering & Technology, Mody Institute of Technology and Science, Rajasthan, INDIA in 2011. Presently, she is pursuing M.Tech. in VLSI Design from same university.

Suman Nehra was born in Gwalior, Madhya Pradesh, INDIA in 1983. She earned B.E. degree in Electronics & Communication Engineering from RGPV University in 2005 and M Tech. degree in VLSI Design from Faculty of Engineering & Technology, Mody Institute of Technology and Science, Rajasthan in 2011. Presently, she is pursuing Ph.D. from Faculty of Engineering & Technology, Mody Institute of Technology and Science, Rajasthan. After stepping into professional world, she started as lecturer with Shekhawati Engineering College. After that she joined Faculty of Engineering & Technology, Mody Institute of Technology and Science, Rajasthan as Asst. Professor 2008. Her current research interests include digital VLSI circuits. She has over 06 papers published in International Conferences and Journals.

B. P. Singh was born in a village Orro, Nawadah, Bihar (India) in 1947. He did B.Sc. (Engg.) and M.Sc. (Engg.) from Bihar Institute of Technology, Sindri, Dhanbad and B.I.T. Mesra Ranchi in 1967 and 1970. He did Ph.D. from Ranchi University Ranchi in 1980. He served B.I.T. Mesra, Ranchi from 1970 to 1981, Indian School of Mines Dhanbad from 1981 to 1987 and Madan Mohan Malaviya Engg. College from 1987 to 2009. From 2009 till date he is the HOD of ECE and EEE, Mody Institute of Technology Lakshmangarh, Sikar, Rajasthan (INDIA). He has over 105 papers to his credits in International and National Journals and over 65 presentations in International and National Seminars/ Symposia/ Conferences. He has authored four books, namely; Microprocessors, Interfacings and Applications, Advance Microprocessors & Microcontrollers, New Age International, New Delhi. Microelectronic Devices & Circuits: Indefinite Admittance Matrix Approach, New Age International, New Delhi. Electronic Devices and Integrated Circuits; Pearson, Education, New Delhi.