A NEW ADDITION DESIGN PRINCIPLE BASED ON TERNARY OPTICAL PROCESSOR

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ABSTRACT

A three-step Ternary optical modified signed digit (MSD) adder is proposed based on decrease-radix design principle (DRDP) which constructs all dualistic ternary logic operators. In this present work all optical scheme of the different ternary logical states are represented by vertical and horizontal polarized state of light. The basic operational unit (BOU) of the adder is implemented with LCD, vertical and horizontal polarizer and suitable control circuit (CC). Optical tri-state gates has been used in the control circuit to have minimal number of BOUs. To further reducing the number of BOUs, pipeline principle has been successfully used in (n+2) cycles to get the final results of two arrays MSD numbers where n is the number of elements in each array. Theoretical design is presented and verified through numerical simulation of the three steps of the MSD addition. The method promises both accuracy and higher processing speed.

I.   INTRODUCTION

The advent of digital-computing techniques has already produced tremendous increases in speed, accuracy , and flexibility over analog-computing techniques. However, digital computing is constrained mainly by Von Neumann interconnection bottleneck, which makes the computation process inherently sequential in nature [1]. Optical computing provides an attractive approach of attaining ultra-high-speed computing since it can process enormous amounts of data in parallel, at a high speed, with high temporal/spatial bandwidth and non-interfering communications [2]. Several nonbinary-number representation schemes, such as multiple-valued fixed radix-number, residue-number, redundant-number, and signed-digit-number representations have been reported in the past decade to increase the speed of computation and to implement these nonbinary-based arithmetic operations digitally and optically. Signed-digit number representations limit carry propagation to one (two) positions to the left during the operations of addition(subtraction) in digital computers. The carry-propagation chains are eliminated by use of redundant representation for operands [3]. In 2000, Jin Yi proposed a new optical computer structure ternary optical computer using light intensity and polarization to denote ternary value:0, 1, 2[4]. In early 2007, Yan JunYang, Jin Yi, and Kaizhong find the rule of multi-valued logic processor and setup the DRDP [5]. After that in 2010, Jin Yi et al. proposed the principle and organization of modified signed-digit (MSD) adder, and designed the MSD adder for TOC [6]. In 2011, Ouyang Shan et al. ternary optical processor TOP construction via the reconfiguration circuit, to an operator demanded byusers dynamically, and namely the limited optical hardware resource can be reused to construct any one of the 19 683 two-input tri-value logic operators [7, 8]. The design of an all-optical system for some basic tri-state logic operations (trinary OR, trinary AND, trinary XOR, Inverter (IN), Truth detector (TD), False detector (FD)) which exploits the polarization properties of light. Nonlinear material based optical switch can play an important role. Tri-state logic can play a significant role towards carry and borrow free arithmetic operations [9, 10].

The main aim of this study is to get suitable design, the control circuit is employed in a new form to obtain less number of basic operation units BOUs which are used in addition operation. We attempt to rise the performance of TOP to higher level comparison with the previous design, some developments have been added in order to obtain an efficient design. In this paper three-step MSD addition optical TOC structure is presented based on DRDP principle. The paper is organized as follows. In Section II design principle of DRDP, the structure of the ternary optical processor and the three-step addition algorithm are discussed. Section III explains with suitable tables the correct operation of the addition. Section IV discusses simulation results of two MSD arrays and discussion. Section V discusses conclusion and suggests a roadmap for future works.

II.   EXPERIMENTAL MATERIALS AND PROCEDURE

A. Decrease-Radix Design Principle (DRDP)

The principle of decrease-radix design principle for making multi-valued logic unit, which proposed by Prof. Yi Jin and his PhD candidates Yan Jun-Yong and Zuo Kaizhong, gives a technological guide for the design of multi-valued computer and become the fundamental theory of ternary optical computer. The main conclusion of the decrease-radix design theory, is that , if the D-state is include as one of the n physical states (n >1) for information representation, then each of the 2-input, n-valued logic operators without carry generation (referred to as an n-valued logic operator in the sequel), can be constructed from no more than nx(n-1) singleton basic operation units (singleton BOUs)following a determinate procedure, with up to n x n x (n-1) types of singleton BOUs. The total number of different 2-input n-valued logic operators is known to be n(nxn)[5,11].

B. Ternary Optical Processor

TOC is a new type of computer, which uses three basic states of light (dark light and two polarized light whose polarization directions are orthogonal to each other) to express information, and the transitions of three states can be used to implement a series of operations. The arithmetic computing in a TOC realized based on MSD system $\{\bar{1}, 0, 1\}$, the vertical polarization light represents (1), the horizontal polarization light represents ($\bar{1}$), and the no light (dark light) represents (0) [12,13].ternary optical processor is mainly composed of 2-D light array, coder, calculator, and decoder. The physical structure of ternary logic optical processor is shown in Fig.1.Coder is made of two polarizer and two pieces of liquid crystal, and calculator is made of two polarizer (white section represents vertical polarizer and black section represent horizontal polarizer) and one piece of liquid crystal, all these components are thin pieces of same size and are stuck together closely. Pixels in the same position of all the liquid crystal of this optical processor are corresponding to one another[14,15].
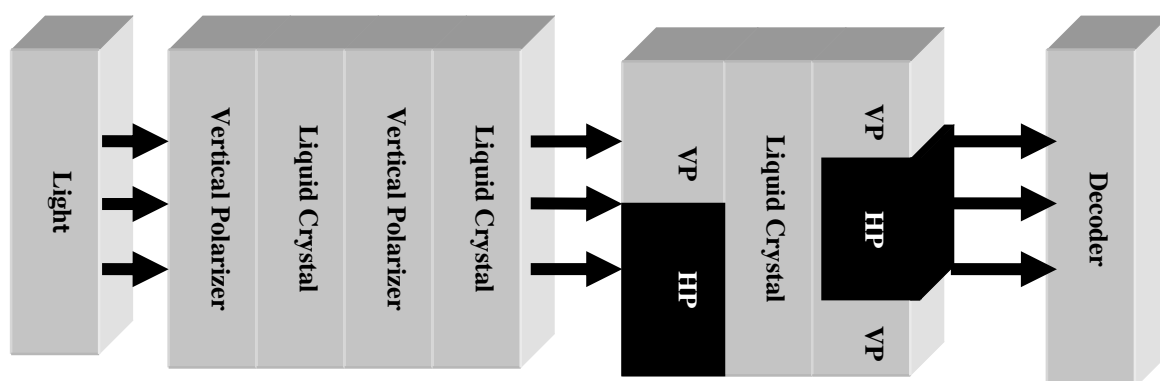

Figure 1. Structure of Ternary Optical Processor.

C. **Three-Step Algorithm for MSD Addition Operation**

MSD was proposed by Avizienis in 1961[16], and was first used on optical computing by Draker in 1986. A number x can be represented in MSD by the following equation:

$$X = \sum_i x_i 2^i \qquad x_i \in \{\bar{1}, 0, 1\} \tag{1}$$

Suppose the MSD representation of augends X and addend Y are :-

$X_{MSD} = X_{n-1}, \ldots, X_i, \ldots, X_0$. **Table 4.** Truth Table of W'-Transformation.

$Y_{MSD} = Y_{n-1}, \ldots, Y_i, \ldots, Y_0$. The three-step addition is performed according to the following:-

Step 1: The T- transformation (carry) and W- transformation (sum) on every couple of bits of X_i and Y_i of the MSD addition are shown in Table 1 and Table 2, respectively[17,18].

$$\text{Compute } X_i + Y_i = 2T_{i+1} + W_i \ (i=0, \ldots, n-1). \tag{2}$$

Table 1. Truth Table of T-Transformation.   **Table 2.** Truth Table of W-Transformation.

W	1	0	$\bar{1}$
1	0	$\bar{1}$	0
0	$\bar{1}$	0	1
$\bar{1}$	0	1	0

Step 2: The T'-transformation and W'-transformation on every couple of bits of T_i and W_i, we get T'_{i+1} and W'_i as shown in Table 3 and Table 4, respectively.

$$\text{Compute } T_i + W_i = 2T'_{i+1} + W'_i \ (i=0, \ldots, n-1) \tag{3}$$

Table 3. Truth Table of T'-Transformation.   **Table 4.** Truth Table of W'-Transformation.

T'	1	0	$\bar{1}$
1	1	0	0
0	0	0	0
$\bar{1}$	0	0	$\bar{1}$

W'	1	0	$\bar{1}$
1	0	1	0
0	1	0	$\bar{1}$
$\bar{1}$	0	$\bar{1}$	0

Step 3: The truth table of final sum Si on every couple of bits of T'_i and W'_i is seen as the T-transformation shown in Table 1.

$$\text{Compute } S_i = W'_i + T'_i \ (i=0, \ldots, n-1) \tag{4}$$

III.   NEW DESIGN OF OPTICAL ADDER USING A TERNARY OPTICAL PROCESSOR

The use of the optical tri-state gates has been suggested as away to eliminate the number of BOUs which are considering the main component of control circuit. The arithmetic operations form the largest field of computer optical arithmetic which operates on one or more operands depending on the operation. The operation is selected from allowable set, which is usually includes addition, subtraction, multiplication, division, and so on. Addition process for two operands which is an arithmetic operation has three steps to be calculated, obtained intermediate results and then compute final sum. The main problem with addition operation is the word length from side and the circuit complexity in the other side, therefore, we will focus on designing an efficient signed-digit adder for two or more operands.

Step One of Design:
T-Transformation:
By using tri-state optical gates (OR & False Detector FD) with suitable design, the three cases combinations$\{(1+1), (1+0), \text{ and } (0+1)\}$ can be implemented using one BOU as shown in Fig. 2. The output of this circuit is equal to 1 only for the combinations$\{ (1+1) \text{ or } (1+0) \text{ or } (0+1)\}$. While the three cases combinations$\{(\bar{1}+\bar{1}), (\bar{1}+0), \text{ and } (0+\bar{1})\}$ is constructed based on single BOU by using tri-state optical gates (OR & Truth Detector TD) with suitable design. The three cases combination$\{(\bar{1}+\bar{1}), (\bar{1}+0), \text{ and } (0+\bar{1})\}$ can be implemented as shown in Fig. 3. The output of this circuit is equal to $\bar{1}$ only for the combination$\{(\bar{1}+\bar{1}) \text{ or } (\bar{1}+0) \text{ or } (0+\bar{1})\}$. The two BOUs are accumulated to form adder in step one (T-transformation) as shown in Fig. 2. Note that only one sub-output (t1, and t2) is activated for any combination of the inputs.
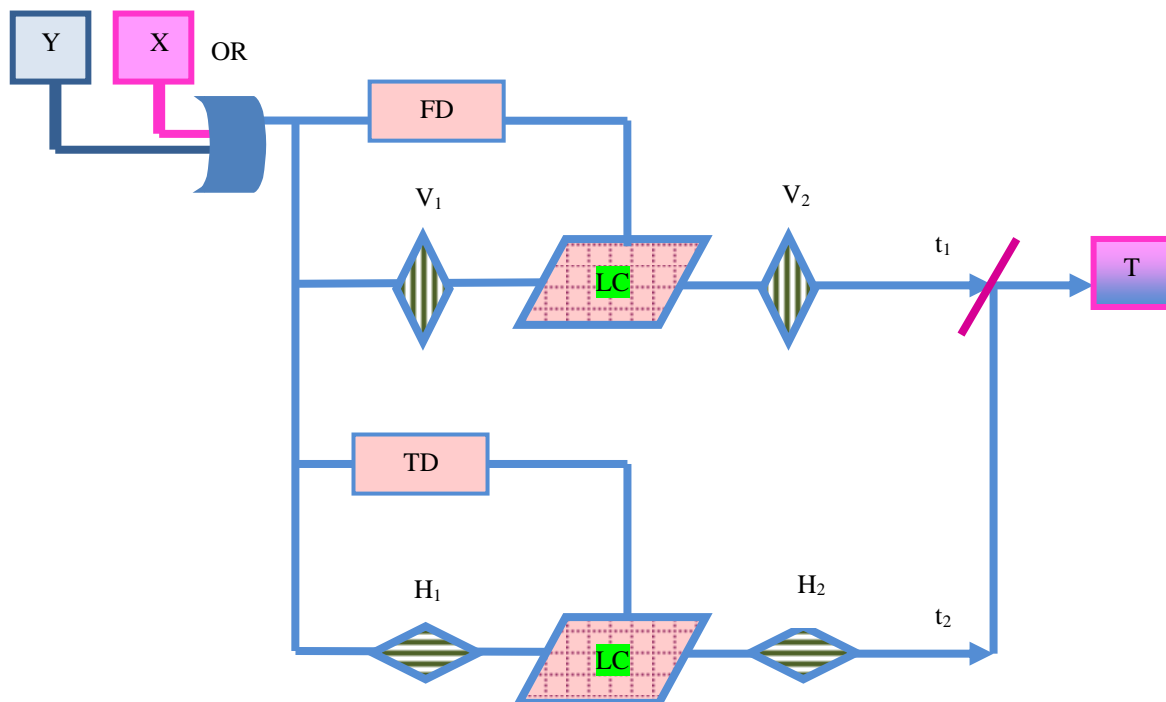

Figure 2. Structure of ATOP for Addition Operation.
(T-Transformation of Step One Addition).

W-Transformation:
By using tri-state optical gates (AND, OR, and Inverter IN) with suitable design, the two cases combination$\{(\bar{1}+0) \text{ and } (0+\bar{1})\}$, the output of this circuit is equal to 1 only for the combination$\{(\bar{1}+0)$ or $(0+\bar{1})\}$. By using tri-state optical gates (AND, OR, and Inverter IN) with suitable design, the two

cases combination$\{(1+0)$ and $(0+1)\}$, the output of this circuit is equal to $\bar{1}$ only for the combination $\{(1+0)$ or $(0+1)\}$. The two BOUs are accumulated to form adder in step one (W-transformation) as shown in Fig. 3. Note that only one sub-output (w1 and w2) is activated for any combination of the inputs.

Figure 3. Structure of MTOP for Addition Operation.
(W-Transformation of Step One Addition).

Step Two of Design:

T'-Transformation: By using tri-state optical gate(False Detector FD), the combination$\{(1+1)\}$ which results an output equal to 1. While using tri-state optical gates(True Detector TD) with suitable design, the one combination$\{(\bar{1}+\bar{1})\}$ can be implemented and the output of this circuit is equal to $\bar{1}$. The two BOUs are accumulated to form adder in step two (T'-transformation) as shown in Fig. 4. Note that only   one   sub-output (t'1 and t'2) is activated for any combination of the inputs.

Figure 4. Structure of MTOP for Addition Operation.
(T'-Transformation of Step Two Addition).

Step Three of Design : The structure and components of step three (T- transformation) are the same as (T-transformation) in step one.

IV.   SIMULATION RESULTS

Optical Simulation of Three-Step Adder : The number of BOUs in this method depends only on the number bits in each operand. Therefore, the number of BOUs is calculated as in Eq.(5):-

$$B = 10 \times (n + 2) \tag{5}$$

Where B:Number of basic operation units
      n: Number of bits in each operands

Example:- For the following addition operation:-

$$
\begin{bmatrix} X_1 \\ X_2 \\ X_3 \end{bmatrix}
+
\begin{bmatrix} Y_1 \\ Y_2 \\ Y_3 \end{bmatrix}
=
\begin{bmatrix} S_1 \\ S_2 \\ S_3 \end{bmatrix}
\Rightarrow
\begin{bmatrix} (28117)_{10} \\ (^-32111)_{10} \\ (32767)_{10} \end{bmatrix}
+
\begin{bmatrix} (21286)_{10} \\ (^-31674)_{10} \\ (^-2618)_{10} \end{bmatrix}
=
\begin{bmatrix} (49403)_{10} \\ (^-63785)_{10} \\ (30149)_{10} \end{bmatrix}
$$

$$
\begin{bmatrix} (111\bar{1}110\bar{1}1011\bar{1}01)_{MSD} \\ (\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}010010\bar{1}\bar{1}\bar{1}\bar{1})_{MSD} \\ (1111111111111111)_{MSD} \end{bmatrix}
+
\begin{bmatrix} (101001101\bar{1}01\bar{1}10)_{MSD} \\ (\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}000101\bar{1}0\bar{1}0)_{MSD} \\ (\bar{1}1110\bar{1}0\bar{1}1001\bar{1}10)_{MSD} \end{bmatrix}
=
\begin{bmatrix} (1100000100001\bar{1}10\bar{1})_{MSD} \\ (\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}\bar{1}100\bar{1}0\bar{1}0\bar{1}1)_{MSD} \\ (1111\bar{1}1\bar{1}11000011\bar{1})_{MSD} \end{bmatrix}
$$

The addition operation consists of five cycles as shown in Table 5. The total numbers of the used BOUs in this design is equal to (238) for the five cycles. The optical simulation of the five cycles is shown in Fig. 5:

Table 5. The Three-Step of Addition Operation for the Five Cycles That are used to get the Final Results.
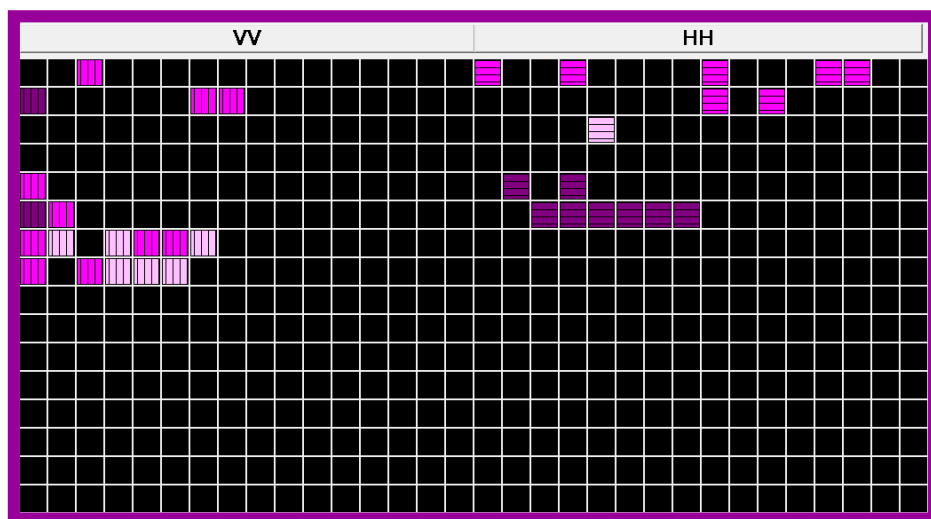
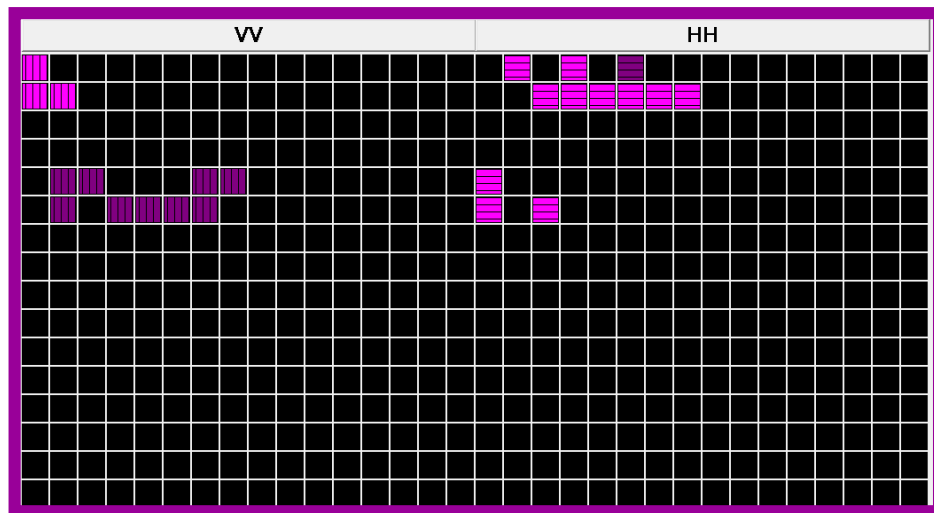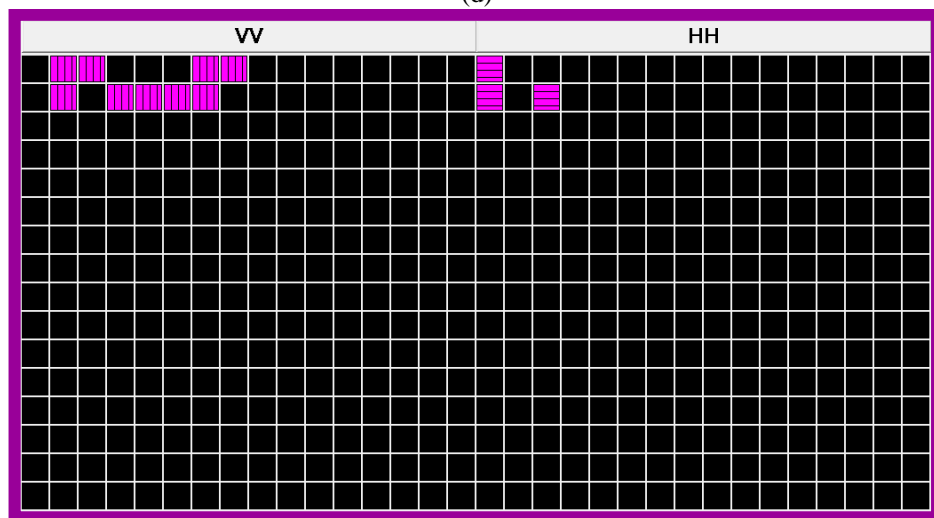| No. of Cycle	Step One	Step Two	Step Three
Cycle 1	$X_1 + Y_1$	----------	----------
Cycle 2	$X_2 + Y_2$	$T_1 + W_1$	----------
Cycle 3	$X_3 + Y_3$	$T_2 + W_2$	$T'_1 + W'_1$
Cycle 4	----------	$T_3 + W_3$	$T'_2 + W'_2$
Cycle 5	----------	----------	$T'_3 + W'_3$
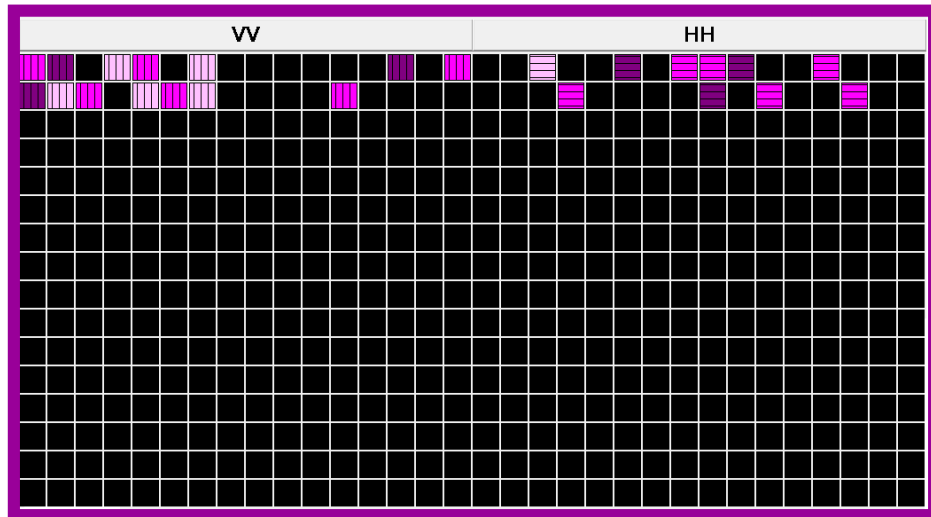
(a)
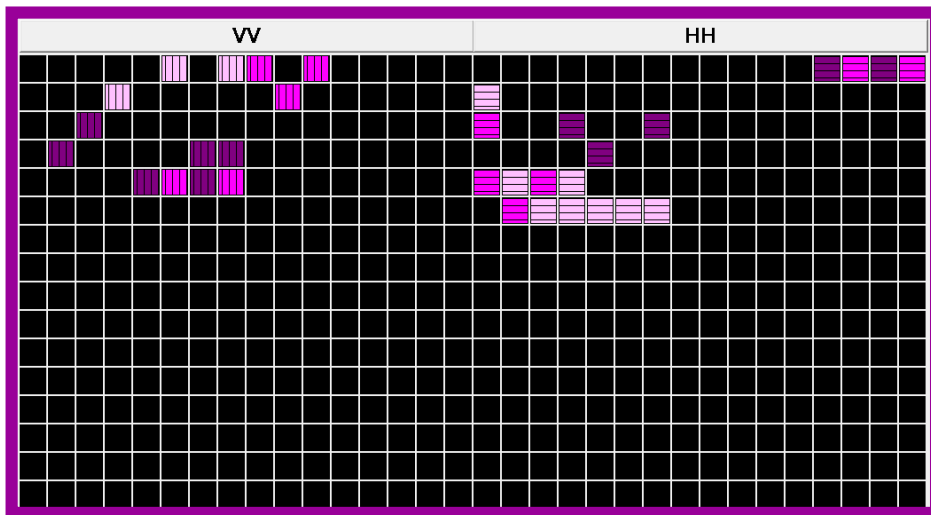
(b)

(c)

Figure 5. The Optical Simulation of Five Cycles in Pipeline Method.
(a) Cycle One. (b) Cycle Two. (c) Cycle Three. (d) Cycle Four. (e) Cycle Five.

(d)

(e)

From this new design, the addition circuit can compute the summation of two array MSD number, Each number may consist of 42 bits. Table 6 shows the benefits of this design as compared with that presented in Ref. [15, 18].

Table 6. Comparison between Current Design and Previous of TOP.

No. of	Previous design [15,18]	Current design
No. of sections	4 Sections (VV, HV, HH, VH)	2 Sections (VV, HH)
No. of Bits	1-14 bits	1-42 bits
No. of BOUs /Bit	22	10
No. of total used BOUs	22*(n+2)	10*(n+2)

V. CONCLUSIONS AND FUTURE WORKS

A new method is presented in this paper that reduces the total number of BOUs. The design is based on a single BOU for the combinations{(1+1), (1+0), and (0+1)} and {($\bar{1}+\bar{1}$), ($\bar{1}$+0), and (0+ $\bar{1}$)} in the generation of T- transformation in step one and step three for addition operation with the aid of using suitable tri-state optical gates control circuits. Similarly, because of the control circuit, the design is based on a single BOU for the combinations {(1+0) and (0+1)} and {($\bar{1}$+0) and (0+ $\bar{1}$)} in the generation of W-transformation in the step one and step two for addition operation. Therefore,

the total number of BOUs /bit in this design becomes equal to 10 BOUs/bit. Thus, reducing number of used BOUs and increasing the speed of operations. We attempt to rise the performance of TOP to higher level as compared with the design in Ref. [14]. The procedure and design used in this paper can be used for the multiplication operation after computing the partial product results with suitable design of BOUs. Also, the work can be extended to develop a TOC that can compute the arithmetic operation of number with higher radix such as trinary and quaternary singed digit numbers (TSD) and (QSD) by using suitable optical circuit that converts these numbers to MSD numbers.

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