POWER COMPETENT CMOS COMPARATOR FOR ANALOG TO DIGITAL CONVERTER CIRCUITS

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ABSTRACT
Comparators are basic building elements for designing modern analog and mixed signal systems. In this paper, a Power efficient CMOS comparator was implemented by using low power technique. Among all the comparators, the dynamic CMOS comparator was chosen because of the efficiency which is highly needed in the case of ADC circuit. Speed and resolution are two important factors which are required for high speed applications. By using the low power technique we have reduced the power of the dynamic CMOS comparator from 16% to 45% .Cadence tool was used to implement the comparator in transistor level .The measured and simulation results show that the dynamic latched comparator design has higher speed, low power dissipation. We have used 180nm technology to analyse the comparator.

KEYWORDS: *Dynamic CMOS comparator, flash ADC circuit.*

I. INTRODUCTION

A comparator becomes the great electronic device, which widely used in the analog to digital converters and plays important role in high speed ADC. In general, a comparator is a device, which compares two current or voltages and produces the digital output based on the comparison. Many applications, such as analog to digital (ADCs), memory sensing circuits and recently also on chip transceivers are widely using comparators. In the last year, most of the researches focus on the comparator with low power consumption, simple thermal management and high efficiency. The growth of the portable electronic devices make the power consumption is critical issue to circuit designers because the low power and high speed comparators are the main building block in the front end of the radio frequency receiver in the most of the modern telecommunications system. Recently, most of the researchers have proposed the dynamic latch comparators based on the cross coupled inverters due to the positive feedback commonly used in flash analog digital converters (ADC) due to their high decision speed.

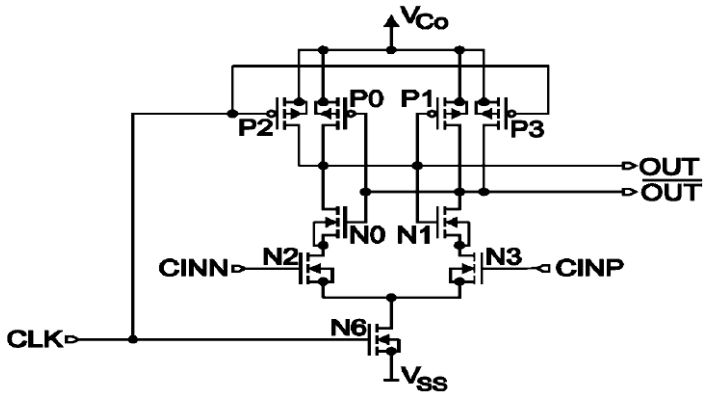


Figure.1: Conventional latch-type comparator

Fig 1 shows a widely used standard conventional latch type comparator circuit with the high impedance input, rail to rail output swing and no static power consumption [1].Robustness against noise and mismatch are the main advantage of the conventional latch type comparator. However, it suffers from high sufficient power supply, which is caused by many stacked transistor in circuit design. Goll and Zimmermann proposed a comparator with reduced delay time [2] in 65nm CMOS using 0.65V as the supply voltage as shown in Figure 2.

The proposed design is different from the conventional circuit by replacing a new latch for low power supply voltage operating, which offers the great advantage of high impedance input, rail to rail output swing, no static power dissipation and indirect influence of the parasitic capacitance of the input transistors to the output nodes.

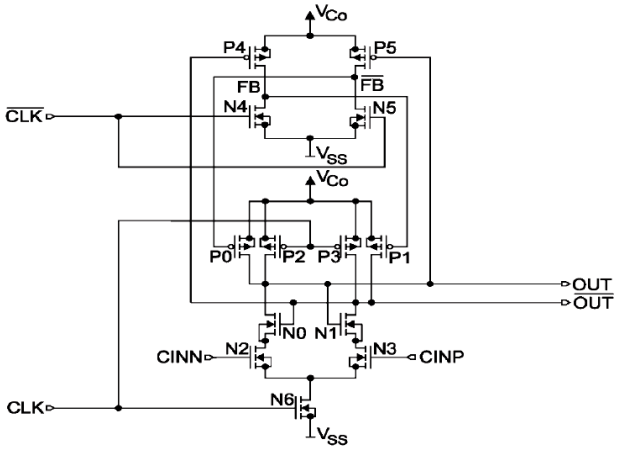


Figure.2: Comparator with modified latch.

In this paper, a new CMOS dynamics latch comparator is presented. The fully dynamic charge sharing topology employed latch circuit with high input impedance. Moreover, a rail to rail output swing is produced with no static power dissipation. In addition, the proposed design comparator is free from indirect influence of the parasitic capacitance of the input transistors to the output nodes. The design is optimized by choosing the right W/L ratio of the transistors in the circuit [5]. The design exhibits latched MOS transistors with faster output. Flash ADCs [11] (sometimes called parallel ADCs) are the fastest type of ADC [3] and use large numbers of comparators.

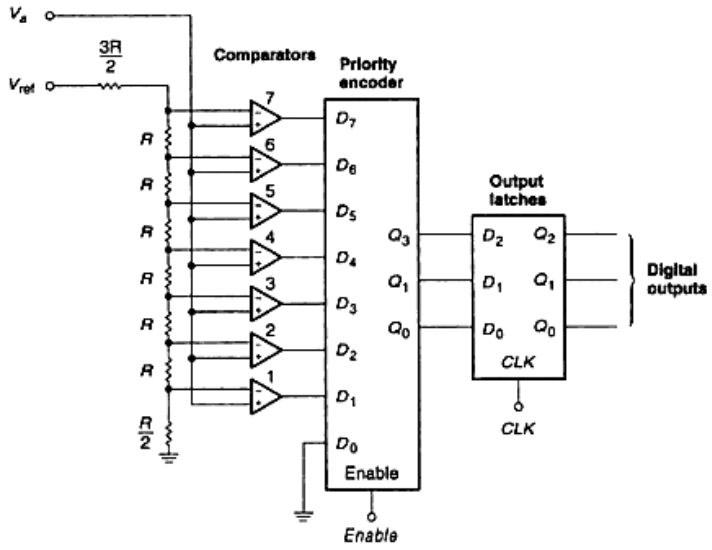


Figure.3: Flash ADC Circuit

The input signal is applied to all the comparators at once, so the thermometer output is delayed by only one comparator delay from the input, and the encoder N-bit output by only a few gate delays on top of that, so the process is very fast.

II. DYNAMIC CMOS COMPARATOR

The dynamic latched comparator is composed of two stages .The first stage is the interface stage which consists of all the transistors except two cross coupled inverters. The second stage is the regenerative stage that is comprised of the two cross coupled inverters, where each input is connected to the output of the other.

It operates in two phases.

1) Interface phase. 2) Regeneration phase.

It consists of single nmos tail transistor connected to ground. When clock is low tail transistor is off and depending on Vp and Vn output reaches to VDD or gnd. When clock is high tail transistor is on and both the outputs discharges to ground. There is reduction of both power and delay in dynamic latched comparator [10] circuit over the double tail latched and pre-amplifier based clocked comparators. Double tail latched comparator has less power consumption but low speed because of more transistor count and pre-amplifier based clocked comparator has high speed because of less transistor count but power consumption is more because it uses an amplification stage, it consumes static power during the amplification period However, since the pre-amplifier based clocked comparator is to work at high frequency, the energy consumption of the pre-amplifier based clocked comparator becomes comparable to the double tail latched comparator. Hence the performance of the pre-amplifier based clocked comparator is limited by the static power dissipation in the evaluation or regeneration phase. Due to fast speed, low power consumption [6], high input impedance and full-swing output, dynamic latched comparators are very attractive for many applications such as high-speed analog-to-digital converters (ADCs)[12], memory sense amplifiers (SAs) and data receivers[8]. They use positive feedback mechanism with one pair of back-to-back cross coupled inverters (latch) in order to convert a small input-voltage difference to a full-scale digital level in a short time. Thus dynamic latched comparator is suitable for both high speed and low power dissipation because of decrease in transistor count which overcomes the problem of double tail latch and pre-amplifier based clocked comparators.

2.1 Latched Comparator

To overcome the limited response time of an OTA-comparator, latched comparators are very often used. A simple transistor circuit of a latched comparator is presented in figure. The comparator consists of a differential stage with a latch as load. Latch comparators [7] have two phases: the rest

mode and the compare mode.in the rest mode the nodes of the latch are shorted to set it to an unstable high gain mode. In the compare mode these nodes are released. Depending on the input voltage the latch will switch vary fast to high (low) state due to the positive feedback in the latch.

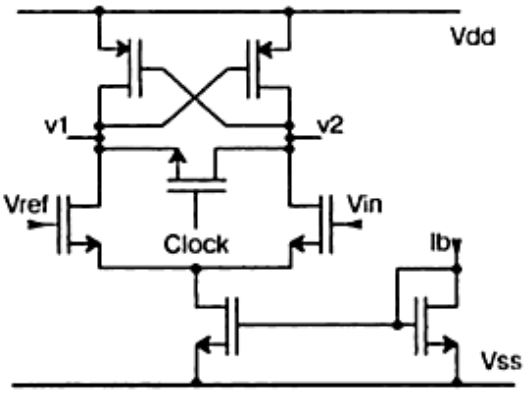


Figure.4: A latched comparator circuit

The drawback of this simple structure is:

- At the end of the compare mode one of the input transistor is forced into the triode region.as a result the total speed of the comparator (including the rest phase) is increased. This is due to the required extra settling time in order to achieve the necessary accuracy in the rest phase
- The switch which controls the two modes is connected to the input transistor. As a result clock feed-through can be fed to the input nodes. This can limit the comparator accuracy especially when a voltage with a high source impedance is being compared.
- The accuracy of this comparator is mainly limited by the unsymmetrical latch structure (only NMOS devices) and by the latch transistor mismatches. These effects are analyzed more in detail in the next section

To overcome the two first problems the input stage of the circuit is usually modified using an extra current mirror as is presented in Figure 5. With such a structure a response time (rest phase include) of 30-40nSec can be achieved.

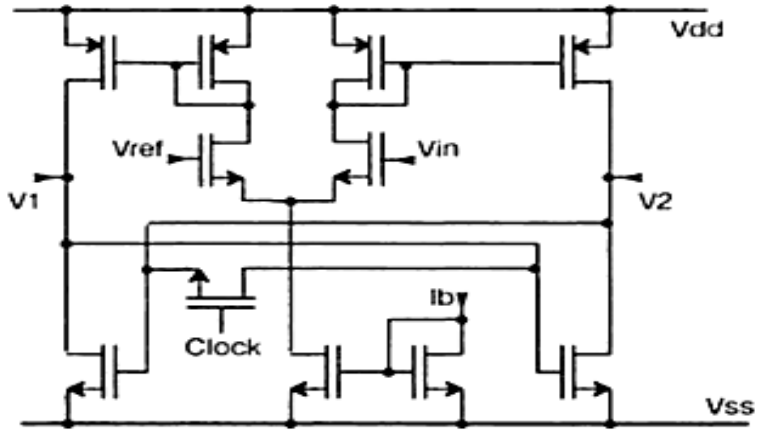


Figure.5: An improved latched comparator

2.2 A High Speed Accurate Comparator

In the realization of high speed CMOS flash A/D converters and high accuracy CMOS over sampling A/D converters, high speed CMOS comparators are indispensable. The high speed structure is presented in Figure 6. It consists of two inverters (M13, M14 and M11, M12).

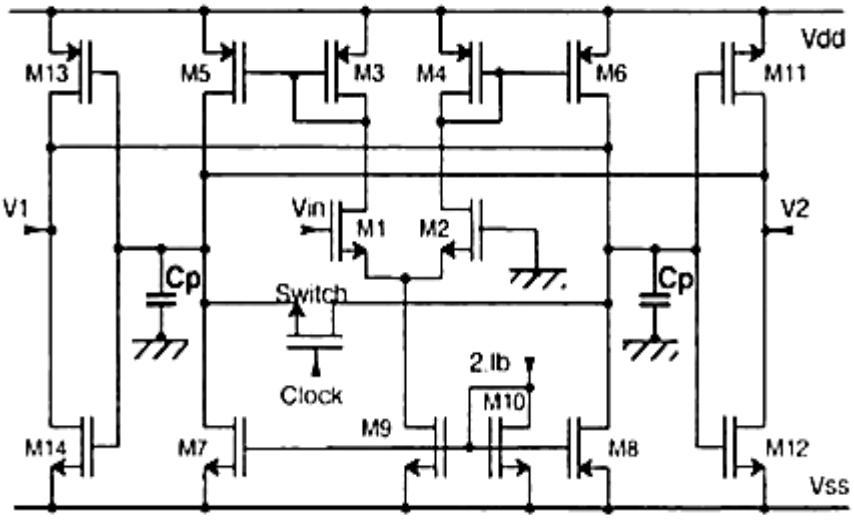


Figure.6: The high speed latched comparator circuit

Assembled as a latch, in combination with a transconductance amplifier (M1-M10). By closing the switch, the latch is set in its unstable state. This structure has several important advantages compared with the other structures using the latch principle. First the input stage does not contain any switches. As a result no clock feed-through is injected to the input nodes. This is very important for an over sampling A/D where an integrator drives the input of the comparator. Secondly, due to M7 and M8, no current from the transconductance amplifier [9] flow into the latch when the switch is closed. As a result the latch voltage is not influenced by the biasing current when the switch is closed. Hence the biasing current can be increased which result in a higher resolution thirdly, only one switch is used in a totally symmetrical structure. So the effect of clock feed-through is minimized. Finally a two inverter latch structure is employed .This is important because the connected circuit is usually a digital building block (an inverter). As a result, if identical inverters are used, the out voltage in the rest mode is present at the threshold voltage of the high (low) transition. This fact remains true even with process variations; as long as the inverters latch transistors are equal to the one of the connected digital inverter.

First the comparator output voltage as function of time is discussed. Then the comparator accuracy due to transistor mismatched and clock feed-through are studied. Finally the comparator speed is discussed.

The comparator: Assuming a constant transconduction (gm) model for the inverters, and if the transconductance of the amplifier is Gm,the output voltage of the comparator as a function of time are (the switch opens at t+0);

$$v_1 = \left(V_D - \frac{Gm}{2.gm}.Vin\right).e^{a.t} + \left(V_C\right).e^{-a.t} + \frac{gm}{2.gm}.Vin + \frac{\Delta IB}{gm} \quad \text{.....Eq(1.1)}$$

$$v_2 = \left(V_D - \frac{Gm}{2.gm}.Vin\right).e^{a.t} + \left(V_C\right).e^{-a.t} + \frac{gm}{2.gm}.Vin + \frac{\Delta IB}{gm} \quad \text{.....Eq(1.2)}$$

Limited accuracy due to transistor mismatch in the latch:

Suppose that one of the latch transistors has a certain mismatch. As a result an offset voltage is generated at the input of the inverter. If the threshold voltage (V_T) of PMOS and NMOS transistors are approximately equal, a symmetrical power supply is used (Vdd = -Vss) and the transistors are designed so that KP(W/L)nmos = KP(W/L)pmos, then the voltage at t=0 without mismatch are V_1=V_2=0.however,due to mismatch, let say a ΔW and ΔVtbecome PMOS transistors M11 and M13, the maximum error voltage at t=0 become $V1V1 \approx -V2\Delta(Vt/4).(\Delta W/2.W+\Delta Vt/Vt)$. As a result an extra V_D is generated which limits the accuracy of the comparator? The comparator reaches a resolution Vr given dy :

$$Vr \approx \frac{gm.Vt}{2.Gm}.\left(\frac{\Delta W}{2.W}+\frac{\Delta Vt}{Vt}\right)$$ ……Eq(1.3)

For example, with $(\Delta W/2.W+\Delta Vt/Vt) \approx 2\%$,gm = 300µA/V and Gm = 500µA/V,Vt = 0.8V, $V_r \approx 5mV$. In order to decrease this error, the transconductance of the latch must be decreased or Gm must be increased.

Clock feed-through:

When the switch opens, a charge is injucted into the capacitances Cp. This result in a common mode signal Vc and a differential signal $2.V_D$. As can be seen from equations 1.1, 1.2, vc will not affect the accuracy, However, the resolution of the comparator is limited by $V_{D,}$ which is

$$V_D = \frac{Cox.(W.L)s.Vstep}{2.Cp}.\frac{\Delta Cp}{Cp + Cox.(W.L)s}$$
$$\approx \frac{\Delta Cp}{2.Cp}.\frac{Ws}{2.Wi + Ws}.Vstep$$ ……Eq(1.4)

Where Vstep = ((Vclock,high-Vclock,low)/2-Vt). (W/L)s are the switch dimensions, ΔCp is the mismatch between the capacitances Cp,(W/L)I are the dimensions of M12 and M14. The aspect ratio of M11,M13 are equal to twice the value of M12,M14 and as a result Cp is approximately equal to 2.Cox(W.L)I (it can be shown that capacitances other than the inverter transistors have a positive effect on the accuracy). Using equations1.1, 1.2 a resolution Vr = 5mV is obtained when (2.Wi<Ws).

$$(W/L)i \approx \frac{Gm.Vr}{\frac{\Delta Cp}{Cp}.KP.(Vgs - Vt)i.Vstep}$$ ……Eq(1.5)

When KP.(Vgs-Vt)I are the parameters of the NMOS transistors M12 and M14 with $\Delta Cp/Cp$=1%,Vstep=1.7V,Gm=500µA/V,KP.(Vgs-Vt)i=50µA/V(W/L) is approximately 5µm/2µm.it is interesting to remark that decreasing(W/L)I will result in a high accuracy. However as it is discussed later, this will also decrease the comparator speed. The way to increase the accuracy is to increase Gm.

The comparator speed:

Neglecting the second order effect, equations1.1, 1.2 can be simplified into (v1≈-V2).

$$t \approx \frac{1}{\alpha}.ln\left(\frac{-V1.2.gm}{Vin.Gm}+1\right)$$ ……Eq(1.6)

With $1/\alpha$ = Cp/gm≈0.7nSec,2.gm/Gm ≈ 1.2,v1 = -2 v and vin = 5mv, the comparator speed is t≈4.3nSec.

In Figure 8, the spice output response is represented for an input voltage Vin = 5mV. As can be seen the speed (4.2nSec) is very close to the calculated one. From equation 1.6, it can be concluded that the speed mainly depends on Cp/gm(=1/α).Cp is approximately the capacitance of the latch inverter plus the capacitance of the connected digital building block.as a result, the speed is approximately equal to the speed of a load inverter(≈2nSec) or is equal to the speed of digital circuits. however, if the W/L's of the latch transistors are further decreased (to increase the accuracy), the parasitic capacitances of the transconductance amplifier and the switch will become dominant, and as a result the comparator speed is going to decrease.to further increase the accuracy it is best to design the input stage with a higher transconductance (more GM but also more power drain). The total response time of this

configuration (include the reset phase) for an accuracy of 5mV becomes les then 10nSec

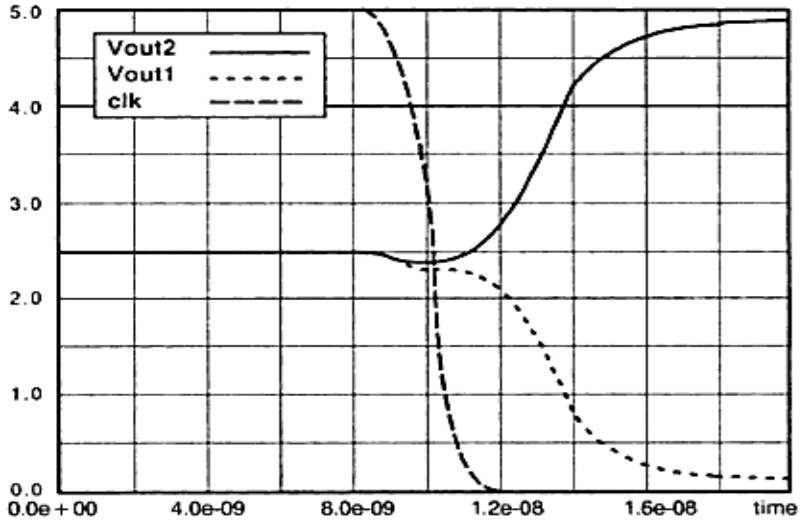


Figure.8: Output response of the high speed comparator

2.3 Resistive Divider Comparator

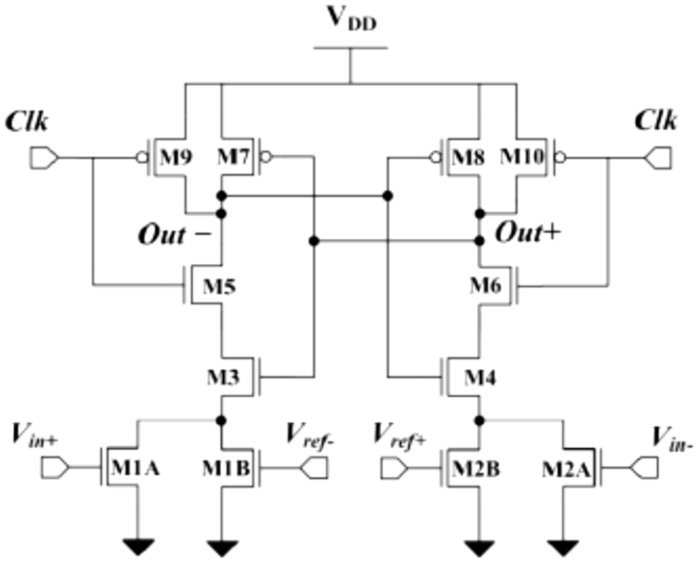


Figure.7: Resistive divider Comparator

Since the input transistor M1A/B and M2A/B operate in the triode region and act like voltage controlled resistors, this comparator is called "Resistive Divider Comparator." The advantage of this comparator [9] is its low power consumption (No DC power consumption) and adjustable threshold voltage (decision level) which is defined as

$$V_{in}(threshold) = \left(\frac{W_B}{W_A}\right) V_{ref} \quad \text{.....Eq(1.7)}$$

where $W_A = W_{1A} = W_{2A}$ $W_B = W_{1B} = W_{2B}$

$V_{in} = V_{in+} - V_{in-}$ $V_{ref} = V_{ref+} - V_{ref-}$

For the analysis, proposed form of the comparator shown in figure will be used.

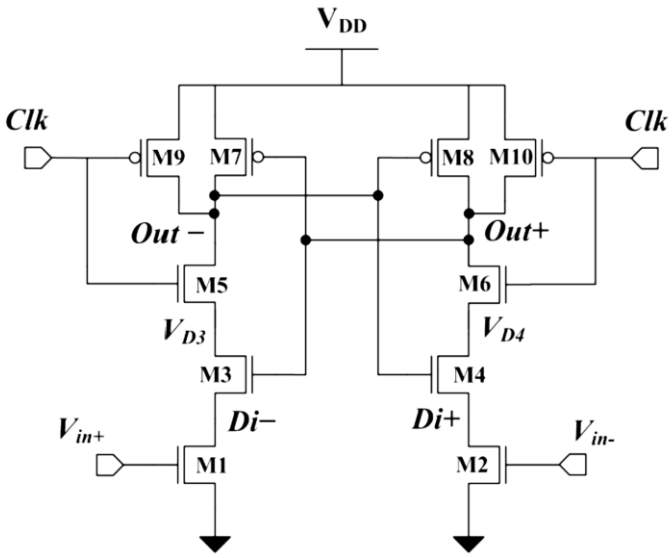


Figure.8: Proposed Resistive divider Comparator

During reset phase (*Clk=0V*), PMOS reset transistor M9 and M10 charge *Out* nodes upto *VDD* (this makes NMOS transistor M3 and M4 on and the node voltage at *VD3,4* discharge tog round) and input transistor M1 and M2 discharge *Di* nodes to ground while NMOS transistor M5 and M6 are off. During evaluation phase (*Clk=VDD*), as both switch transistorM5 and M6 are on, each node voltage at *Di+*and*Di−* instantly rises up to the certain values, which are defined as

$$V_{Di+} = \frac{r_{ds1\,on}}{r_{ds1\,on} + r_{ds3,4\,on} + r_{ds5,6\,on}} \times V_{out-}(\approx V_{DD}) \quad \text{.....Eq(1.8)}$$

$$V_{Di-} = \frac{r_{ds2\,on}}{r_{ds2\,on} + r_{ds3,4\,on} + r_{ds5,6\,on}} \times V_{out+}(\approx V_{DD}) \quad \text{.....Eq(1.9)}$$

Then, each Out node voltage starts to discharge from VDD to ground inversely proportional to the applied input voltage such a way that if Vin+ increases, then it makes VD decrease and increases VGS3,ID3,and decrease Vout-,VGS4But it will increase Vout+ and remaining load driving terminals(VGS3). With positive feedback operation from the back-to-back cross-coupled inverter pairs (M7/M3 and M8/M4), one Out node will discharge to ground and the other Out node will charge up to VDD again and this comparator will finish its comparison. Since the input transistor M1 and M2 are operated in the linear region during evaluation phase, the transconductance for those transistors are can be approximately written as

$$g_{m1,2} = \mu_n C_{ox}\left(\frac{W_{1,2}}{L}\right) V_{ds1,2} \quad \text{.....Eq(2.0)}$$

Also, because transistor M3 and M4 are operated in the saturation region during evaluation phase, the transconductance for those transistors are can be written as

$$g_{m3,4} = \mu_n C_{ox}\left(\frac{W_{3,4}}{L}\right)(V_{gs3,4} - V_{tn}) \quad \text{.....Eq(2.1)}$$

The transconductance of transistor M3 and M4 is much larger than that of the input transistor pair; hence the differential voltage gain built between *Di* nodes from the input transistor pair is not big enough to overcome an offset voltage caused from such a small mismatch between transistor M3 and M4 pair. As a result, those transistors are the most critical mismatch pair in this comparator and needed to be sized big enough to minimize the offset voltage at the cost of the increased power

consumption. Besides, the mismatch between transistor M5 and M6 pair (which is switches and operated in the linear region) also causes the considerable input-referred offset voltage. Furthermore, as the common mode voltage *Vcom* of the input transistor pair increases, the relative difference between the voltage controlled resistors (*rds1,2*) becomes smaller at the same amount of the input voltage difference Δ*Vin* and this in turn increases the offset voltage.

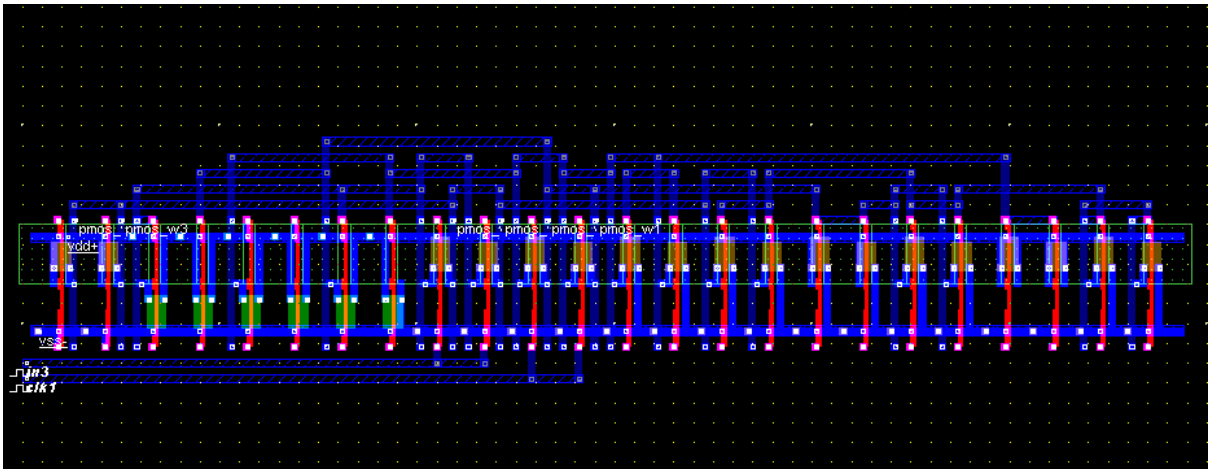


Figure.9: Layout of Resistive divider Comparator

III. SIMULATION WAVEFORMS

1. High Speed Latched Comparator

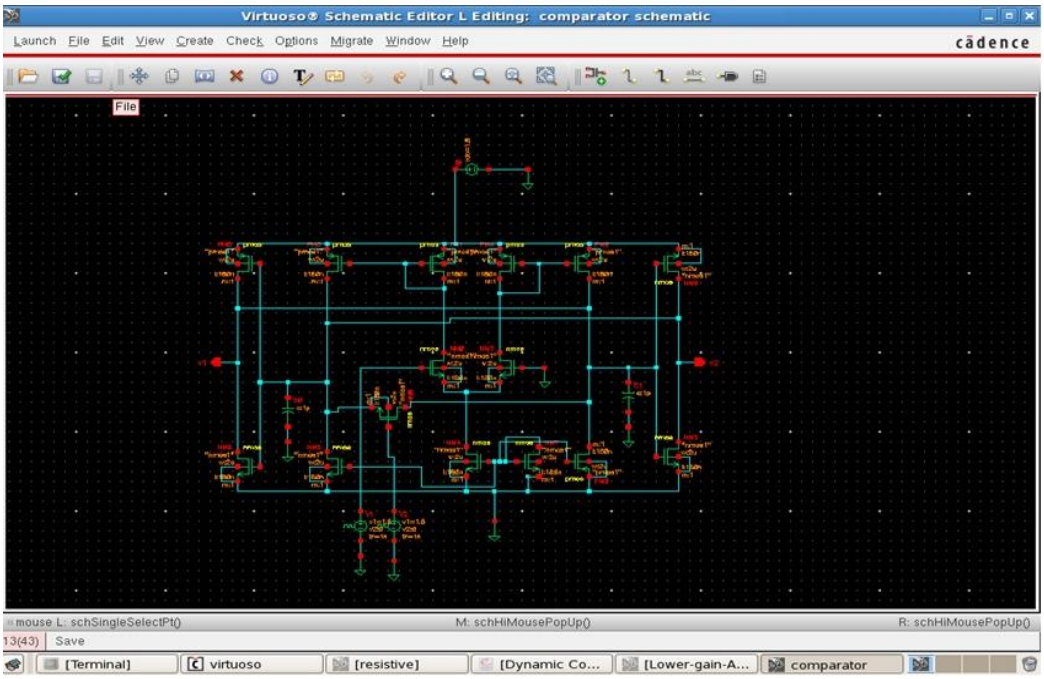


Figure.10: Schematic diagram of high speed latched comparator

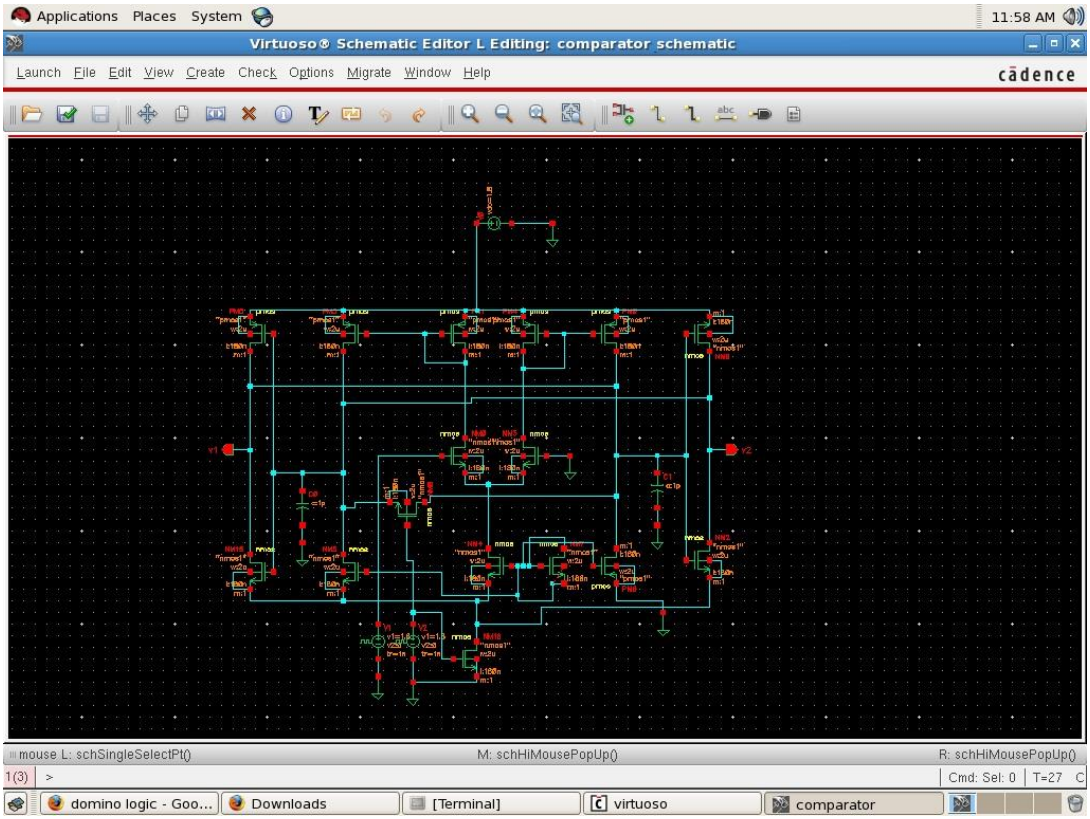


Figure.11: Response of high speed accurate Comparator With low power logic

2. Latched Comparator

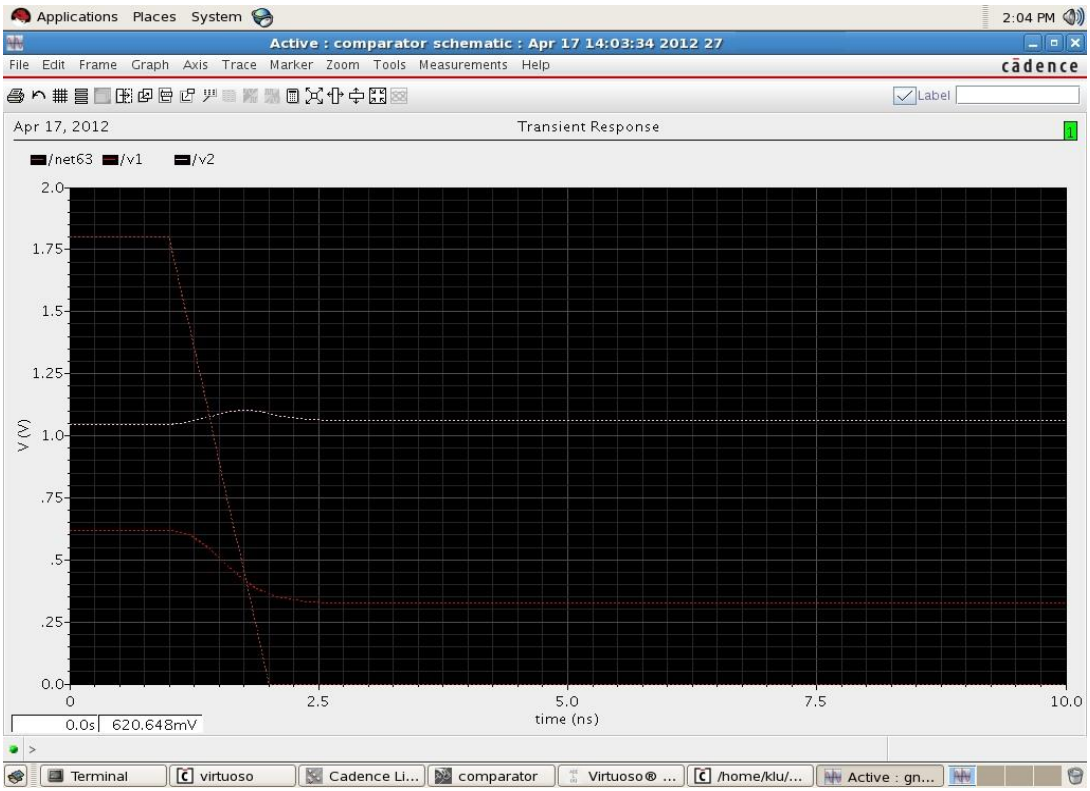


Figure.12: Transient response of Latched Comparator Implemented in Cadence

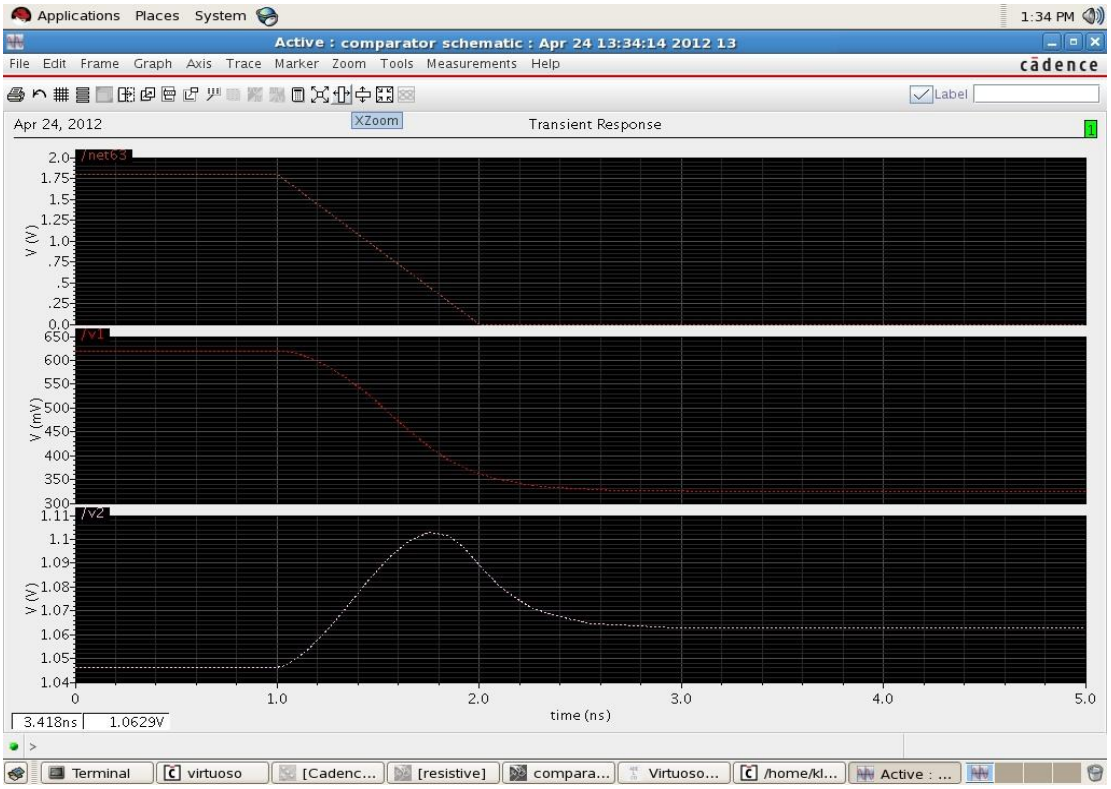


Figure.13: Transient response of Latched Comparator Implemented in Cadence

3. Resistive divider comparator*:*

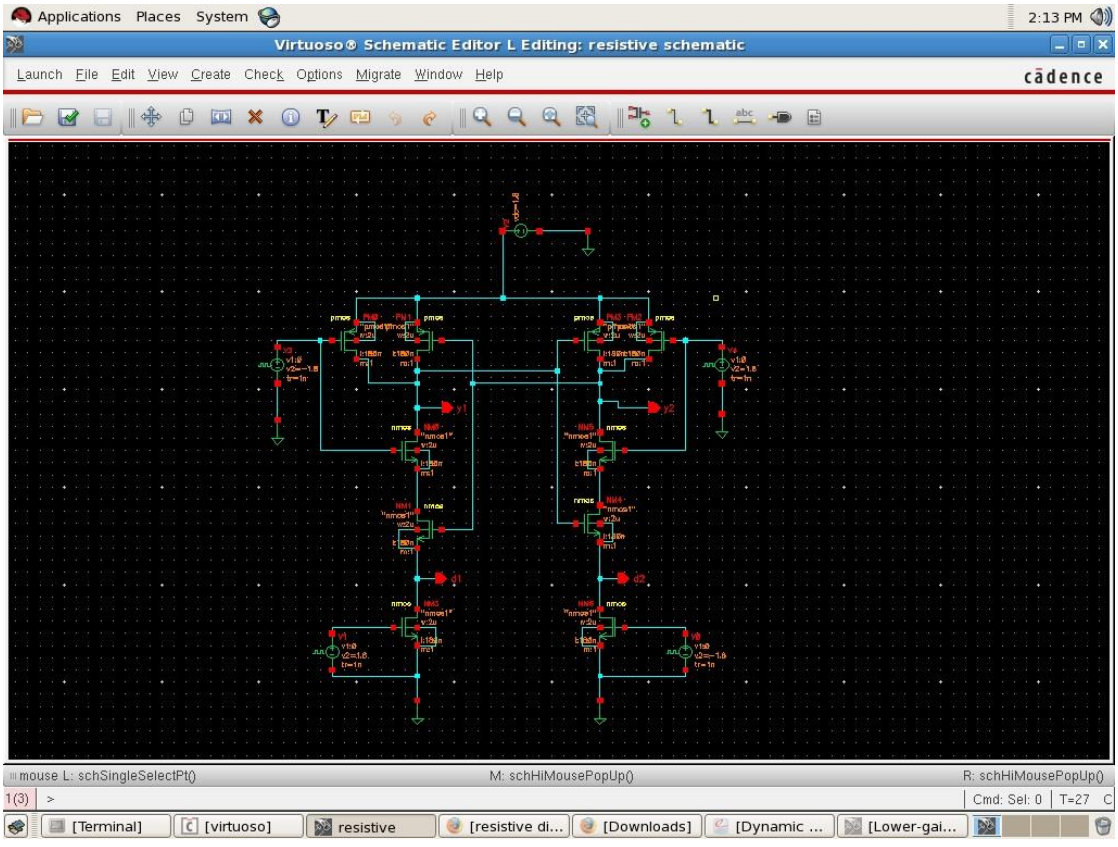


Figure.14: Resistive divider Comparator implemented in Cadence

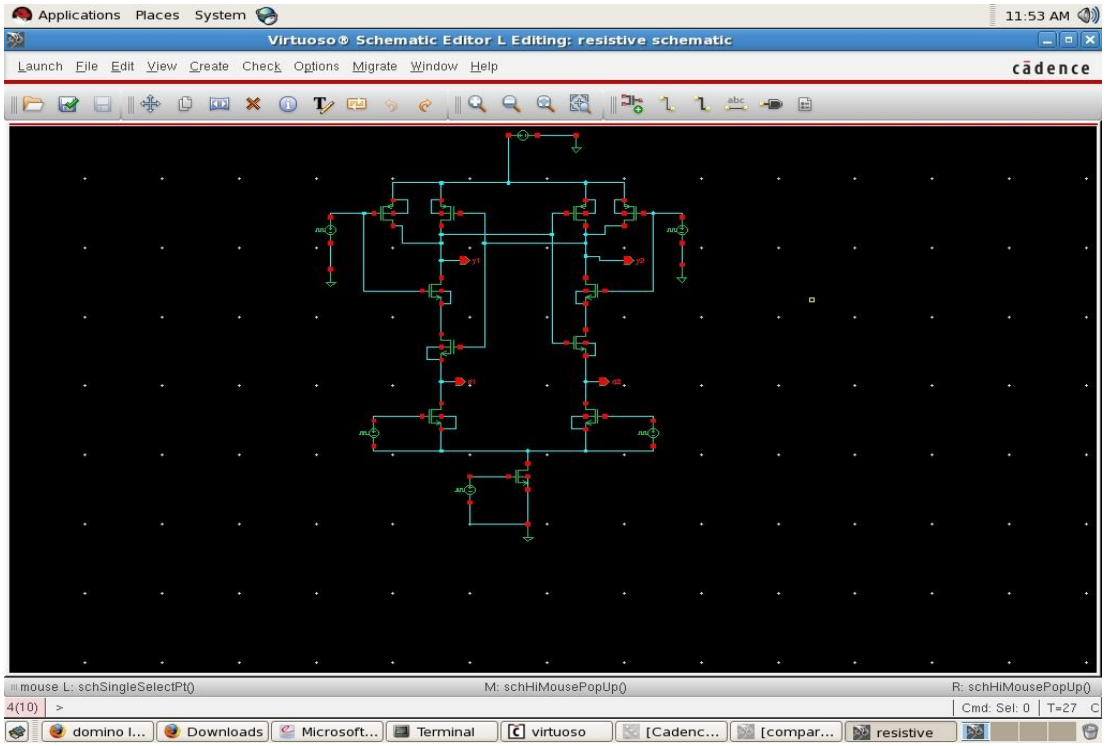


Figure.15: Resistive divider Comparator Implemented in Cadence with Low power Technique

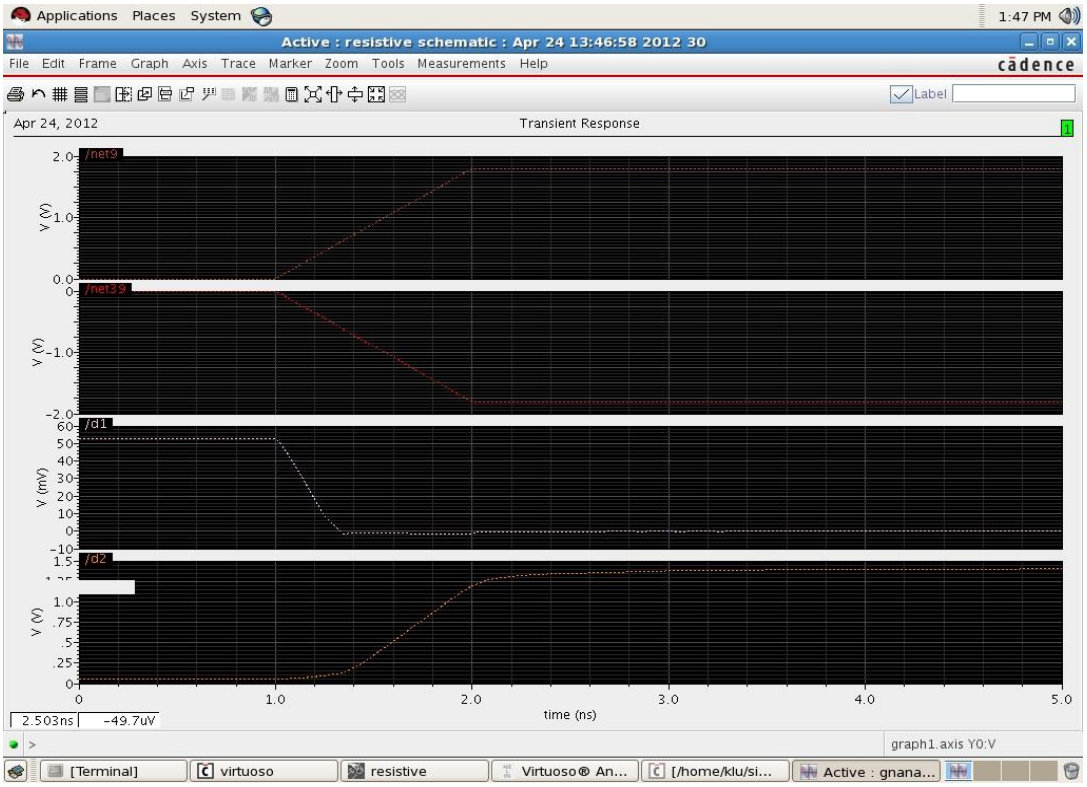


Figure.16: Transient response of Resistive divider Comparator Implemented in Cadence

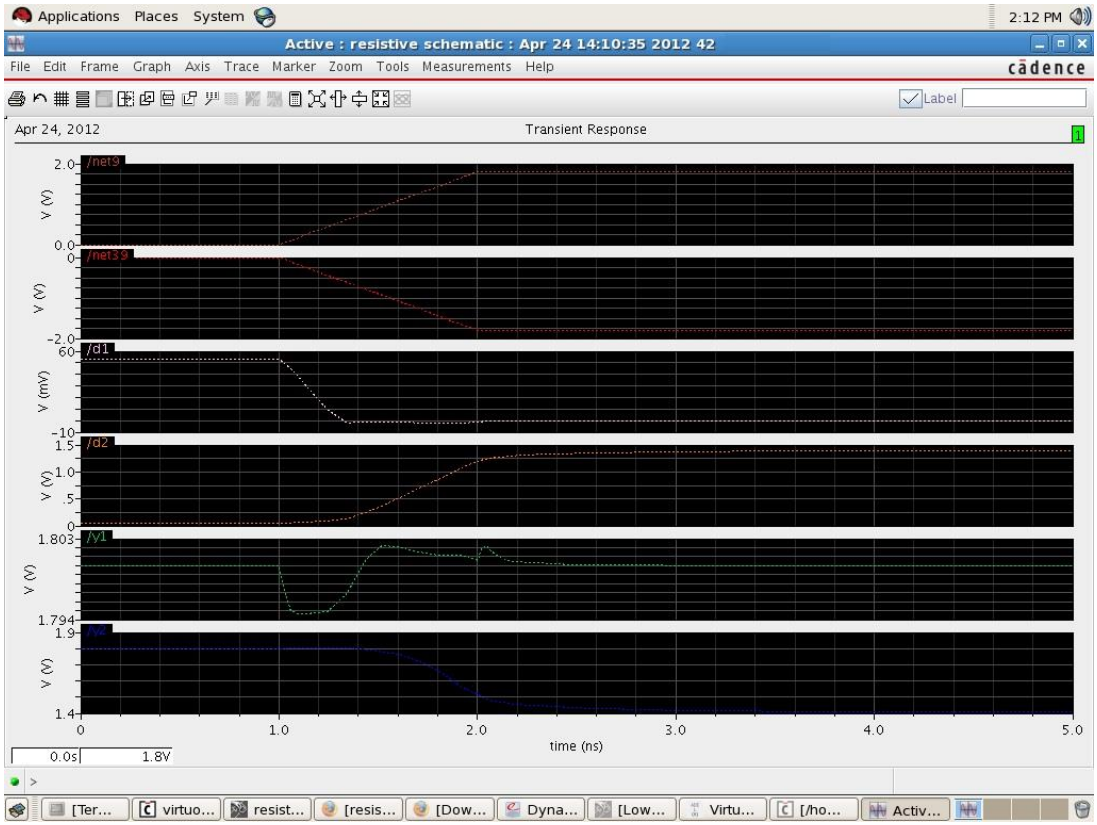
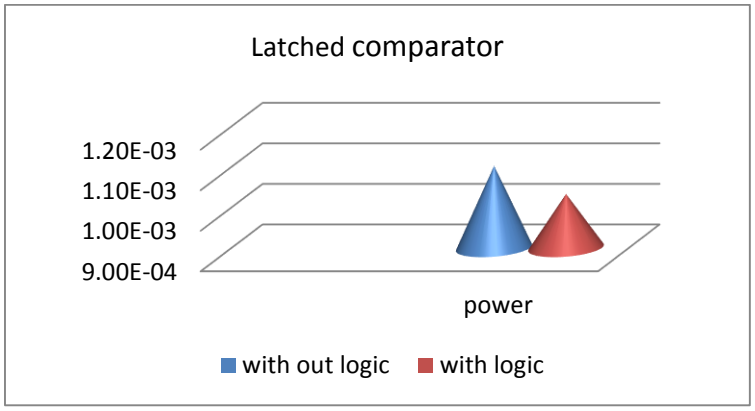
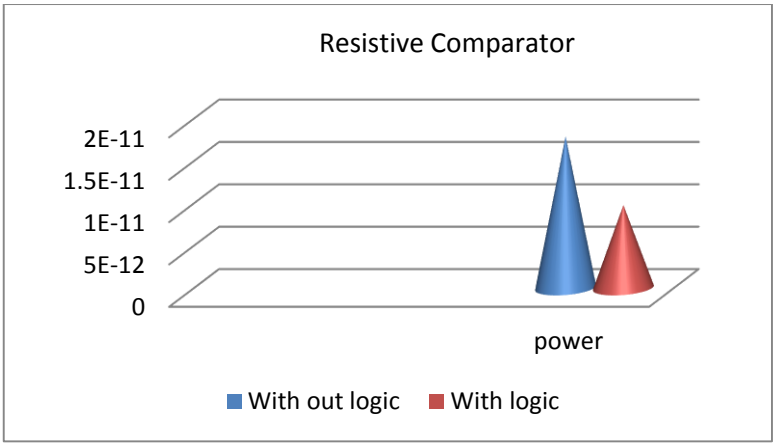


Figure.17: Transient response of Resistive divider Comparator Implemented in Cadence

IV. RESULTS AND DISCUSSION



Graph.1: Latched comparator



Graph.2: Resistive Comparator

Table.1: Comparison

Power Dissipation	Latched Comparator	Resistive divider Comparator
With Out Logic	1.10238 mw	17.8988 pw
With Logic	1.03378 mw	9.79285 pw

V. CONCLUSION

It can be concluded that despite its advantages such as zero-static power consumption and adjustable threshold voltage, since Lewis-Gray comparator shows a high offset voltage and its high offset voltage dependency on a different common mode voltage V_{com}, it is only suitable for low resolution comparison.The proposed low power technique for comparator is very effective for achieving a small area and low offset voltage comparator using a deep sub-micron CMOS technology.

VI. FUTURE WORK

Literature survey is going on various comparators which are using in flash ADC circuits. After the theoretical analysis is completed, Implementation is going to be done in various power reduction techniques with suitable mechanisms.

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