

# A COMPARISON OF I-V MODELS FOR CARBON NANOTUBE FIELD EFFECT TRANSISTORS

Roberto Marani and Anna Gina Perri

Electrical and Information Engineering Department, Electronic Devices Laboratory,  
Polytechnic University of Bari, via E. Orabona 4, Bari - Italy

## ABSTRACT

*In this paper we present a comparison among I-V models of CNTFETs proposed in literature in order to determine the model more easily implementable in simulation software for electronic circuit design. We have compared the CNTFETs model, already proposed by us, with Deng-Wong's and Koswatta's models. In particular our model, already structured to implement in simulator software, has been modified to characterize the I-V characteristics of CNTFETs below threshold. In this way it has been possible to have a more complete comparison, because the examined models consider the behaviour of device in sub-threshold regime. In spite of other models, our model seems to allow an easier implementation in the computer aided design of the most common analogue and digital circuits, showing a good agreement between the experimental and simulated characteristics, with processing times practically instant.*

**KEYWORDS:** *Nanoelectronic Device, Nanotechnology, Carbon Nanotube Field Effect Transistors, Modeling, Output and Transfer characteristics.*

## I. INTRODUCTION

In the nanoelectronic field the semiconductor industry and the whole scientific community are exploring a number of alternative device technologies. Some approaches involve moving away from traditional electron transport-based electronics: for example, the development of spin-based devices. Another approach, on which we focus here, maintains the operating principles of the currently used devices, primarily that of the field-effect transistor, but replaces the conducting channel with carbon nanomaterials such as one-dimensional (1D) Carbon NanoTubes or two-dimensional (2D) graphene layers.

These new devices, able to work better at nanometer scale, have molecular building block not coming from lithography and, along with these devices, molecular electronics will change the equation in our tool box, we will drop out well known partial differential equation for charge diffusion and we will use quantum mechanic to describe electrons, holes, atoms, molecules and photons.

CNTFETs, as already discussed, are field effect transistors using a carbon nanotube as channel, and are regarded as an important contending device to replace conventional silicon transistors [1].

As it is known, the carbon nanotubes consist in a hexagonal mesh of carbon atoms wrapped in cylinder shapes, some time with closing hemispherical meshes on the tips. Since they could be extended several millimeters, they have a huge length/diameter ratio making them unidimensional structures (1-D). Moreover an important characteristic of CNT is mesh torsion, denoted as *chirality*, which has a strong influence on the CNT behaviour. Depending on their chirality, electronic band structure changes, band gap can appear making them semiconductors, or cannot appear, making them conductors. Furthermore the CNT behaviour as semiconductor has an energy gap inversely proportional to their radius.

About modelling issues, most of the CNTFETs models available in literature are numerical and make use of self-consistency and therefore they cannot be directly implemented in modelling languages to design electronic circuits.

Nowadays the most widely used language available is SPICE, or any of its evolution, with various graphical interfaces. Another language which has a solid implementation is Verilog-A, which is very interesting since it allows devices description in a syntax quite near to C programming language.

In this paper we present a comparison among I-V models of CNTFETs proposed in literature [2-11]. In particular we analyze some models of CNTFETs, which can describe the device behavior also for low power applications (sub-threshold regime).

The aim of this paper is to identify the model, which can be easier implemented in simulation software for electronic circuit design.

The presentation of the paper is organized as follows. Section 2 gives a brief description of the CNTFET model proposed by us [2-3], while in Section 3 we have modified our model in order to have better simulations when supply voltage is lower than the threshold voltage of transistor.

Sections 4 and 5 describe respectively the main characteristics of Deng-Wong's and Koswatta's models [9] [10], which analyze the behavior of CNTFETs with a wide range of chiralities and diameters and for CNTFET with either metallic or semiconducting CNT conducting channel.

Moreover both models take into account also the quantum confinement effects on both circumferential and axial directions, the acoustical/optical phonon scattering in the channel region and the tunnel effect between semiconductor bands. The conclusions are described in Section 6.

## II. OUR MODEL [2-3]

Our I-V model, developed for a n-type conventional CNTFETs, is based on the hypothesis of ballistic transport and makes reference to a work of A. Raychowdhury *et al.* [11] and on the following improvements introduced by F. Prégaldiny *et al.* [12-13] to solve some numerical problems of the original paper [11].

When a positive voltage is applied between drain-source ( $V_{DS} > 0$  V), the hypothesis of ballistic transport allows to assert that the current is constant along the CNT and therefore it can be calculated at the beginning of the channel, near the source, at the maximum of conduction band, where electrons from the source take up energy levels related to states with positive wave number, while the electrons from the drain take up energy levels related to states with negative wave number.

When a positive voltage is applied between gate-source ( $V_{GS} > 0$  V), the conduction band at the channel beginning decreases by  $qV_{CNT}$ , where  $V_{CNT}$  is the surface potential and  $q$  is the electron charge. With the hypothesis that each sub-band decreases by the same quantity along the whole channel length, the drain current for every single sub-band can be calculated using the Landauer formula [14]:

$$I_{DSp} = \frac{4qkT}{h} \left[ \ln(1 + \exp \xi_{Sp}) - \ln(1 + \exp \xi_{Dp}) \right] \quad (1)$$

where  $k$  is the Boltzmann constant,  $T$  is the absolute temperature,  $h$  is the Planck constant,  $p$  is the number of sub-bands, while  $\xi_{Sp}$  and  $\xi_{Dp}$  have the following expressions:

$$\xi_{Sp} = \frac{qV_{CNT} - E_{Cp}}{kT} \quad \text{and} \quad \xi_{Dp} = \frac{qV_{CNT} - E_{Cp} - qV_{DS}}{kT} \quad (2)$$

being  $E_{Cp}$  the sub-bands conduction minima.

Therefore the total drain current can be expressed as [14]:

$$I_{DS} = \frac{4qkT}{h} \sum_p \left[ \ln(1 + \exp \xi_{Sp}) - \ln(1 + \exp \xi_{Dp}) \right] \quad (3)$$

We have considered the first five sub-bands, but we have verified only three sub-bands are required to describe the C-CNTFET behaviour having diameters ranging from 1 nm to 4 nm.

Moreover we have verified that the sub-band effect is hidden when the quantum resistance  $R_s$  of the doped source region in series with the parasitic ones of the electrodes is considered.

The surface potential,  $V_{CNT}$ , is evaluated by the following approximation:

$$V_{CNT} = \begin{cases} V_{GS} & \text{for } V_{GS} < \frac{E_C}{q} \\ V_{GS} - \alpha \left( V_{GS} - \frac{E_C}{q} \right) & \text{for } V_{GS} \geq \frac{E_C}{q} \end{cases} \quad (4)$$

where  $E_C$  is the conduction band minima for the first sub-band.

The parameter  $\alpha$  depends on the  $V_{DS}$  voltage and has the following expression [2-3]:

$$\alpha = \alpha_0 + \alpha_1 V_{DS} + \alpha_2 V_{DS}^2 \quad (5)$$

where  $\alpha_0$ ,  $\alpha_1$  and  $\alpha_2$ , functions of both CNTFET diameter and gate oxide capacitance  $C_{ox}$ , must be extracted from the experimental device characteristics [2-3].

Fig. 1 shows the 3D plot of  $\alpha$  versus the nanotube diameter and the voltage  $V_{DS}$ , having assumed  $C_{ox}$  equal to 3.8 pF/cm.

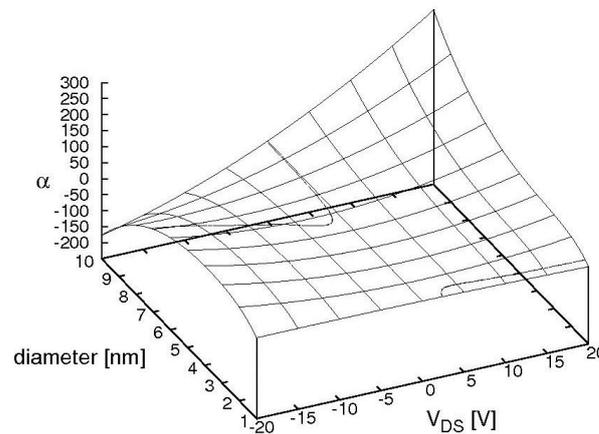


Figure 1. 3D plot of  $\alpha$  vs the nanotube diameter and the voltage  $V_{DS}$ .

In Fig. 1 we have highlighted two regions in which the  $\alpha$  parameter assumes negative values, not physically significant. Therefore Fig. 1 allows to assert the model describes the behaviour of CNTFET, having diameter between 1 nm and 4 nm, with a maximum value of  $V_{DS}$  equal to about 5 V, because, for  $V_{DS} > 5$  V,  $\alpha$  is negative.

As  $V_{CNT}(V_{GS})$  and its derivative are not continuous for  $V_{GS} = \frac{E_{Cp}}{q}$ , we have solved this problem

replacing Eqn. (4) with the following relationship [3]:

$$V_{CNT} = V_{GS} - \frac{\alpha \left( V_{GS} - \frac{E_C}{q} \right) + \sqrt{\left[ \alpha \left( V_{GS} - \frac{E_C}{q} \right) \right]^2 + 4\epsilon^2}}{2} \quad (6)$$

in which a smoothing parameter  $\epsilon$ , assumed equal to 0.05 V as in [13], has been introduced.

The difference between Eqn. (4) and Eqn. (6) is negligible when  $V_{GS}$  is outside the range

$$\left[ \frac{E_C}{q} - 2\epsilon, \frac{E_C}{q} + 2\epsilon \right].$$

Fig. 2 shows the surface potential  $V_{CNT}$  versus  $V_{DS}$  for different values of  $V_{GS}$ , while Fig. 3 allows to evaluate  $V_{CNT}$  for different values of the nanotube diameter.

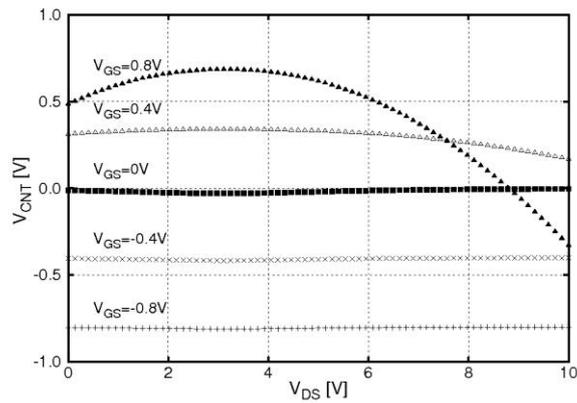


Figure 2.  $V_{CNT}$  vs  $V_{DS}$  for different values of  $V_{GS}$ .

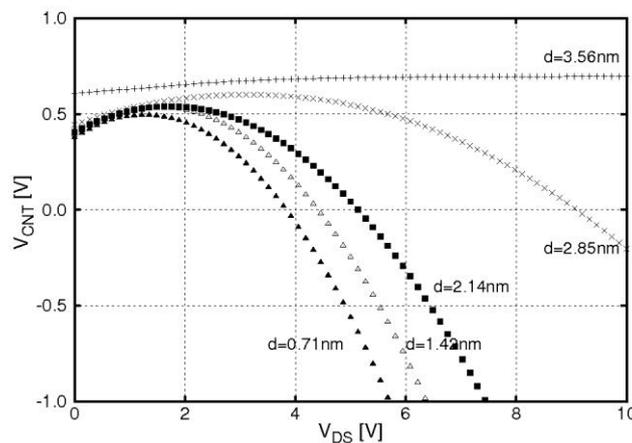


Figure 3.  $V_{CNT}$  vs  $V_{DS}$  for different values of the nanotube diameter.

Fig. 4, in which calculated values of  $I_{DS}$  vs  $V_{DS}$  for different values of  $V_{GS}$  are reported, allows to assert the model can well describe the behaviour of CNTFET with a maximum value of  $V_{DS}$  equal to 3 V.

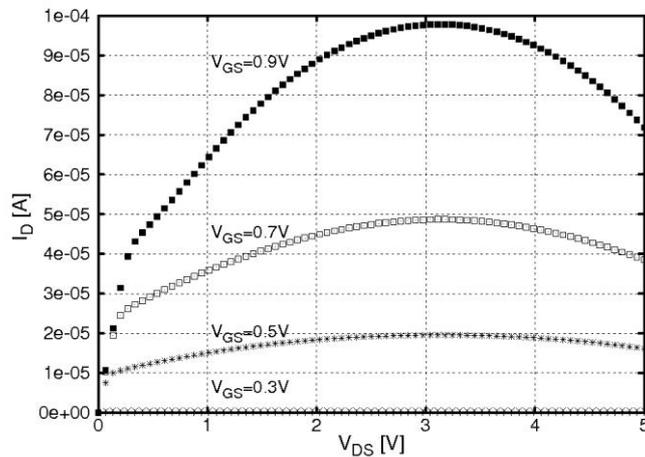


Figure 4.  $I_{DS}$  vs  $V_{DS}$  for different values of  $V_{GS}$ .

For  $V_{DS} \geq 3$  V, we assume that  $I_{DS}$  current has reached its saturation value, like MOSFET model.

Moreover from Fig. 5, which shows the computed values of current  $I_{DS}$  versus  $V_{DS}$  determined considering one, two, three and more sub-bands ( $p$ ), we have verified that only three sub-bands are sufficient to describe the output characteristics of the CNTFET with a relative error, referring to the  $I_{DS}$  values of the FETToy numerical model [15], less than 5%.

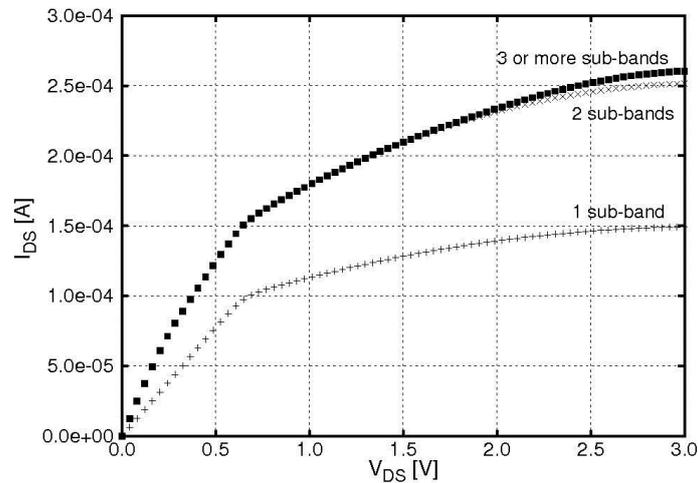


Figure 5.  $I_{DS}$  vs  $V_{DS}$  for a sub-band number  $p \geq 1$ .

### III. ID-VGS MODELLING IN SUBTHRESHOLD REGIME

For low power applications (when supply voltage is lower than the threshold voltage of transistor), such as hearing aids, the transistor operates in subthreshold regime. In this case it is important the ratio of on- to off-current ( $I_{on}/I_{off}$ ). This ratio characterizes the difference in current between a closed and open switch.

The on-current in MOSFETs decreases exponentially as the supply voltage is lowered. The same happens in carbon nanotube transistors. However, compared to MOSFETs, the off-current in CNTFETs continues to decrease as the voltage across the FET from drain to source decreases.

Carbon nanotubes have a varying  $I_{on}/I_{off}$  ratio, depending on the nanotube structure and properties [1] [4]. These very high current values in CNTs are due to their ballistic transport and their limited electron and hole scattering [3]. Therefore, CNTs have the ability to increase performance while adhering to lower power requirements in subthreshold circuits.

In this paragraph we describe our procedure to model the current in CNTFETs, operating in the low voltage, subthreshold regime, in order to determine the functionality of future subthreshold CNTFETs in digital design.

The total current in a CNTFET, as described previously, depends on the tunnelling current both of the holes and of the electrons through the source and drain Schottky barriers: the current in a CNTFET exponentially increases, reducing the thickness of the Schottky barrier at source, with also an increase of the subthreshold current.

In comparison with MOSFETs, in CNTFETs we have not the minimum current for  $V_{gs} = 0$  V, but to  $V_{gs} = V_{ds}/2$ . This is true for all CNTFETs having the same metal used for the gate, drain and source. This minimum condition  $V_{gs} = V_{ds}/2$  is independent on metal work function.

In order to model the  $I_D$ - $V_{GS}$  characteristics, we have implemented a Matlab code, characterized by a minimum current at  $V_{DS}/2$ , threshold voltage and exponential subthreshold current.

In particular the equations, which allow to value the current for a n-channel transistor (for a p-channel transistor we have the same expressions with negative voltages values), are reported in [6].

The obtained  $I_D$ - $V_{GS}$  characteristics, for a n-channel and a p-channel CNTFETs, are shown in Fig. 6 and 7 respectively.

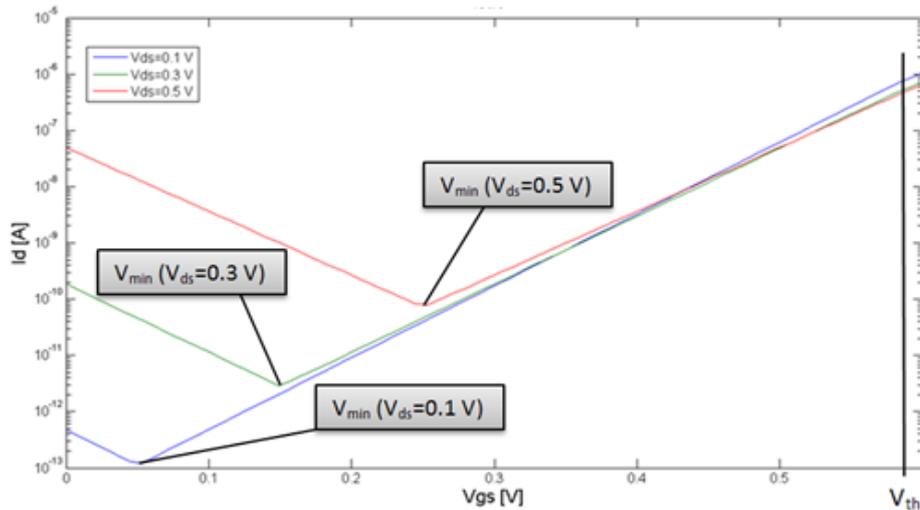


Figure 6. Simulated  $I_D$ - $V_{GS}$  characteristics of a n-channel CNTFET.

The CNTFET subthreshold regime is verified between the two threshold voltage ( $V_{th}$ ) points. These points have the same distance from the minimum voltage.

The distance from the minimum to the threshold is  $\square V_{SUB}(V_{DS}) = V_{th} - V_{min}$ .

In Fig. 8 we have reported the experimental  $I_D$ - $V_{GS}$  characteristics [16] [17] and our simulated ones, for a CNT diameter equal to 1,3 nm (up) and 2.5 nm (down).

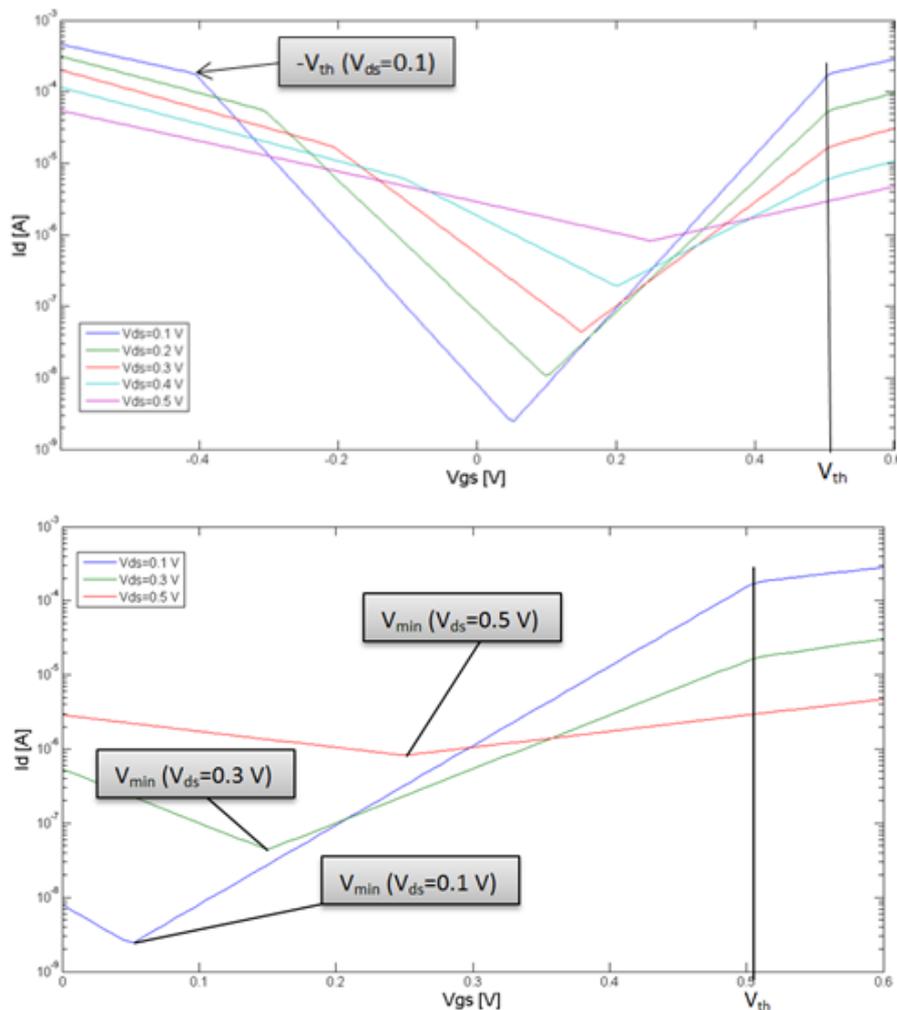
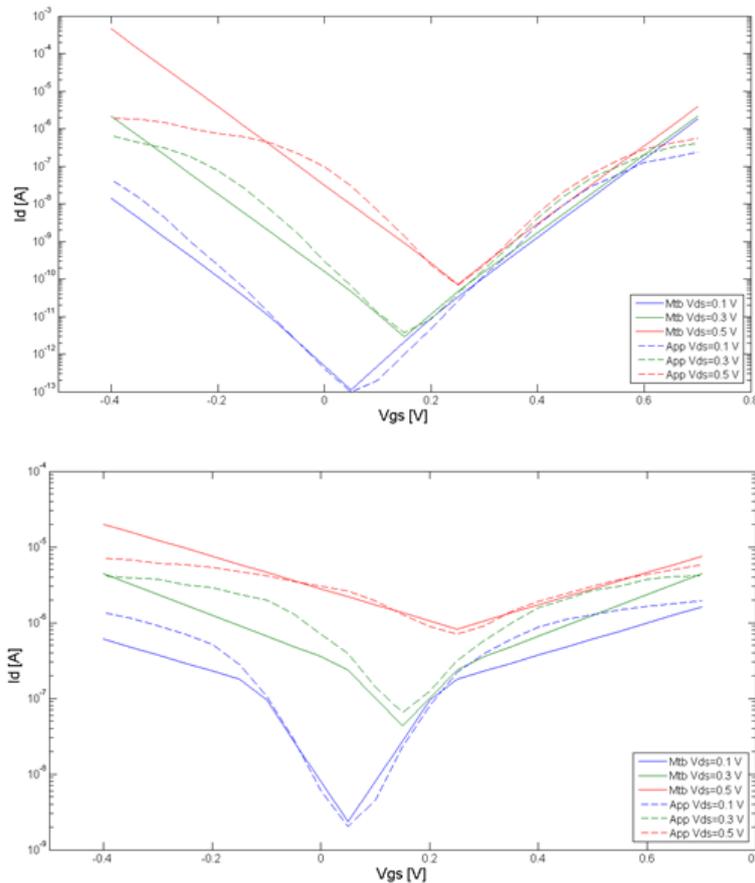


Figure 7. Simulated  $I_D$ - $V_{GS}$  characteristics of a p-channel CNTFET.



**Figure 8.** Comparison between the experimental  $I_D$ - $V_{GS}$  characteristics and our simulated ones.

In order to compare our model with experimental results, in Tables 1a) and 1b) we have reported the numerical values of  $V_{min}$ ,  $I_{Dmin}$  and  $V_{th}$ , obtained in [16][17] and those obtained by our model, for two CNTFETs having diameters ( $D_t$ ) 1.3 nm and 2.5 nm respectively. Moreover  $h_n$  is a constant depending on the process variations [16].

**Table 1a.** Numerical values of  $V_{min}$ ,  $I_{Dmin}$  and  $V_{th}$ , obtained in [16][17] (blue) and those obtained with our model (red), for a CNTFET having diameter  $D_t$  equal to 1.3 nm.

| $V_{ds}$ [V] | $V_{min}$ [V] | $I_{Dmin}$ [A]        | $V_{th}$ [V] | $h_n$ [ $V^{-1}$ ] | $D_t$ [nm] |
|--------------|---------------|-----------------------|--------------|--------------------|------------|
| 0.1          | 0.05          | $1.19 \cdot 10^{-13}$ | 0.58         | 16.1               | 1.3        |
|              | 0.05          | $1.11 \cdot 10^{-13}$ | 0.6          |                    |            |
| 0.3          | 0.15          | $2.83 \cdot 10^{-12}$ | 0.58         | 16.1               | 1.3        |
|              | 0.15          | $3.73 \cdot 10^{-12}$ | 0.6          |                    |            |
| 0.5          | 0.25          | $7.71 \cdot 10^{-11}$ | 0.58         | 16.1               | 1.3        |
|              | 0.25          | $7.22 \cdot 10^{-11}$ | 0.6          |                    |            |

**Table 1b.** Numerical values of  $V_{min}$ ,  $I_{Dmin}$  and  $V_{th}$ , obtained in [16][17] (blue) and those obtained with our model (red), for a CNTFET having diameter  $D_t$  equal to 2.5 nm

| $V_{ds}$ [V] | $V_{min}$ [V] | $I_{Dmin}$ [A]       | $V_{th}$ [V] | $h_n$ [ $V^{-1}$ ] | $D_t$ [nm] |
|--------------|---------------|----------------------|--------------|--------------------|------------|
| 0.1          | 0.05          | $2.34 \cdot 10^{-9}$ | 0.50         | 14.6               | 2.5        |
|              | 0.05          | $2.03 \cdot 10^{-9}$ | 0.45         |                    |            |
| 0.3          | 0.15          | $4.38 \cdot 10^{-8}$ | 0.50         | 14.6               | 2.5        |
|              | 0.15          | $6.42 \cdot 10^{-8}$ | 0.45         |                    |            |
| 0.5          | 0.25          | $8.19 \cdot 10^{-7}$ | 0.50         | 14.6               | 2.5        |
|              | 0.25          | $7.02 \cdot 10^{-7}$ | 0.55         |                    |            |

From Fig. 8 and Tables 1a) and 1b), it is easy to see a good agreement between the experimental and simulated  $I_D$ - $V_{GS}$  characteristics, with a negligible relative error, and this supports the validity of our approach. Moreover, the computation is instantly, or with processing times too short to be evaluated. To perform all the simulations we have used a common Windows-based PC, equipped with a Pentium IV CPU and main memory of 1 Gbyte.

#### IV. DENG-WONG'S MODEL [9]

The model, proposed in literature by Deng-Wong [9], analyzes the intrinsic region of channel for a MOSFET-like CNTFET with a single-walled CNT. The discussion is valid for CNTFET consist of both metallic nanotubes that semiconductors, with a diameter and a chirality that may belong to a wide range.

The analysis has been focused on a single intrinsic channel of a CNTFET, so it is possible to assume a quasi-ballistic transport and lack of parasitic capacities and resistances. For the MOSFET-like CNTFET, as the behavior of a pFET is very similar to a nFET, only one of the two configurations has been taken into account (n-type).

In this model three types of current that contribute to the total one are considered:

1. the thermionic current due to semiconductor bands
2. the current supplied from the metal bands, in the case where there are metallic CNTs
3. the leakage current caused by the tunnel effect between semiconductor bands.

In particular the last one becomes significant in the subthreshold region, that is for negative voltages in a n-FET.

Moreover this model is valid for CNTFET with a wide range of chiralities and diameters and for CNTFET with either metallic or semiconducting carbon-nanotube conducting channel.

This model takes into account also the non-idealities, that to say the quantum confinement effects on both circumferential and axial directions, the acoustical/optical phonon scattering in the channel region, and the screening effect by the parallel CNTs for CNTFET with multiple CNTs.

Assuming a ballistic transport, in [9] it is possible to see that there is little difference (< 3%) between the on-current for an infinitely long gate length and the on-current for a 100-nm gate-length device; With 32-nm gate length, the on-current is about 90% of the long-channel value. This slight ballistic current drop from long-channel to short-channel devices is due to the energy quantization in the axial direction. Phonon scattering in the 32-nm-long channel region further reduces the on-current of about 7%.

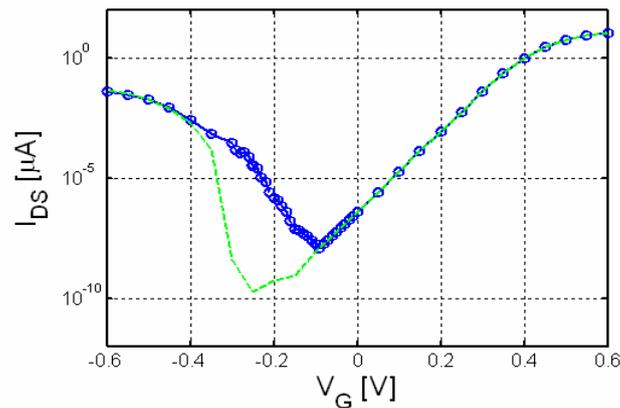
The leakage current caused by the tunnel effect between semiconductor bands is only significant with high values of  $V_{DS}$ , and the subthreshold slope gets worse with larger electrostatic capacitance between the channel and the substrate.

These results have allowed us to neglect the non-idealities in our model, because we have verified [2-3] they have small influence in the computer aided design in the most common analogue and digital circuits [5] [7-8].

#### V. KOSWATTA'S MODEL [10]

The leakage current caused by the tunnel effect between semiconductor bands (Band To Band Tunneling, BTBT) has been already analyzed in [10], in which two processes of BTBT are considered: the first one analogue to that proposed in [9] and a second process in which the phonon-electron scattering is taken into account.

In particular the effect of the electron-phonon scattering is most visible in the current dependence from the gate voltage, as shown in Fig. 9.



**Figure 9.**  $I_{DS}$  vs.  $V_{GS}$ , for  $V_{DS} = 0.1$  V: without scattering (dashed line); with phonon scattering (solid line with circles) [from 10].

The dotted green line represents the I-V characteristic in the ballistic approximation, the continuous blue one takes into account the scattering. The two curves are almost identical for large positive or negative values of the applied voltage.

In particular, for positive voltages, the current saturates when the potential barrier formed by the channel is low enough to allow all carriers able to flow through without undergoing reflections. The current decreases as the voltage with a slope of approximately 60 mV/decade, as expected for a flow above the barrier, due to the tail of the Fermi distribution.

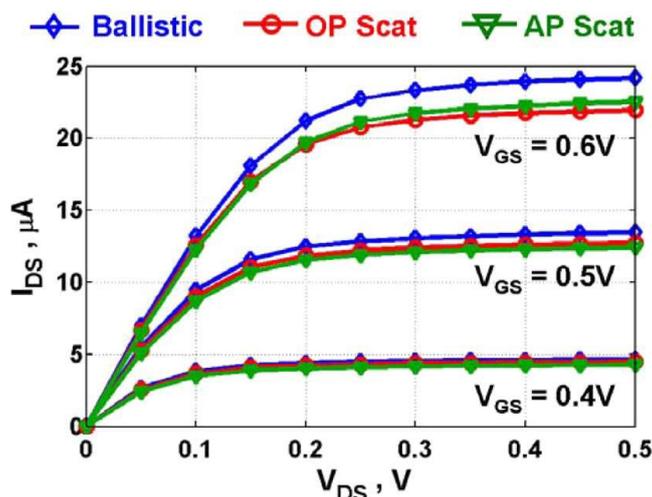
We have an increase of the current for negative voltages, when tunnel effect comes into play. This happens if the condition occurs for which the top of the valence band in the channel is aligned with the bottom of the conduction band of the source. Another condition that contributes to the phenomenon is the presence of empty states on the drain at the same energy. Then, the current saturates for large negative voltages and when a sufficient number of discrete states is at an energy such as to allow the transfer of carriers from the states of the source, filled, to those of the drain, empty.

The difference between the ballistic case and the one that considers the scattering phenomenon is pronounced for small gate voltages.

As can be seen in Fig. 9, the threshold voltage relative to the tunnel effect, in the presence of electron-phonon scattering, is moved to the right: this type of conduction is possible through the emission of a phonon, when the top of the valence band in the channel is at an energy lower than the bottom of the conduction band in the source. This is in agreement with the fact that the displacement of the voltage is approximately equal to the energy of a phonon.

Moreover Fig.9 shows the existence of a steep slope in the sub-threshold region, less than 60 mV/dec at room temperature. Therefore the current in CNTFETs., operating in the low voltage, subthreshold regime, it is crucial to include the effects of scattering electrons-phonons, in order to obtain the correct value of the threshold voltage.

This statement is confirmed examining Fig. 10, which compares the  $I_{DS}-V_{DS}$  characteristics in case of ballistic transport and in the presence of scattering.

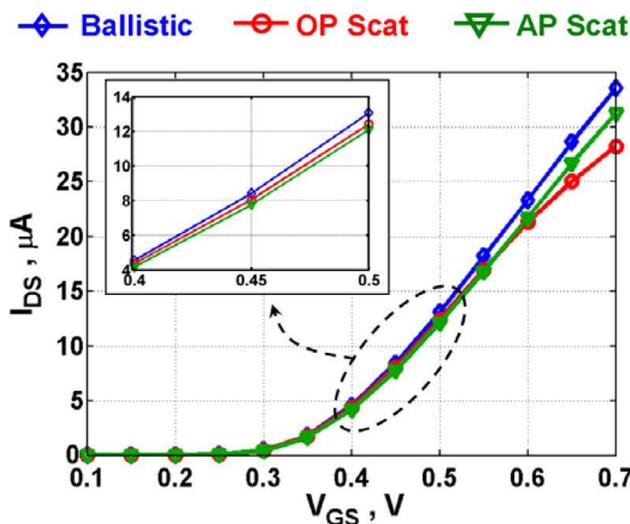


**Figure 10.**  $I_{DS}$ - $V_{DS}$  for the (16,0) CNTFET under ballistic transport, OP scattering and AP scattering [from 10].

We note immediately that the scattering has an appreciable influence on the ON current of the device. In particular, we must distinguish two situations of scattering: for  $V_{GS} = 0.6$  V, the current is reduced of about 9% compared to the ballistic case in the presence of optical phonons and of 7% with acoustic phonons.

Moreover, for moderate gate voltages ( $V_{GS} \leq 0.5$  V), the effect of acoustic phonons is greatest; for higher values of  $V_{GS}$  ( $V_{GS} \geq 0.6$  V), electron-optical phonons scattering becomes predominant.

This is confirmed also examining Fig. 11, which shows the  $I_{DS}$ - $V_{GS}$  characteristics in case of ballistic transport and in the presence of scattering.



**Figure 11.**  $I_{DS}$ - $V_{GS}$  for the (16,0) CNTFET under ballistic transport, OP scattering and AP scattering [from 10].

The insert of Fig. 11 shows that for moderate values of  $V_{GS}$ , electron-acoustic phonon scattering prevails compared to that of optical phonons, while for values  $V_{GS} \geq 0.6$  V the situation is opposite, as we have already said.

## VI. CONCLUSIONS AND FUTURE DEVELOPMENTS

In this paper a comparison among some I-V models of CNTFETs proposed in literature [2-11] is presented, in order to identify the model more easily implementable in simulation software for electronic circuit design.

In particular we have compared the CNTFETs model, already proposed by us [2-8], with those proposed in [9] and [10].

Our model, based on the hypothesis of fully ballistic transport in a mesoscopic system between two non-reflective contacts, utilizes analytical approximations, derived from quantum mechanical simulations of the devices, in order to avoid the resort to self-consistency and to obtain a structure to implement in simulator software.

Moreover we have modified our model to characterize the I-V characteristics of CNTFETs below threshold. In this way it has been possible to have a better comparison since the examined models [9] [10] consider the behaviour of device in sub-threshold regime, taking into account the quantum confinement effects on both circumferential and axial directions, the acoustical/optical phonon scattering in the channel region and the tunnel effect between semiconductor bands.

Compared to the other models, our model seems to allow an easier implementation in circuit simulators, showing a good agreement between the experimental and simulated characteristics, with processing times instant or too short to be evaluated.

In the future, in order to validate the implementation of the proposed CNTFET model, we will utilize it, both in Verilog-A and in SPICE simulators, to design typical analogue circuits and logic blocks. In particular, for these applications it has been necessary to model the current in CNTFETs, operating in the low voltage, subthreshold regime to determine the functionality of future subthreshold CNTFETs.

## REFERENCES

- [1] Avouris Ph., Radosavljević M., Wind S. J., (2005) "Carbon Nanotube Electronics and Optoelectronics", in: Rotkin SV, Subramone S, editors. "Applied Physics of Carbon Nanotubes: Fundamentals of Theory, Optics and Transport Devices", Berlin Heidelberg; Springer-Verlag, ISBN: 978-3-540-23110-3.
- [2] Marani R., Perri A. G., (2011) "A Compact, Semi-empirical Model of Carbon Nanotube Field Effect Transistors oriented to Simulation Software"; *Current Nanoscience*, vol. 7, issue 2, pp. 245-253.
- [3] Gelao G., Marani R., Diana R., A. G. Perri A. G., (2011) "A Semi-Empirical SPICE Model for n-type Conventional CNTFETs"; *IEEE Transactions on Nanotechnology*, vol. 10, issue 3, pp.506-512.
- [4] Marani R., Perri A. G., (2012) "A DC Model of Carbon Nanotube Field Effect Transistor for CAD Applications"; *International Journal of Electronics*, vol, 99, n. 3, pp. 427 - 444.
- [5] Marani R., Perri A. G., (2012) "Simulation of CNTFET Digital Circuits: a Verilog-A Implementation"; *International Journal of Research and Reviews in Applied Sciences*, vol. 11, issue 1, pp. 74-81.
- [6] Marani R., Perri A. G., (2012) "Modelling and Implementation of Subthreshold Currents in Schottky Barrier CNTFETs for Digital Applications"; *International Journal of Research and Reviews in Applied Sciences*, vol. 11, issue 3, pp. 377-385.
- [7] Marani R., Gelao G., Perri A.G., (2012) "Comparison of ABM SPICE library with Verilog-A for Compact CNTFET model implementation"; *Current Nanoscience*, vol. 8, issue 4, pp. 556-565.
- [8] Marani R., Gelao G., Perri A.G., (2013) "Modelling of Carbon Nanotube Field Effect Transistors oriented to SPICE software for A/D circuit design"; *Microelectronics Journal*, DOI:10.1016/j.mejo.2011.07.012, pp.33-39.
- [9] Deng J., Wong H.-S. P., (2007) "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Non idealities and Its Application—Part I: Model of the Intrinsic Channel Region", *IEEE Transactions on Electron Devices*, Vol. 54, n. 12, pp. 3186 - 3194.
- [10] Koswatta S., Lundstrom M. S., Anantram M. P., Nikonova D. E., (2005) "Simulation of Phonon-Assisted Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors", *Applied Physics Letters*, vol. 87, n. 2, pp. 87 - 89 .
- [11] Raychowdhury A., Mukhopadhyay S., Roy K., (2004) "A Circuit-Compatible Model of Ballistic Carbon Nanotube Field-Effect Transistors", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 23, n. 10, pp. 1411-1420.
- [12] Prégaldiny F., Lallement C., Kammerer JB., (2006) "Design-Oriented Compact Models for CNTFETs, *Proceedings of International Conference on Design and Test of Integrated Systems in Nanoscale Technology*, Tunis.
- [13] Prégaldiny F., Lallement C., Diange B., Sallese M., Krummenacher M., (2007), "Compact Modeling of Emerging Technologies with VHDL-AMS", Huss SA, editor, *Advances in Design and Specification Languages for Embedded Systems*, Dordrecht: Springer Netherlands; ISBN: 978-1-4020-6147-9.
- [14] Datta S., (1995) "Electronic transport in mesoscopic systems," in *Cambridge Studies in Semiconductor Physics and Microelectronic Engineering*. vol. 3, New York: Cambridge University Press, ISBN:978-0-521-599943-6.

- [15] Rahman A., Wang J., Guo J., Hassan MdS., Liu Y., Matsudaira A., Ahmed S., Datta S., Lundstrom M., (2006) "FETToy", <http://www.nanohub.org>.
- [16] Appenzeller J., Knoch J., Derycke V., Martel R., Wind S., Avouris Ph., (2002) "Field modulated carrier transport in carbon nanotube transistors", *Physical Review Letters*, vol. 89 126801.1—126801.4.
- [17] Avouris Ph., Martel R., Derycke V., Appenzeller J., (2002) "Carbon nanotube transistors and logic circuits", *Physica B: Condensed Matter*, vol. 323, pp. 6 - 14.

## AUTHORS

**Roberto Marani** received the Master of Science degree (cum laude) in Electronic Engineering in 2008 from Polytechnic University of Bari, where he received his Ph.D. degree in Electronic Engineering in 2012.

He worked in the Electronic Device Laboratory of Bari Polytechnic for the design, realization and testing of nanometrical electronic systems, quantum devices and FET on carbon nanotube. Moreover Dr. Marani worked in the field of design, modelling and experimental characterization of devices and systems for biomedical applications.

In December 2008 he received a research grant by Polytechnic University of Bari for his research activity. From February 2011 to October 2011 he went to Madrid, Spain, joining the Nanophotonics Group at Universidad Autónoma de Madrid, under the supervision of Prof. García-Vidal.

Currently he is involved in the development of novel numerical models to study the physical effects that occur in the interaction of electromagnetic waves with periodic nanostructures, both metal and dielectric. His research activities also include biosensing and photovoltaic applications.

Dr. Marani is a member of the COST Action MP0702 - Towards Functional Sub-Wavelength Photonic Structures, and is a member of the Consortium of University CNIT – Consorzio Nazionale Interuniversitario per le Telecomunicazioni.

Dr. Marani has published over 100 scientific papers.



**Anna Gina Perri** received the Laurea degree cum laude in Electrical Engineering from the University of Bari in 1977. In the same year she joined the Electrical and Electronic Department, Polytechnic University of Bari, Italy, where she is Full Professor of Electronics from 2002.

From 2003 she has been associated with the National Institute of Nuclear Physics (INFN) of Napoli (Italy), being a part of the TEGAF project: "Teorie Esotiche per Guidare ed Accelerare Fasci", dealing with the optimal design of resonance-accelerating cavities having very high potentials for cancer hadrontherapy.

In 2004 she was awarded the "Attestato di Merito" by ASSIPE (ASSociazione Italiana per la Progettazione Elettronica), Milano, BIAS'04, for her studies on electronic systems for domiciliary teleassistance.

Her current research activities are in the area of numerical modelling and performance simulation techniques of electronic devices for the design of GaAs Integrated Circuits and in the characterization and design of optoelectronic devices on PBG (Photonic BandGap).

Moreover she works in the design, realization and testing of nanometrical electronic systems, quantum devices, FET on carbon nanotube and in the field of experimental characterization of electronic systems for biomedical applications.

Prof. Perri is the Head of the Electron Devices Laboratory of the Polytechnic University of Bari.

She has been listed in the following volumes: Who's Who in the World and Who's Who in Engineering, published by Marquis Publ. (U.S.A.).

She is author of over 250 journal articles, conference presentations, twelve books and currently serves as Referee of a number of international journals.

Prof. Perri is the holder of two Italian patents and the Editor of two international books.

She is also responsible for research projects, sponsored by the Italian Government.

Prof. Perri is a member of the Italian Circuits, Components and Electronic Technologies – Microelectronics Association, and an Associate Member of National University Consortium for Telecommunications (CNIT).

Prof. Perri is a Member of Advisory Editorial Board of International Journal of Advances in Engineering & Technology and of Current Nanoscience (Bentham Science Publishers).

